Validation of a High-Performance Emulator for SVF

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The next generation of onboard processors represented by the LEON2 and LEON3 present a challenge for engineers wishing to validate onboard software (OBSW) in a real-time context or wishing to run the OBSW within a real-time simulator. Processor emulation technology successfully used for ERC32 represented by Gaisler's TSIM, SpaceBel's LEON SVE and ESA/ESOC's ERC32 Emulator does not allow real-time performance on today's hardware when applied to a LEON processor.

One solution being explored by Gaisler and Astrium is a hardware-based emulator. Another approach, explored by SciSys first for the ERC32 and now for LEON, has been to use dynamic translation emulator technology. This approach was also explored before by the University of Coimbra, which implemented a dynamic translator for the LEON2 processor (LeonVM), proving that real-time performance was achievable.

Dynamic Translation offers performance improvement of 5-10 times over traditional emulators while retaining the benefits of software based emulators. It works by translating blocks of code from the target (LEON) to the host (e.g. Intel) on the fly and storing these blocks in RAM. When the code blocks are called again they are accessed from RAM and do not have to be translated again, giving a significant performance gain. SciSys has already used a dynamic translation emulator (QERC, based on QEMU) in the context of the Galileo Constellation Simulator project and recognised from the beginning the possible benefits for LEON based missions. Under an ESA Innovation Triangle Initiative, SciSys with its partners FFQTECH and the University of Coimbra are assessing the applicability of this technology to be used within a Software Validation Facility.

The project includes the following activities:

- Identify possible performance enhancements, the benefits from the enhancements and implement those which offer the biggest benefit.
- Assess the impact (if any) of dynamic translation on instruction timing accuracy and the timing of I/O interactions.
- Assess and adopt the latest improvements to QEMU (e.g. removal of compiler dependency and instruction timing enhancements).
- Implement the selected QEMU enhancements to create a derivative that can be used in an SVF (QERL) that will support both LEON and ERC32.
- Implement a TSIM-like interface to allow it to be readily interchanged with TSIM.
- Validate and compare performance with the QEMU baseline.
- Compare performance against another LEON emulator (TSIM) running the same ERC32 and LEON OBSW in the ESA VSRF/RSVF.

The paper will report the latest status of this project, what has been achieved and present early results that have been obtained.