SIMLEON : A LEON processor emulator

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Outline

- Background
- Development process
- Current status & users
- Future work
- Conclusion

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Background

- 1750 emulators
  - At CNES
    - First development for the SPOT family in 1985
    - Reused for the PROTEUS family since 1998
  - At ASTRIUM
    - First development for E3000 operation simulator in 1998
    - Used for :
      - 15 telecom spacecrafts
      - Rocsat and Theos earth observation satellites
    - Improved version to achieve SW validation developed for METOP to replace HW benches
    - Now also used for E3000 SIMAIT (numerical satellite and EGSE simulation used to prepare AIT procedures) and SVF

Background

- SIMERC32 (ERC32 emulator)
  - Developed in 2001/2002
  - CNES/Astrium co-funding with shared IPR
  - Current users :

Program	Use case	User
Pléiades	SVF, SIMAIT, SIMEFM	Astrium Satellites
	Operations (BOSS & SINUS)	CNES
Galileo	SVF	Astrium Satellites
GAIA	SVF	Dutch-Space/Astrium Satellites
Bepi-Colombo	SVF	Astrium Satellites
Vega launcher	SVF	Astrium ST
Ariane5 new generation	SVF	Astrium ST
Airbus A350	SVF	EADS Airbus

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SIMLEON Development inputs

- Development started in 2006
- CNES/Astrium co-funding (extension of the SIMERC32 cooperation)
- Requirements are based on SIMERC32 specifications :
  - Overall timing accuracy should be better than 80% (today is better than 93%)
  - Addition of a “watch point” service
  - Addition of a cache mechanism (configurability : line/set number…)
  - Target platforms : Linux and Windows (x86)
- Reuse of interfaces/service definition from SIMERC32

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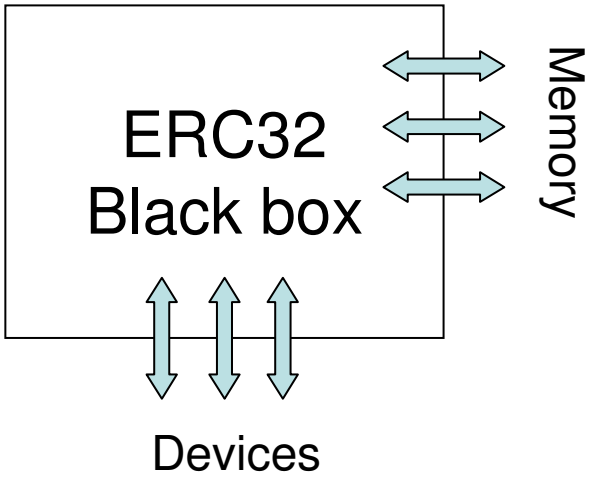
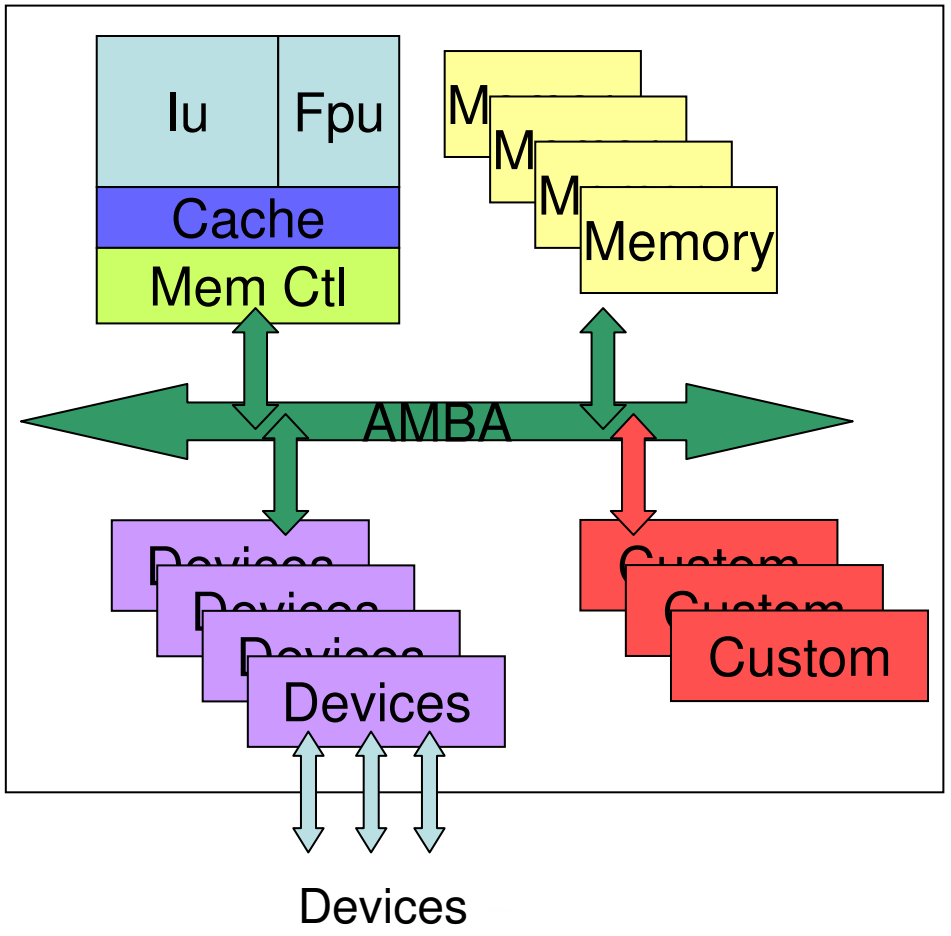
Leon VHDL flexibility

- Leon processor is delivered as open-source VHDL IP
  - Easy to change a component
  - Processor is no more a non-modifiable black box
  - Part of design/devices can be different
    - Memory controller can be changed to add automatic scrubbing :
      - Memory controller registers differ
      - Memory controller overall behavior differs
      - Other part of the design stay in place
  - Memory mapping is easy to change
  - Type of memory (SRAM, SDRAM…) is “easy” to change too
  - … easy to change everything by design !

ERC 32 VS Leon
System designer point of view





- ERC32 : internal bus not available
- LEON : internal bus available to plug extension (custom devices…)

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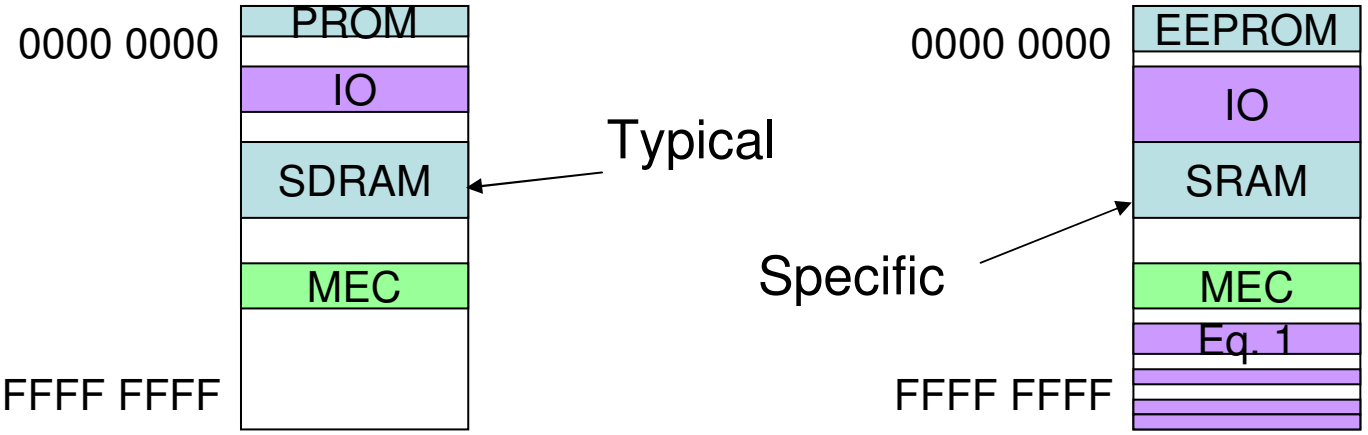
Development challenges (1/2)

- Emulator core was redesigned to take into account Leon2/3 flexible HW design
  - Core split in module
    - Configured via build system : fully configurable
    - Respect the same interface : exchangeable
  - Eg : memory controller :
    - Specify memory area parameters (size, timings, base address…)
    - Easily add another area at compile time



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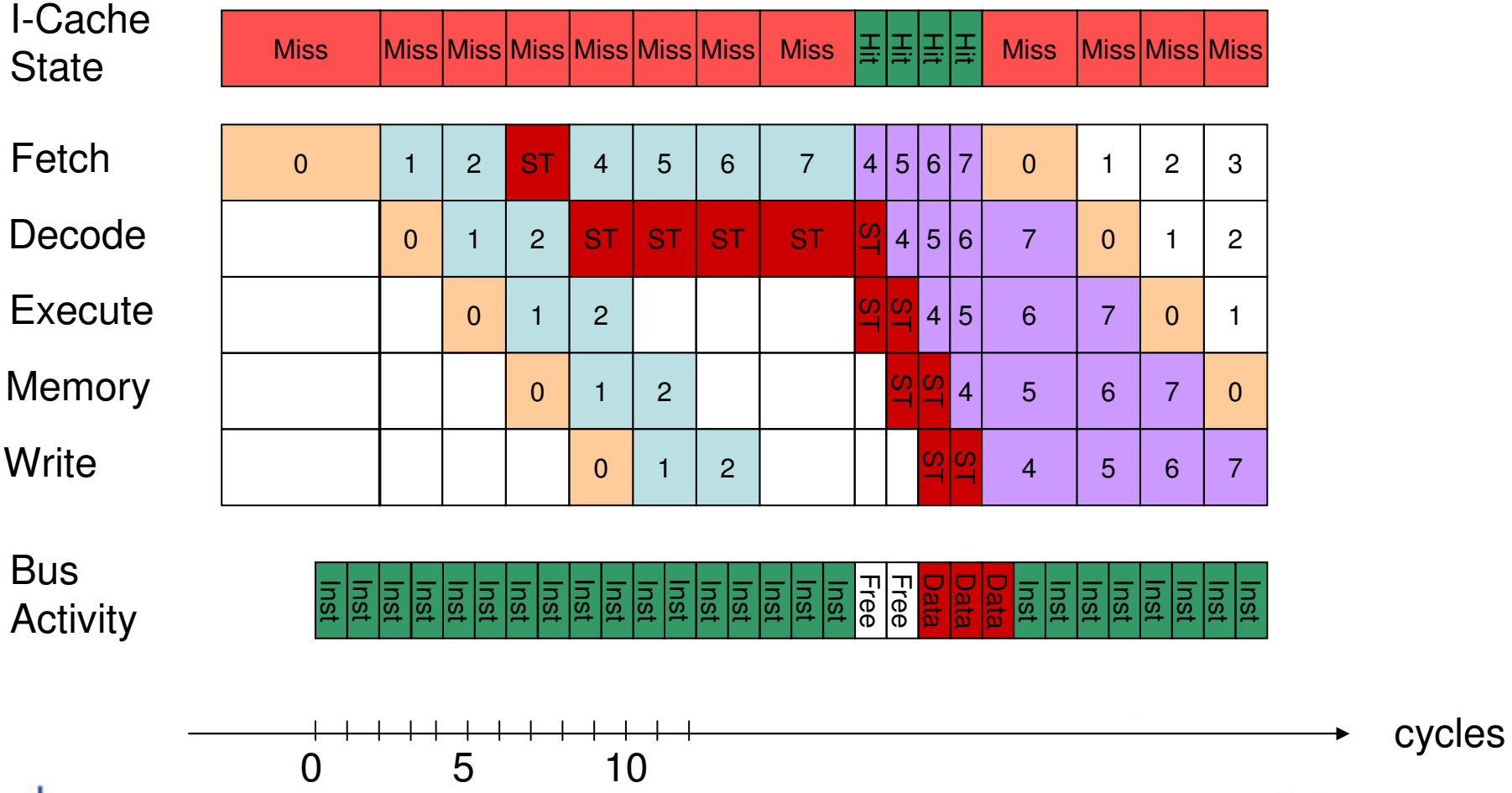
Development challenges (2/2)

- Timing computation



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Current status

- Validation performed by comparison with VHDL
  - Leon2 : ok
    - Processor 1.0.32-xst VHDL for LEON2
    - Validation report available
  - Leon3 : in progress
    - Processor 1.0.13 VHDL for LEON3
    - Validation report to be available at the end of the year
- Performance
  - Leon2 40 MHz, Stanford benchmark test :
    - With accurate timing (compliant with spec) : 51% of real time
    - With average timing (no cache, …) : 91% of real time

Current users

- AlphaSat payload
  - SVF delivered
- AstroSat250 (Astrium platform)
  - SVF delivered
  - SIMEFM (HITL with OBC numerical model) foreseen

Future Work
Performance improvement

- Current version is not yet optimised
  - Local optimisation : expected improvement up to 20%
- JIT for performances improvement
  - A dynamic binary translation has been prototyped
    - Acceleration factor is greater than 10

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Conclusion

- Operational and qualified product is available
- Accuracy requirement achieved
  - Already used for the new SVF benches
- Real time performance for operation simulator is met
  - Without cache and pipeline simulation, average timing
- Some performance improvement expected for HITL use case
  - And JIT prototype demonstrates huge acceleration factor
- By managing the Leon processor complexity and the incoming JIT acceleration factor we are confident for developing the next generation processor emulators

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