Real-time SpaceWire and PacketWire Interfaces as Developed for GAIA Verification

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INTRODUCTION

In the last decennium Dutch Space has designed and built several EGSE's to support the AIV of ATV, Herschel and Planck S/C's. Common to all the projects has been the need for hard real time performance of the FEE and SCOE's to enable the use in closed loop test configurations. The monitoring of on board discrete and bus connections without compromising the real time aspects of the signal can prove challenging. This holds in particular for the modern high speed on-board busses, based on LVDS signals.

The recent GAIA SCOE provided the opportunity to complete the development of 'non intrusive' test-means, which allows monitoring of SpaceWire and PacketWire traffic by looking at the voltage levels on the individual signals lines. The main objectives of the project were:

- To provide representative real time simulation of missing SpaceWire and PacketWire equipment towards the CDMU.
- Simulation and fully transparent monitoring of the on-board bus links, without added latency on time stamps or time tagged message generation.
- It should be possible to switch between monitoring a link and simulating a bus transceiver without HW reconfiguration.
- Integrated into the Dutch Space architecture to provide a unified solution for SpaceWire and PacketWire connections
- Cost effective and flexible for re-use in future projects

DUTCH SPACE STANDARD ARCHITECTURE

The standard Dutch Space SCOE HW architecture is shown in Fig. 1. This architecture is based on straightforward COTS interface cards, moving the more complex functionality towards the FEE and host SW with its inherent flexibility.

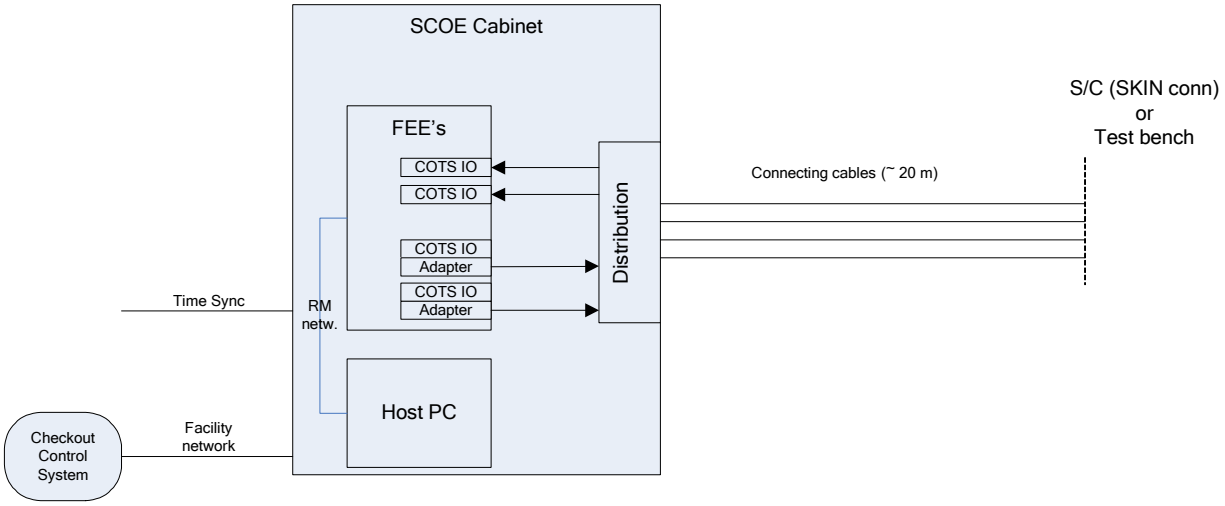

Fig. 1. DS Standard SCOE architecture

A standard multi processor PC hosts most of the high level programs like the Eurosim simulator, local MMI, FEE control, time synchronization and Central Checkout System interface. One or more 19" FEE subracks provide the S/C interfaces. If compliant with the S/C interfaces SCOE inputs can be directly connected to COTS interface modules. SCOE outputs are always routed over an 'Adapter Board' that protect the S/C. Dutch Space has developed a number of these Adapter Boards that cover most of the standard discrete S/C types like bi-level, analogue and pulse command signals. The host PC and the FEE's are connected over a real time Reflective Memory network. A distribution box rearranges signals between the COTS IO connectors and S/C SKIN connectors or connector bracket of a testbench. Simple project specific parts like dummy load resistors for RCS or heater simulation are also located in the distribution box.

SPACE AND PACKETWIRE EXTENTION OF THE STANDARD ARCHITECTURE

Both the SpaceWire and PacketWire share the same extension to our standard architecture as shown in Fig. 2.

Bus signals are acquired with small 'Active Interface Boxes' (AIB) which are placed between a bus cable and its unit (CDMU in the GAIA case) on the S/C or test bench. Because both the SpaceWire and the two PacketWire busses on GAIA are cross strapped between units, groups of four busses are operated in a mutually exclusive fashion. Therefore bus traffic can be multiplexed on a single simulation / monitoring connection to the SCOE by using a 'Multiplex Box' (MUX) which is located near the S/C or test bench. A COTS FPGA card provides the basic SpaceWire and PacketWire interfaces and the Adapter Board (AB) contains line drivers and (self) test means

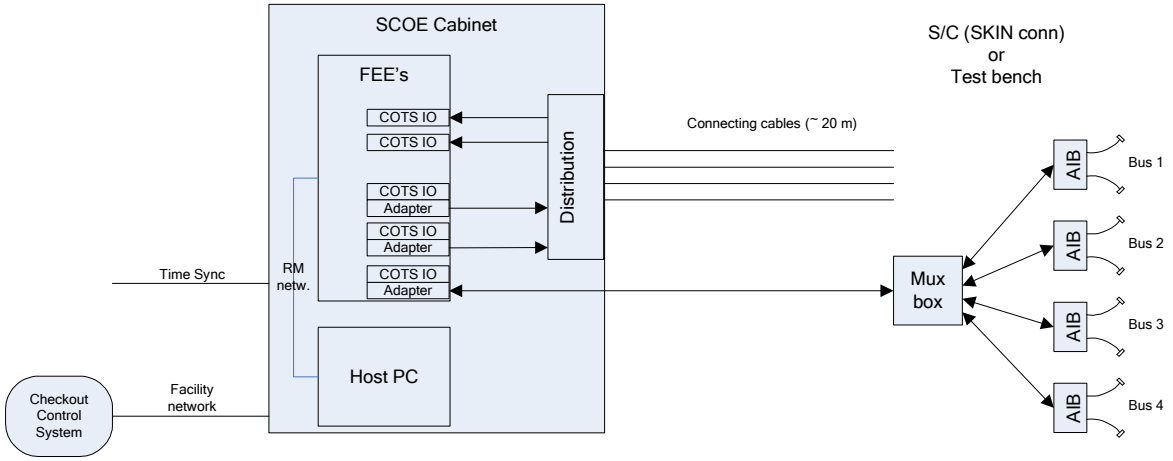

Fig. 2. Space and PacketWire extension topology

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PacketWire Details

Fig. 3 shows a schematic view of one of the PacketWire links to a MUX and four AIB's.

With the exception of the control signals, all connections between AIB, MUX and adapter board consist of the bipolar LVDS PWR_READY, PWR_VALID, PWR_DATA and PWR_CLOCK signal set defined in the PacketWire specification. Inside the AIB, MUX boxes and on the AB, low voltage logic signal levels are used to simplify switching.

The AIB has the following functions:

- Monitor the PacketWire traffic by looking at the voltage levels on the individual signal lines. Because the pickup point is at the CDMU side, this will monitor both onboard and simulated PacketWire traffic.
- Switch between a simulated or a 'real' PDHU PacketWire link. Normally the switch is commanded from the COTS FPGA card through the MUX box. However because the connections to the AIB and the MUX box are identical it is possible to monitor / control a single AIB directly from the AB.
- Since the AIB is connected to flight hardware, the power and ground should be isolated to avoid ground loops over the EGSE and a DCDC converter is included in the design. In addition an overvoltage protection on the supply voltage eliminates the risk of overvoltage on the PacketWire signal lines.

As shown in Fig. 3, the selection of which of the four PacketWire links is monitored or simulated is made in the MUX box. For the monitor channel, this selection can be automatic or controlled by the FPGA card. In autonomous mode it is based on the value of the four pw_valid signals from the AIB's, where the channel with the most recent asserted pw_valid is connected with the SCOE. The MUX box also has appropriate drivers and receivers for the 20 m. connecting cable to the SCOE.

The COTS IO card comes from Alpha Data and holds a Virtex II FPGA from Xilinx.

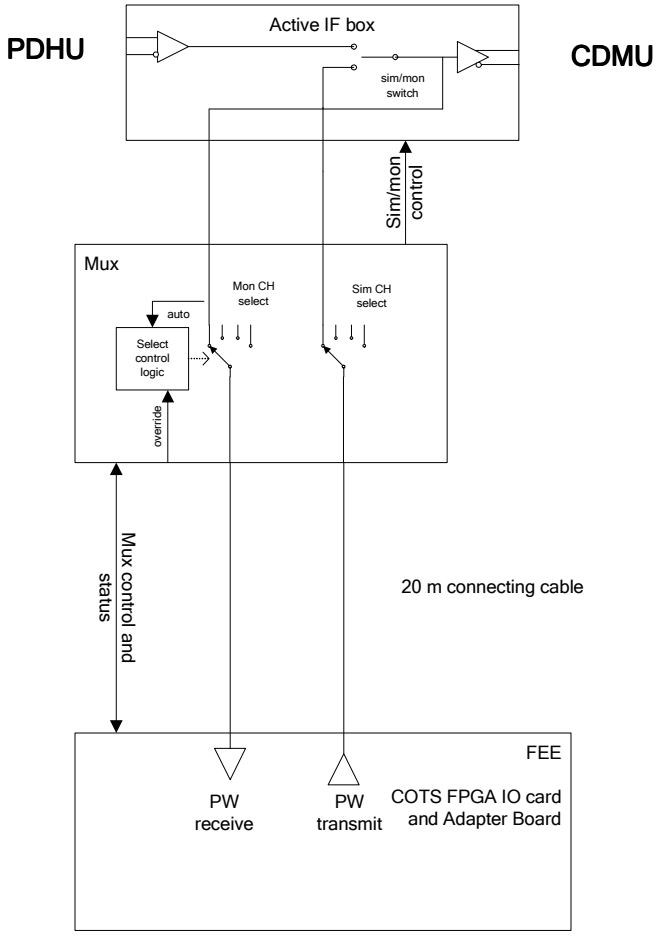

Fig. 3. PacketWire monitor / simulation chain

SpaceWire Details

The SpaceWire monitor / simulation chain is almost identical to the PacketWire as can be seen in Fig. 4. The bidirectional data and strobe pairs can be monitored by the receiver part of two SpaceWire channels or simulated by a third at the SCOE side. As with the PacketWire, the COTS IO card comes from Alpha Data but this time with a Virtex IV FPGA from Xilinx. Autonomous mode will select the link which has most recently driven their strobe or data signal.

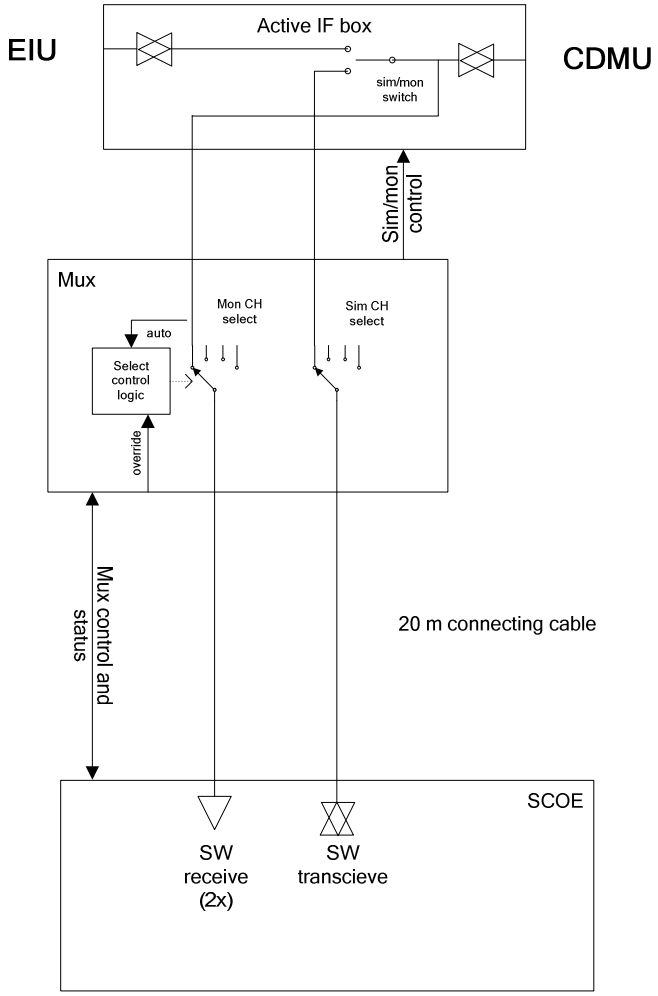

Fig. 4. SpaceWire monitor / simulation chain

The COTS FPGA card holds three SpaceWire channels, two for monitoring the bi-directional data and a third for simulating an EIU. FEE's can use these independent SpaceWire channels in a number of ways:

SpaceWire AB Operational Mode (Fig. 5)

In the Operational Mode, J1 is configured as full SpaceWire channel connected to the SPW-1 channel of the PMC module. The Adapter board also provides a driver for transmission over the 20 meter cable. J2 is used for monitoring of a full SpaceWire channel. The Din and Sin signals of this connector are routed to the receiver of SPW-2 channel on the PMC module. The Dout and Sout signals are routed to the receiver of SPW-3 channel on the PMC module.

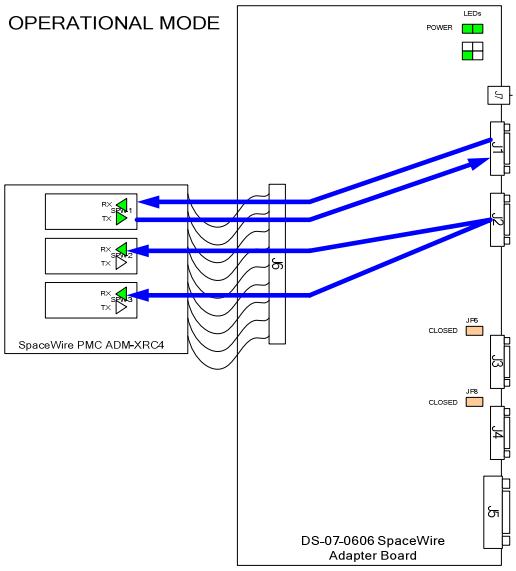

Fig. 5. SpaceWire AB operational mode

SpaceWire AB Port Test Mode (Fig. 6)

The purpose of this mode is to make the IO card more generic and provide 3 independent SpaceWire channels. In this mode, J1 is again configured as full SpaceWire channel connected to the SPW-1 channel of the PMC module. J3 is configured as a full SpaceWire channel connected to the SPW-2 channel of the PMC module. J4 is configured as a full SpaceWire channel connected to the SPW-3 channel of the PMC module. This mode is used to test the individual channels on the PMC module.

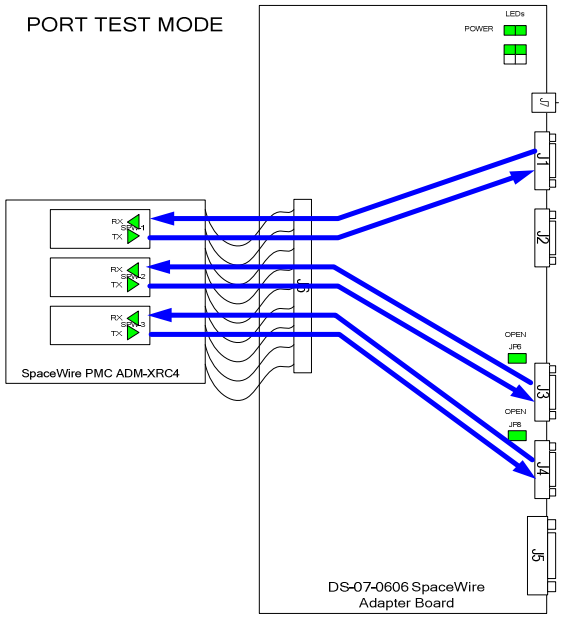

Fig. 6. SpaceWire AB port test mode

SpaceWire AB Monitoring Test Mode (Fig. 7)

The purpose of the Monitoring Test Mode is to provide an easy way of testing the COTS FPGA card with the AB as well as the related FEE SW. Only a standard SpaceWire cable and a loopback plug as shown in the figure are required.. J1 is again configured as full SpaceWire channel connected to the SPW-1 channel of the PMC module. J3 is routed through to J4. This loopback channel is monitored as follows: The Din and Sin signals of the J3 connector are routed to the receiver of SPW-2 channel on the PMC module. The Din and Sin signals of connector J4 are routed to the receiver of SPW-3 channel on the PMC module.

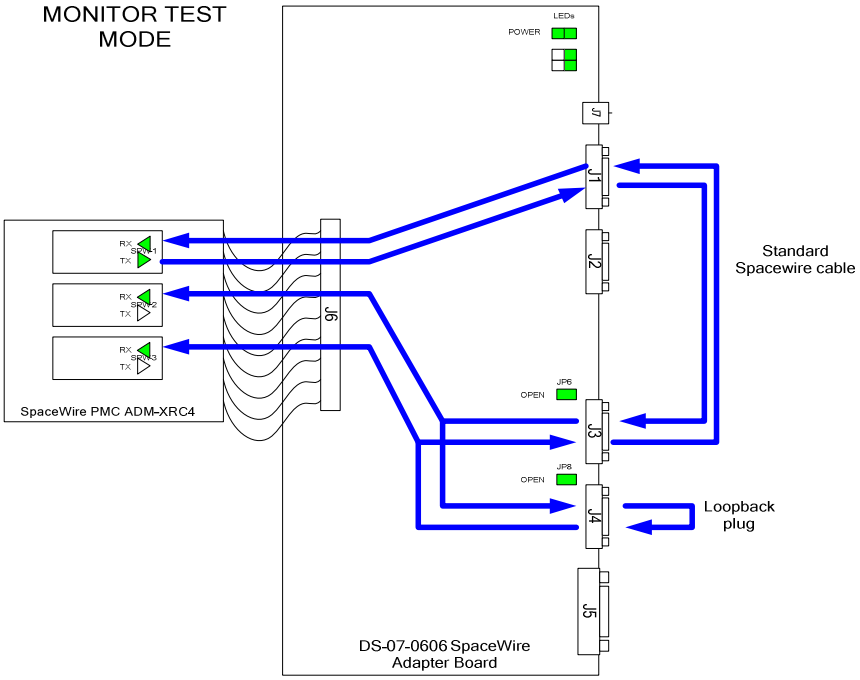

Fig. 7. Monitor test mode

HW TESTS RESULTS

The PacketWire and SpaceWire interfaces use the same driver and receiver IC's and therefore the signal characteristics measured with an oscilloscope on an opened PacketWire AIB at the end of the 20 meter connecting cable are a good characterization of the performance of both interface types. Fig. 8 shows reflections at 15 ns which are due to the mismatch of the MDM connectors and the impedance change at the soldering points of the flying leads onto the AIB PCB. The magnitude of these reflections however is within the limits of the SpaceWire specification.

The SpaceWire link has been operated up till 180 Mbps albeit with a connecting SpaceWire cable of only 2 m. Measured skew at the end of the 20 m connecting cable in the AIB however is sufficiently small (2.08 ns) to assume that the space and PacketWire links will operate up to the same limit with longer cables and the AIB / MUX boxes in the link

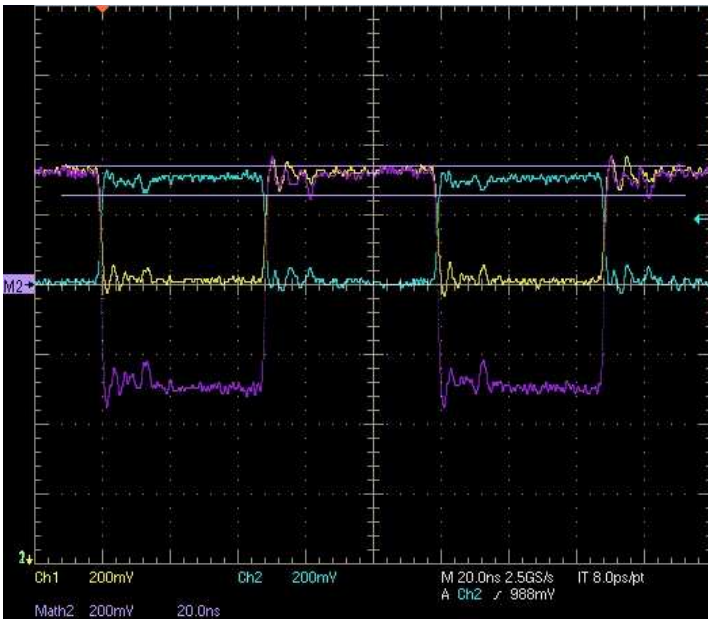

Fig. 8. PTW-MON-CLK signal at 20 m. (AIB)

CONCLUSIONS

Non intrusive real time PacketWire and SpaceWire monitor and simulation HW for EGSE's was developed that can operate up to 180 Mbps.

At the moment the system is used on a daily basis on the GAIA avionics test bench and will be used soon when integrating the GAIA S/C in Toulouse. Although refinements to the system are planned, the development of the S/C bus monitor and simulation HW has achieved all its basic goals.

A major benefit of the architecture is that SpaceWire links can be monitored without adding extra nodes to a SpaceWire network.

Acknowledgements

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