SENTINEL-3
SIMULATION CORE

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INTRODUCTION

The development of the Sentinel-3 Avionics and the Sentinel 3 **C**entral **S**oft**W**are (CSW) is mainly based on these three facilities:

- GNC **Hi**gh **Fi**delity Simulator (HiFi): is a pure numerical simulator facility primarily used for initial validation of the AOCS algorithms and supports the AOCS robustness/sensibility campaign. The HiFi is equivalent to a **F**unctional **E**ngineering **S**imulator (FES).
- **S**oftware **V**alidation **F**acility (SVF): is a pure numerical facility used for CSW verification and supporting the Functional Chain Validation dry runs. It permits execution, test and debugging of the CSW within a simulated on-board computer connected to a simulated spacecraft and space environment. The fidelity of the models included in the SVF is such that these models simulate all functions which are addressed by the CSW.
- **V**irtual-**EM** (VEM): is a hybrid test bench with hardware in the loop, then with a part of the avionics on table and where the missing units are simulated. The VEM is used for the HW/SW integration of the **O**n **B**oard **C**omputer (OBC) with CSW and the Avionics/System functional validation. The VEM is equivalent to a Spacecraft AIV Simulator.

<u>Which simulator architecture should we used to rationalize the development of these facilities ?</u>

To rationalize the development of the Sentinel 3 simulators, these facilities are based upon a common simulation core. This core, also called **R**eal **T**ime **S**imulator (RTS), is used along the lifecycle of the project and adapted in various configurations in relation to the targeted facility.

RTS needs only to encompass two kinds of categories of models:

- Satellite models: in charge to simulate avionics units, satellite dynamics and the space environment.
- Architecture models: in charge to manage the transverse functionalities of the simulators: times, synchronisations with the **S**ystem **U**nder **T**est (SUT) and with the test scenario, scheduling of the models, …

The same test procedures run on these facilities and provide data results. A mechanism has been implemented in order to match results (values and timestamps) from one facility to the other. This mechanism is called “data bus synchronisation”. The aim is to reproduce the same time synchronization mechanism on the VEM and on the SVF facilities.

SATELLITE MODELS

The set of satellite models, included in the simulation core (RTS), integrates all the user requirements in terms of scope, fidelity and performance.
The modeling of an avionics unit by a model, or a set of models, to the targeted facility is made according to a tunable scheme and a *layered architecture*. So, in fact, the modeling used, and reused, by these facilities is implemented (developed and tested) only once.

The *layered architecture* allows modeling equipment unit mechanisms using layers. The number of layers and their scope is the best compromises in view of the reuse objectives in the various facilities. The functionalities of an equipment unit are modeled as shown in Fig.1.

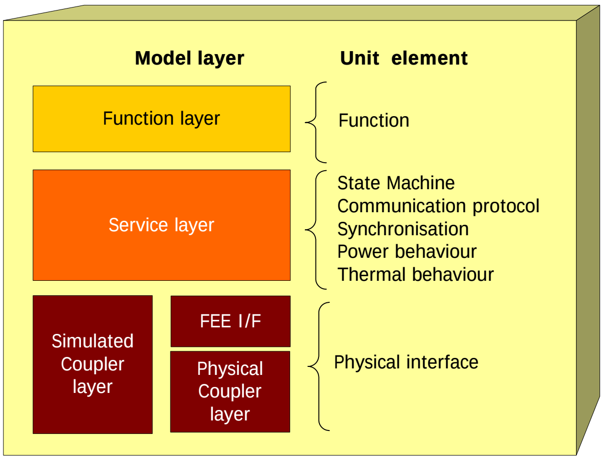

Fig. 1. Model Layered Organization

Legend:
FEE I/F: **F**ront **E**nd **E**quipment **I**nter**f**ace.

From this *layered architecture*, the simulation of one equipment unit becomes an assembly of layers in relation to the class of the targeted facility.

- A simulator focused on the functions of the equipment units embeds only the function layers.
- A numerical simulator representative of the dynamic behaviour of the equipment units embeds the following layers: function, service and simulated coupler.
- And a simulator exchanging data with real equipment units embeds the following layers: function, service, FFE I/F and the Physical coupler layer.

ARCHITECTURE MODELS

The set of architecture models, included in the simulation core (RTS), contains all the functionalities necessary to satellite models to be operated in the various classes of facilities. Some of architecture models are common to all targeted facilities and others are facility dependent.

The architecture models included in all facilities are:

- *Timing & Signal*. This model manages and dispatches clock signals coming from the SUT, manages the data need to fix the mission time. It also shifts data values collected during the simulation to the reference frame of the mission date.
- *RTS Manager*. This model schedules the satellite models according to the basic simulation clock coming from Timing & Signal model.
- *Simulation Mode Manager*. This model produces outputs of models, belonging to the function layer, in accordance with the simulation loop mode engaged on sub-systems (opened, closed, or tabulated).

The models depending on the targeting facility are:

- *VEM Master*. This model is only present in the VEM facility. It is in charge to catch the synchronization signals and events from the HW couplers of the VEM bench (VEM couplers). The mechanism dedicated to exchange these data with the VEM couplers is based on a common library. This library provides services to read, to write data and to raise interruptions through a reflective memory.
- *VEM I/F models or FEE I/F models*. These models are in charge of exchanging avionic engineering data between the VEM couplers and the service layers.

See below a scheme about how RTS interfaces with the VEM couplers.

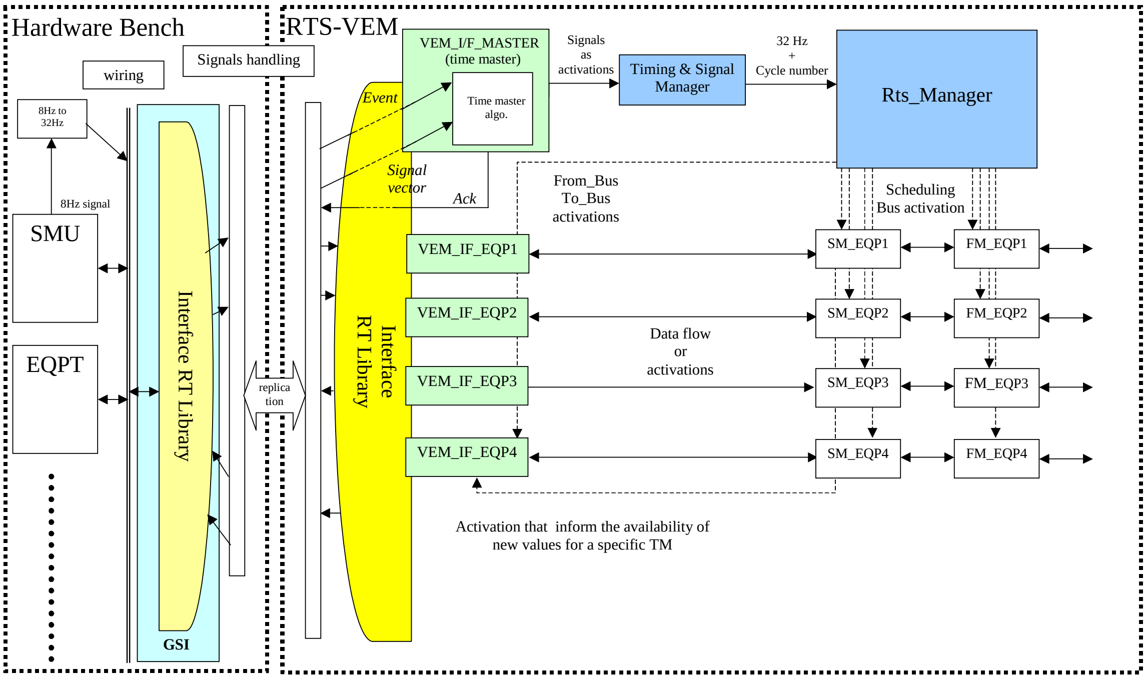

Fig. 2. RTS-VEM interface block diagram

This scheme also shows the functional chain made by the architecture models. For each facility, this chain always works the same way. The Timing & Signal model received signals and events from the SUT and then dispatches these data to the RTS Manager and the Simulation Mode Manager models. Once these information received, the RTS Manager schedules the satellite models according to a strict mechanism called "data bus synchronization".

DATA BUS SYNCHRONISATION MECHANISM

The data bus synchronization mechanism has been implemented in order to use the same time synchronization for data exchange on all facilities.

This mechanism relies on three signals. These signals are delivered by the RTS Manager model, whatever the facility is.

- The "From Bus" signal is used to read data from the On Board Computer or from the shared memory.
- The basic simulation clock signal is the atomic signal used to schedule all the avionic models according to a scheduling table (32Hz on Sentinel 3 simulator).
- The "To Bus" signal is used to transfer data to the On Board Computer or to the shared memory.

The goal of this mechanism is to have the same process of time synchronization, for all the facilities. So an execution of the same procedure produces the same time stamped results, on each facility.

See below a scheme about how this mechanism runs on the SVF and on the VEM facilities.

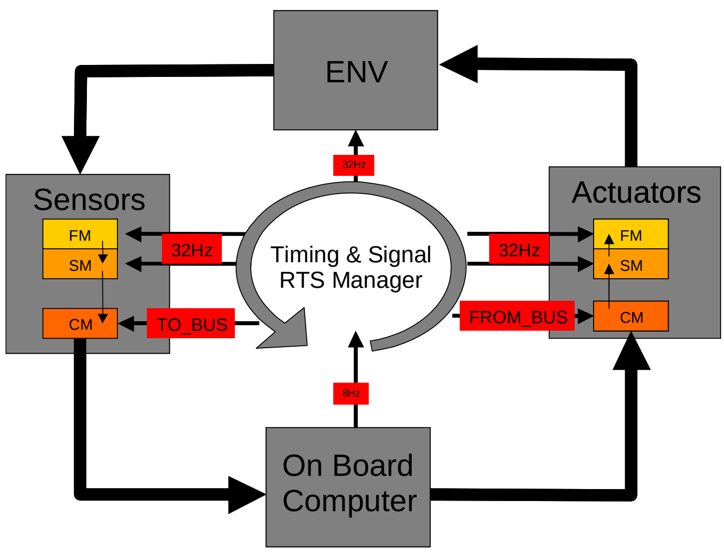

Fig. 3. Data bus synchronisation on the SVF facility.

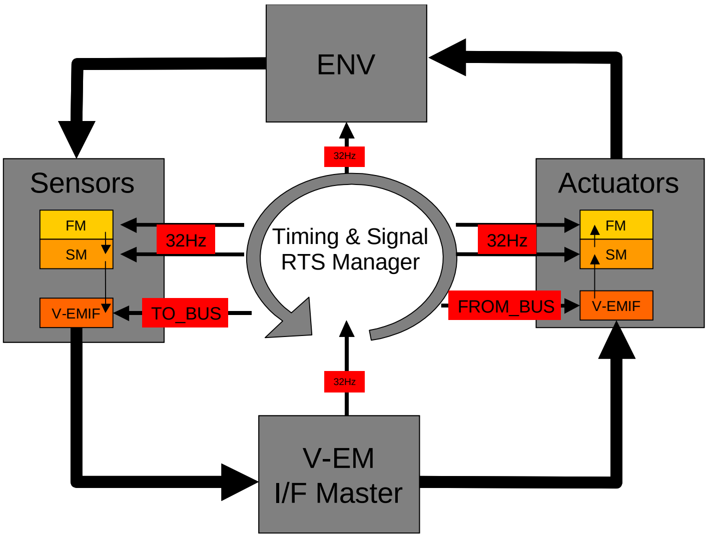

Fig. 4. Data bus synchronisation on the VEM facility.

Legend:
- FM: Functional Model layer
- SM: Service Model layer.
- CM: simulated layer of the Coupler Models.
- VEMIF: VEM I/F models or FEE I/F models

On the SVF, the Timing & Signal model is in charge of converting the clock signal received from the On Board Computer (8 Hz on Sentinel 3) to the basic simulation clock (32 Hz on Sentinel 3) with tick numbers. In the case of the VEM, the Timing & Signal model receives the basic simulation clock from the Virtual Bench (the HW couplers). So both the SVF as the VEM, the Timing & Signal model provides the basic simulation clock with a tick number to the RTS Manager.
Whatever the facility, the RTS manager schedules the satellite model with the same clock signals as inputs. No others treatments are made, depending on the facility, for scheduling the satellite models.

Thanks to the same mechanism used to time stamp data exchanged with the SUT, it is easy to analyze and compare results between facilities. Once this comparison done, each facility is now reliable to run test procedures.

RTS ON THE SVF AND VEM FACILITIES FOR SENTINEL 3

The two schemes below detail the design of the two main Sentinel 3 facilities: SVF and VEM. These designs are based upon the same simulation core encompassing the layered architecture, the architecture models and the data bus synchronization mechanism.

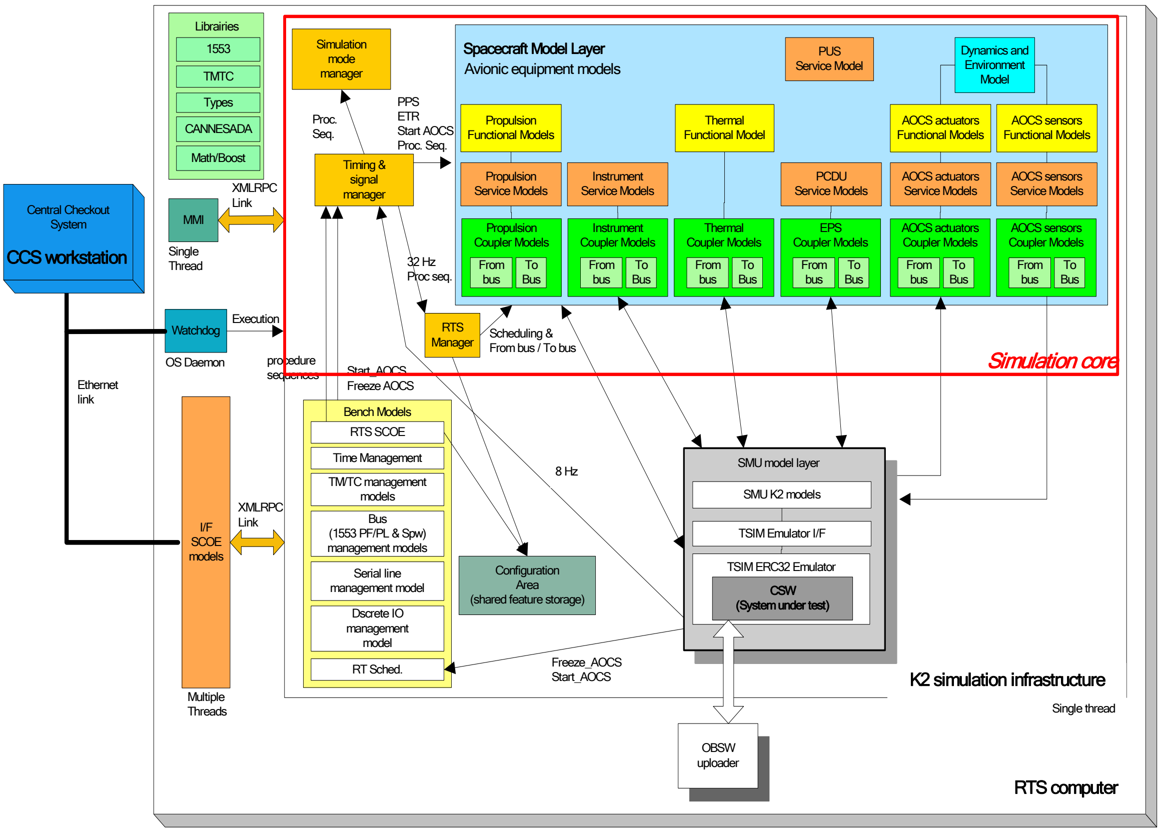

Fig. 5. Design of the SVF facility.

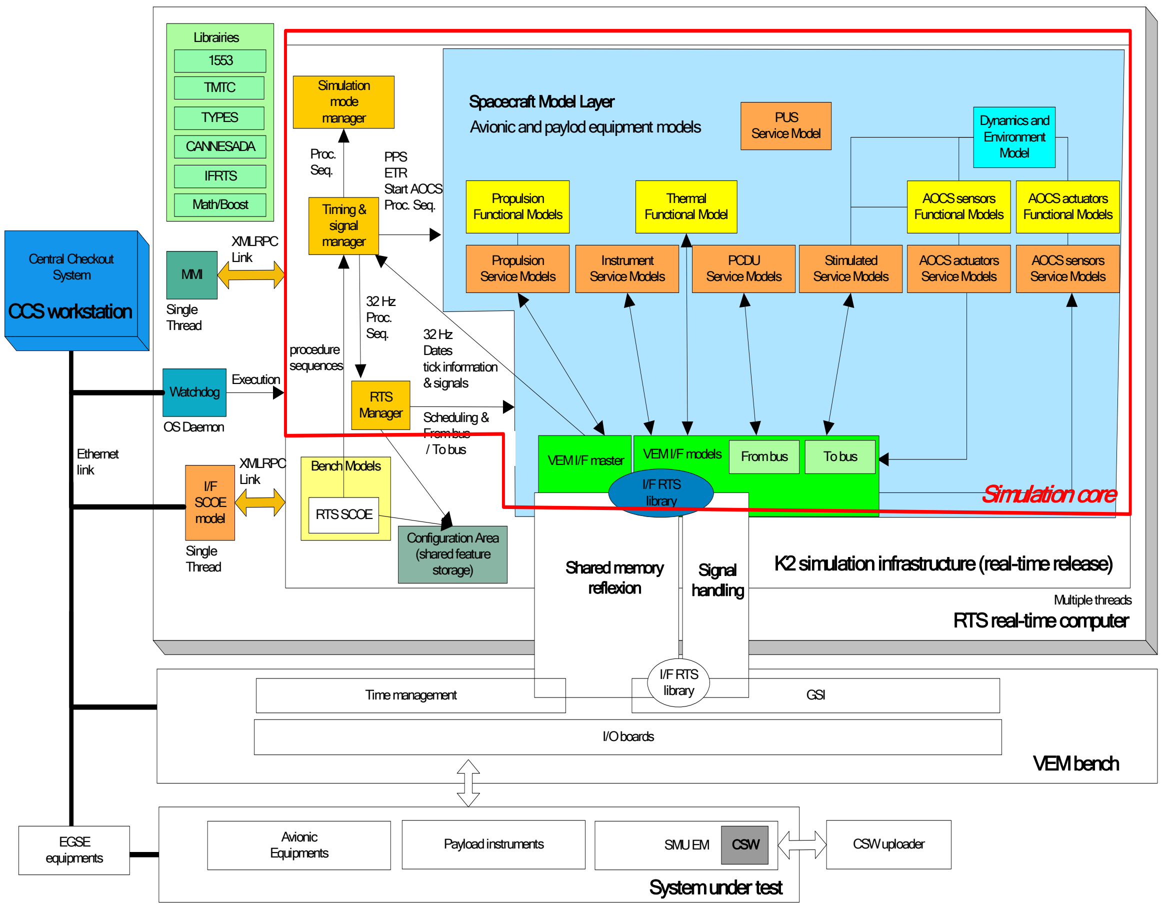

Fig. 6. Design of the VEM facility

Legend:

SMU : **S**atellite **M**anagement **U**nit → the **O**n **B**oard **C**omputer.

K2: The simulation infrastructure.

The satellite models have been grouped in a layer called the Spacecraft model layer.

All the technical choices, explained in this paper and implemented in the simulation core are possible only because our simulation infrastructure, K2, is developed in the aim to support real time runs. All K2's code lines are optimized, and K2 provides services and tools to develop and test satellite and architecture models in both real time and non real time environments.

CONCLUSION

The simulation core is the answer to rationalize the development of simulation facilities. It maximizes the reuse of models and also includes to a common mechanism of time synchronization for time stamping data exchange.

On Sentinel 3, thanks to the simulation core, it has been possible to develop the two main facilities (SVF and VEM) in the same times. Therefore, once a new simulation core is available, the process of simulator development allows to validate and to deliver these two facilities almost at the same time. Based on the same RTS computer with K2, our simulation infrastructure, no cross-compilation is now necessary.

At the present stage of the Sentinel 3 simulator developments, the open loop releases of the SVF and VEM facilities have already been delivered. The next and final deliveries, the closed loop issues, are foreseen for the middle of November.