SESP 2010

Session:	Session: Processor Emulators (13)
Type:	Concurrent Session
Date:	Wednesday, September 29, 2010
Time:	14:00 - 15:00
Room:	Newton
Chair:	
Co-chair:	
Remarks:	

Seq	Time	Title	Abs No
1	14:00	JIT Technology for SimLEON - Numerical Emulation of LEON2/LEON3 Processors Meurant, Olivier EADS Astrium GmbH, FRANCE Operation simulator require at least real-time simulation, and benches involving hardware-in-the-loop need even more performances for I/O. Users of numerical simulation always call for faster simulator as it helps validation campaigns and operations preparation. Classic emulators consume a lot of CPU power but with old generations of processors this type of software were able to deliver acceptable performances due to the low computing powers of the emulated processors. With LEON processors, featuring a cache system, a 7-stage pipeline and able to be clocked up to 200MHz, a step in emulation technology is mandatory to follow performances needs. However this step must not degrade neither the full set of functionalities currently offered or its fidelity. The development of a new generation of emulators based on binary translation (ie JIT compiler) already began in EADS Astrium and shows promising results. This paper will present technology choices and current results of the development.	
2	14:30	Performance Improvements in the ESOC Emulator Marchesi, Jose E. Terma GmbH, GERMANY While the ESOC Emulator is the best performant ERC32 emulator currently available, we can identify at least three reasons why performance improvements would be of benefit to ESOC. First, current and future missions at ESOC are requiring higher and more demanding Emulation power in terms of more powerful processors, and more processors, to emulate i.e. Constellation simulators. Second, there is an increasing demand in operational simulators to emulate more software running on processors rather than writing functional models, for example Mass Memory and Payload sub systems, as well as parallel emulation of AOCS and Basic OBSW. Third, a Leon emulator could be based in the current ESOC Emulator, expanding the current codebase to cover the SPARC v8 instruction set. In an effort to increase the performance of the Emulator Terma GmbH made a full relocation of the Emulator to a real 64-bit RISC hardware platform - SPARC v9. This makes it possible to generate emulator cores directly in assembly code instead of C. The ESOC emulator was originally written in Alpha assembly for performance issues and was later relocated to C. In that process we identified other improving opportunities, like the reduction	

of the codebase by using Ada 95/2005 facilities such as tagged types. This paper shows the performance improvements currently obtained and possible further improvements that could be possible in the future.