Essential Telemetry (ETM) Support ASIC

Final Presentation

ESTEC, December 9, 2015

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Objectives

Background for this development

Essential Telemetry Acquisition

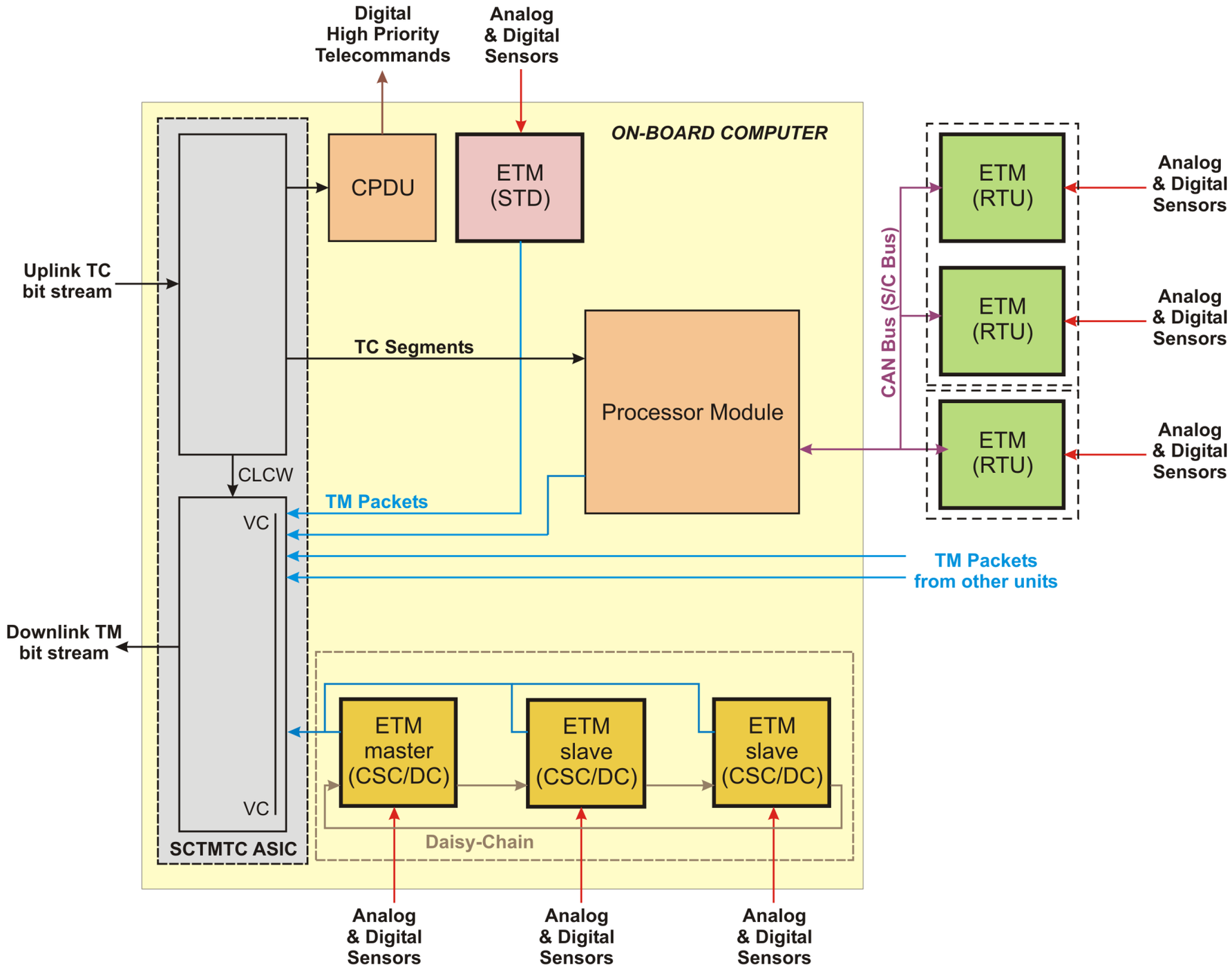
- Essential Telecommands are decoded by H/W with minimum electronics Involved
- Correspondingly, ETM allows to autonomously acquire and format essential telemetry (analog and digital) for direct transmission to ground

Remote Terminal Unit

- By inclusion of a suitable bus interface in the ETM it becomes a compact autonomous remote terminal interface unit.
- Spacecraft mass and power can be reduced

Objectives

ETM Applications in a Spacecraft



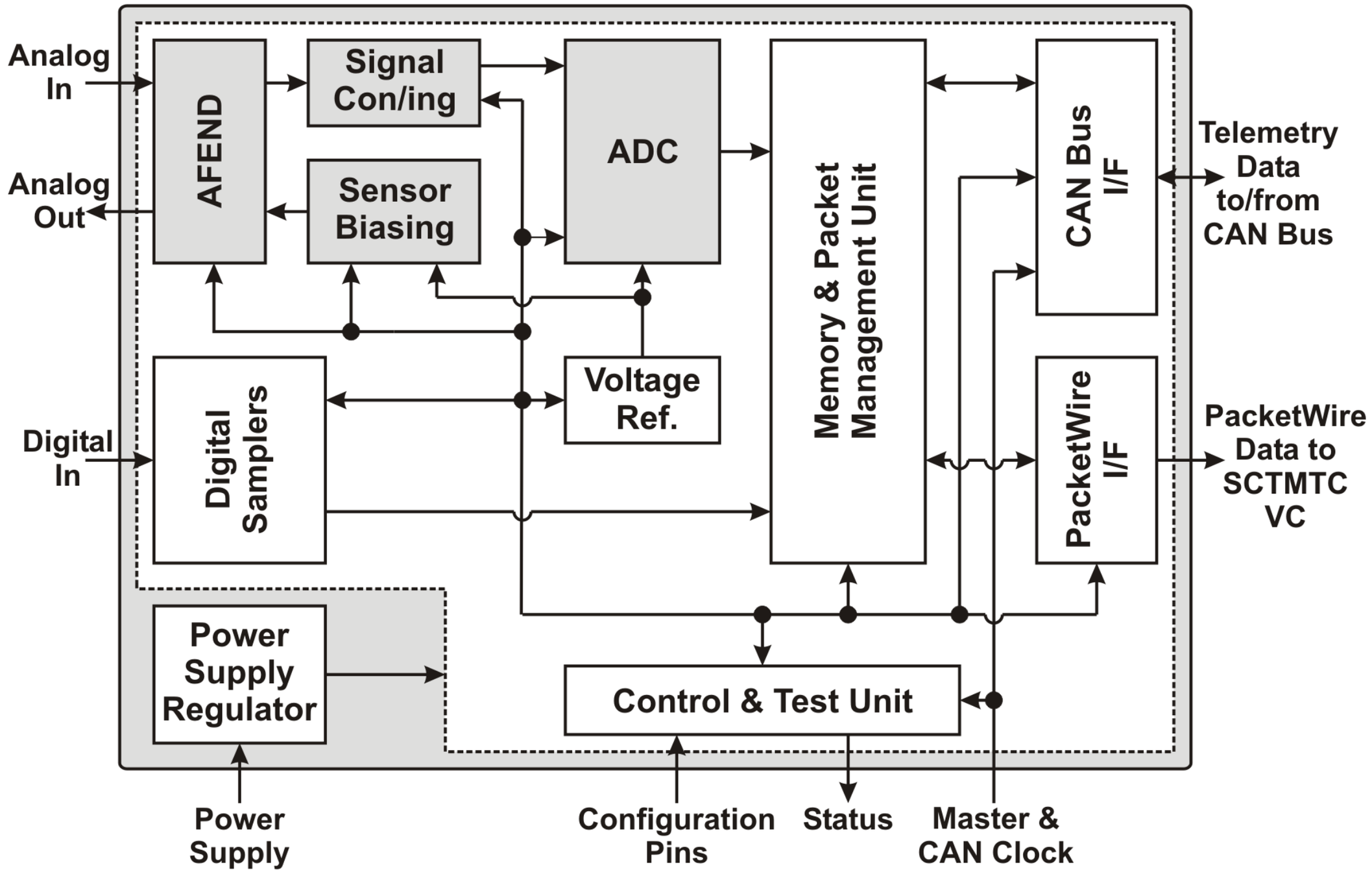
ETM Overview

Functionality

- Sequential scanning and sampling of discrete analog (voltage or temperature) & digital inputs.
- Convert the analog inputs to digital values.
- Format the sampled data into space packets.
- Sampling time reference can be included in packet (optional).
- Output the sampled formatted data either through CAN or PacketWire IF.

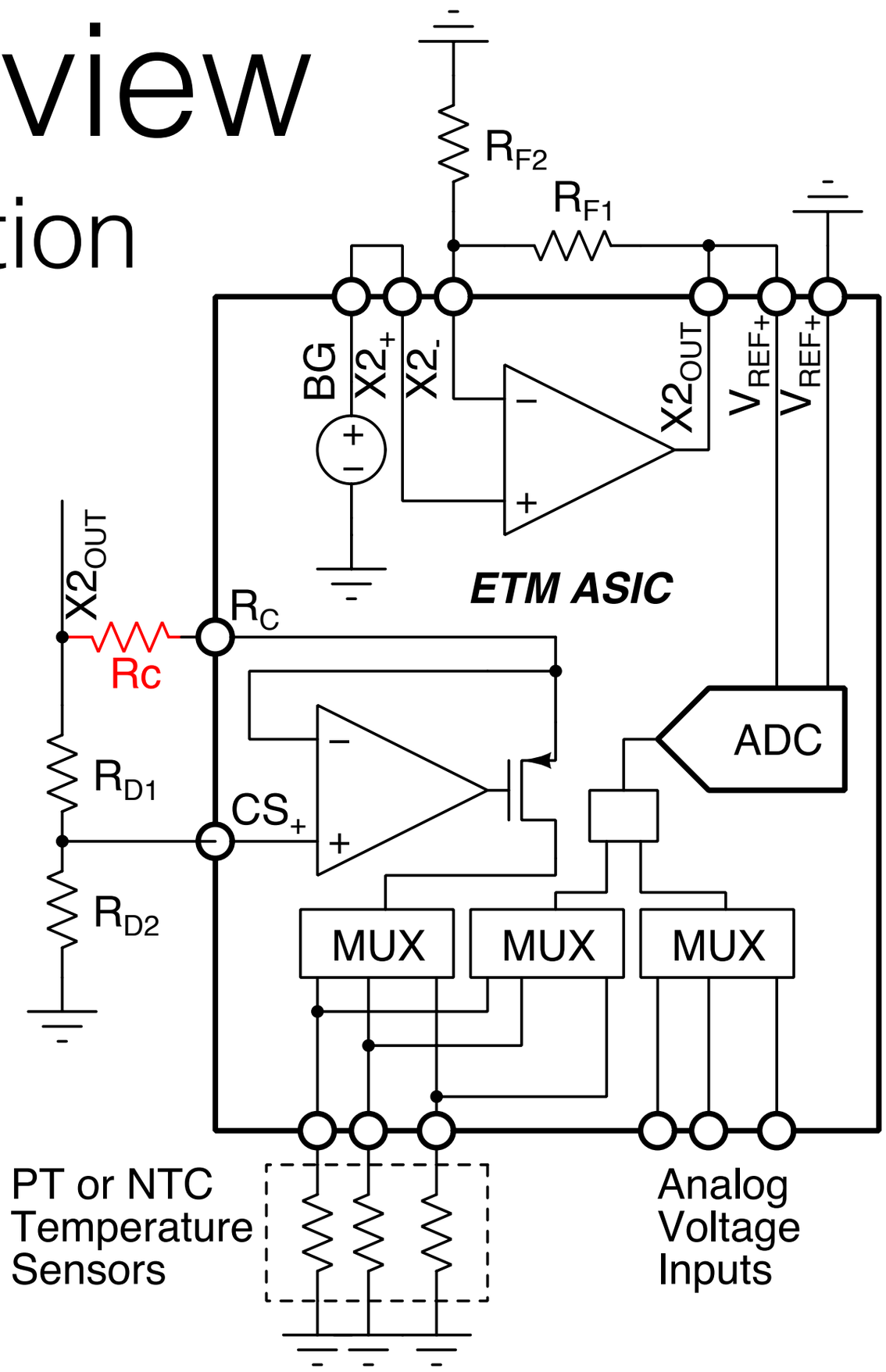
ETM Overview

ETM Block Diagram



ETM Overview

Analog Section



ETM Overview
Operating modes

- Number of analog sampled channels: 4, 8, 16, 32
  - Grouped in 4 groups
  - Each group can be independently configured as voltage, or temperature measurement
- Number of digital sampled channels: 16
- Sampling period: 2 ms to 50 sec
- Ability to release packet on a change of digital inputs or every 65536 sampling periods

Activities
Overview

- Engineering Model (EM) Design, Verification & Fabrication
- EM Testing
- Flight Model (FM) design upgrade and Fabrication
- FM Testing
- FM Lot Acceptance Testing

Activities

EM Design / Performance Objectives

- Targets were
  - 300 KRad TID hardness
  - Single event latch up (SEL) threshold: 67 MeV.cm^2/mg
  - Single event functional Interrupt (SEFI) threshold (SEL): 67 MeV.cm^2/mg
  - Single Event Upset (SEU) threshold: 50 MeV.cm^2/mg
  - Power Consumption: 100 mW
  - Code histogram Centered value ±1 LSB regardless of the interface.

Activities

EM Design / Design Flow

- Design Methodology chosen was full custom layout for both analog and digital units

- The use of the above methodology resulted in low power consumption and very good radiation hardness

- Verification of the design was covered through:

  - Detailed timing analysis and characterization of the cells produced at block level

  - System level spice simulations with varying clock frequencies (margins were set to above x2)

  - Development of an FPGA with all the digital part of the ASIC

Activities
EM Fabrication

- Prototype was fabricated in the IHP SiGe 0.25 um process.
- Only CMOS transistors were used
- Packaged in
  - CQFP 256 package
  - PGA 256 package for TID and SEE tests

Activities
EM Test

- Functional and temperature tests
- TID test at ESTEC
- Californium Test at ESTEC
- SEE Test at UCL/HIF
- Compatibility tests with SCTMTC ASIC

Activities

EM Functional and Temperature Tests

- Stuck at Fault and IDDQ tests were performed to verify the correct layout of the device and assess yield in the digital section

- Performance tests were performed to assess the analog section. Tests were performed at -55, 25 and 125 degC and for power supplies of 2.97, 3.3 and 3.63 V.

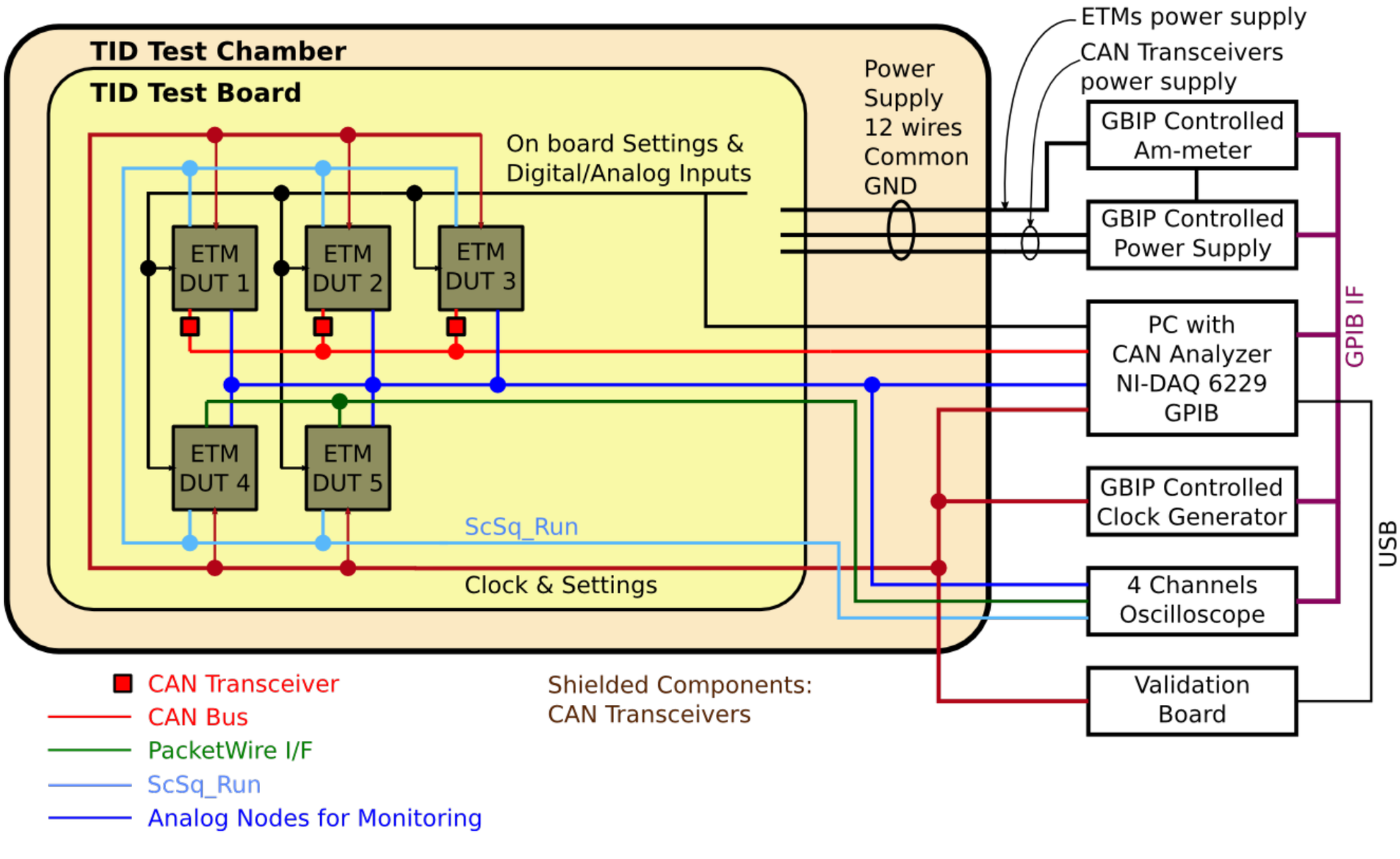
- Special tests were performed with varying clock frequency and temperature.

Activities
EM Test Key Results

- Passed functional tests
- TID hardness of more than 1 MRad
  - Use of digital auto zeroing for TID levels of 300 KRad and above
- SEL and SEFI free up to 67 MeV.cm^2/mg
- SEU $LET_{THRESHOLD}$ = between 32 and 40 MeV.cm^2/mg
- I_{VDD} = 3-4 mA @ 3.3V
- Low induced digital noise in the analog section

Activities

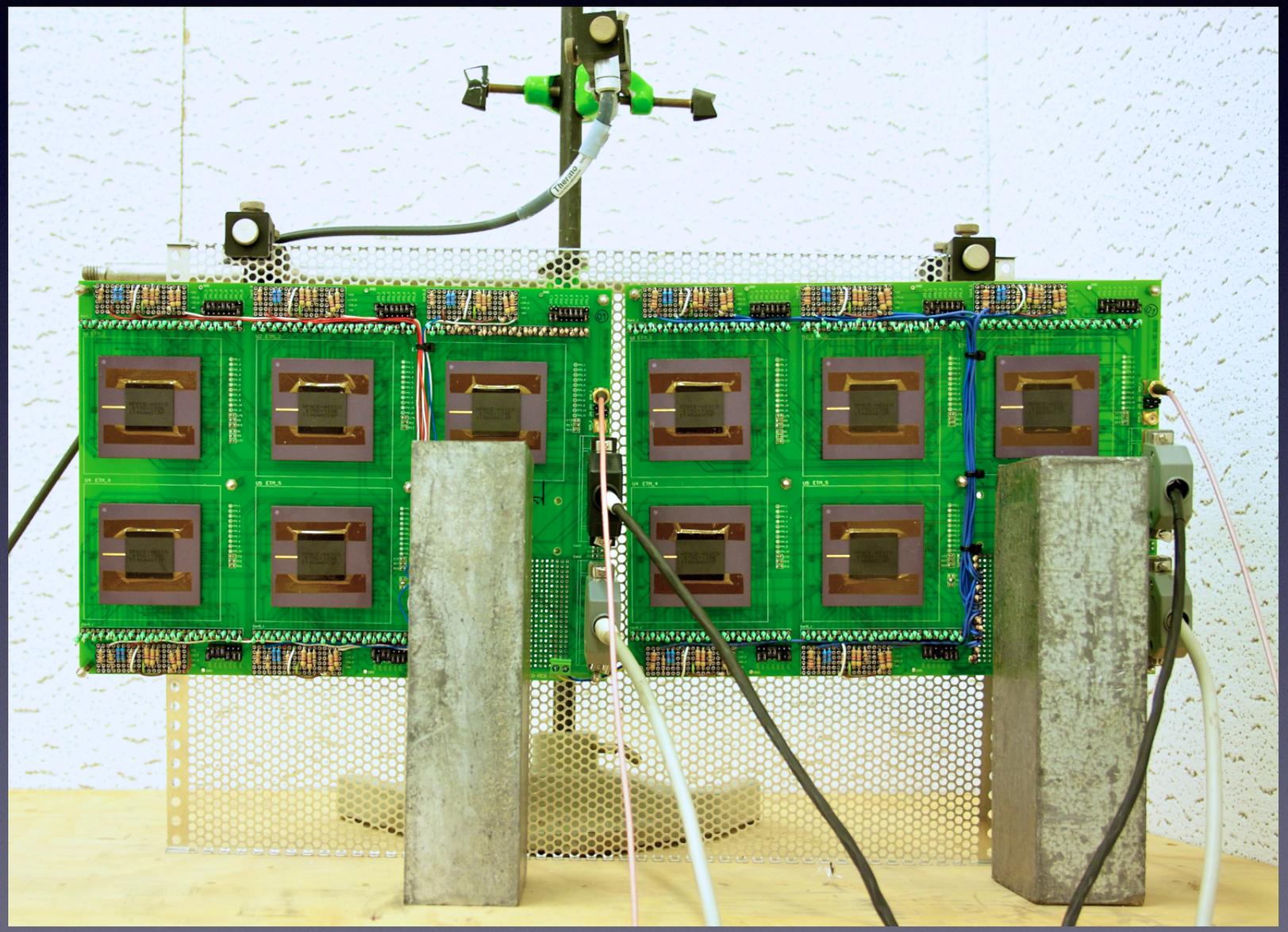
EM TID Test



Activities

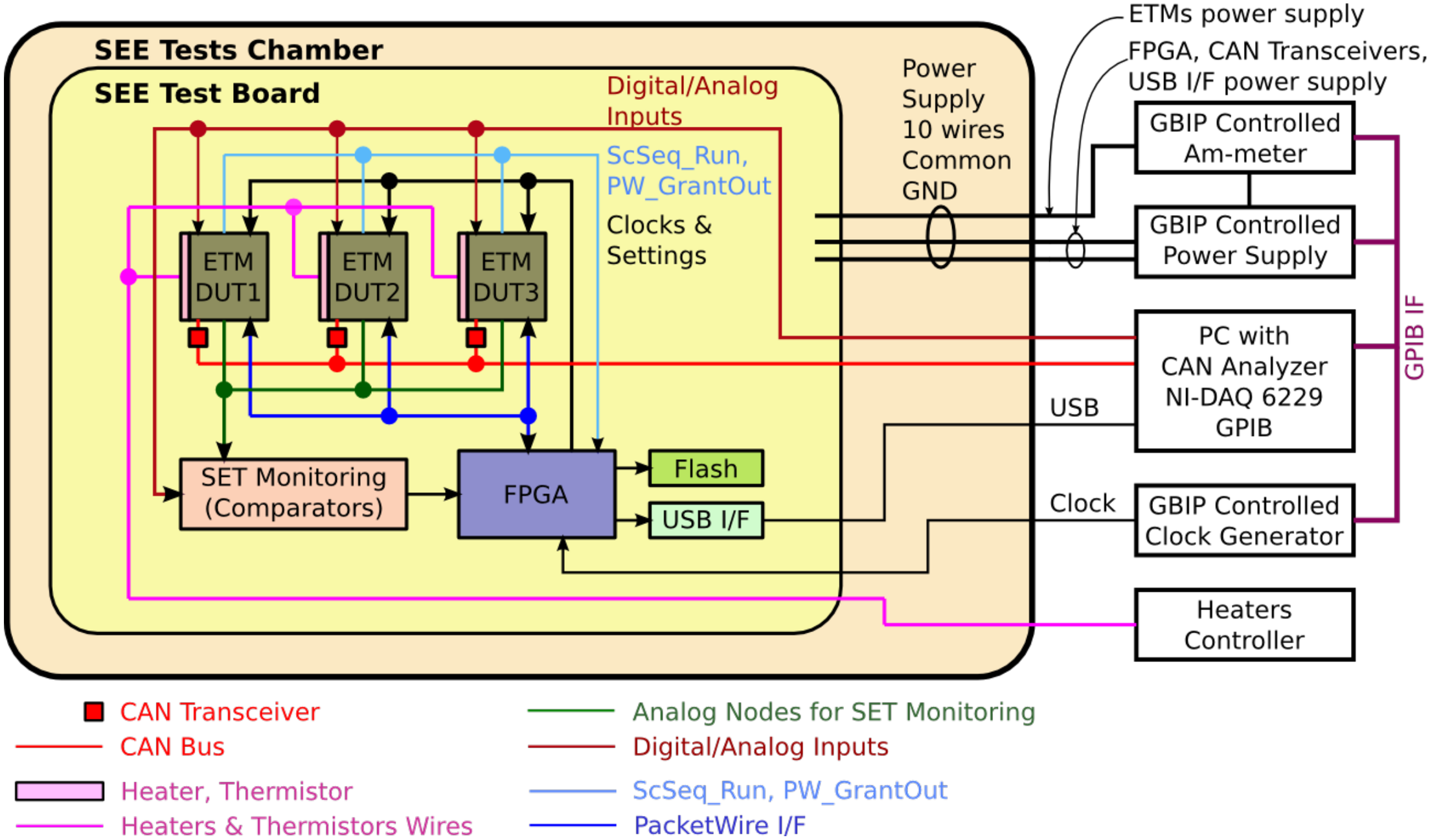
EM TID Test

- TID Test Setup for 10 ETM devices
- Sensitive support electronics were protected with lead brick



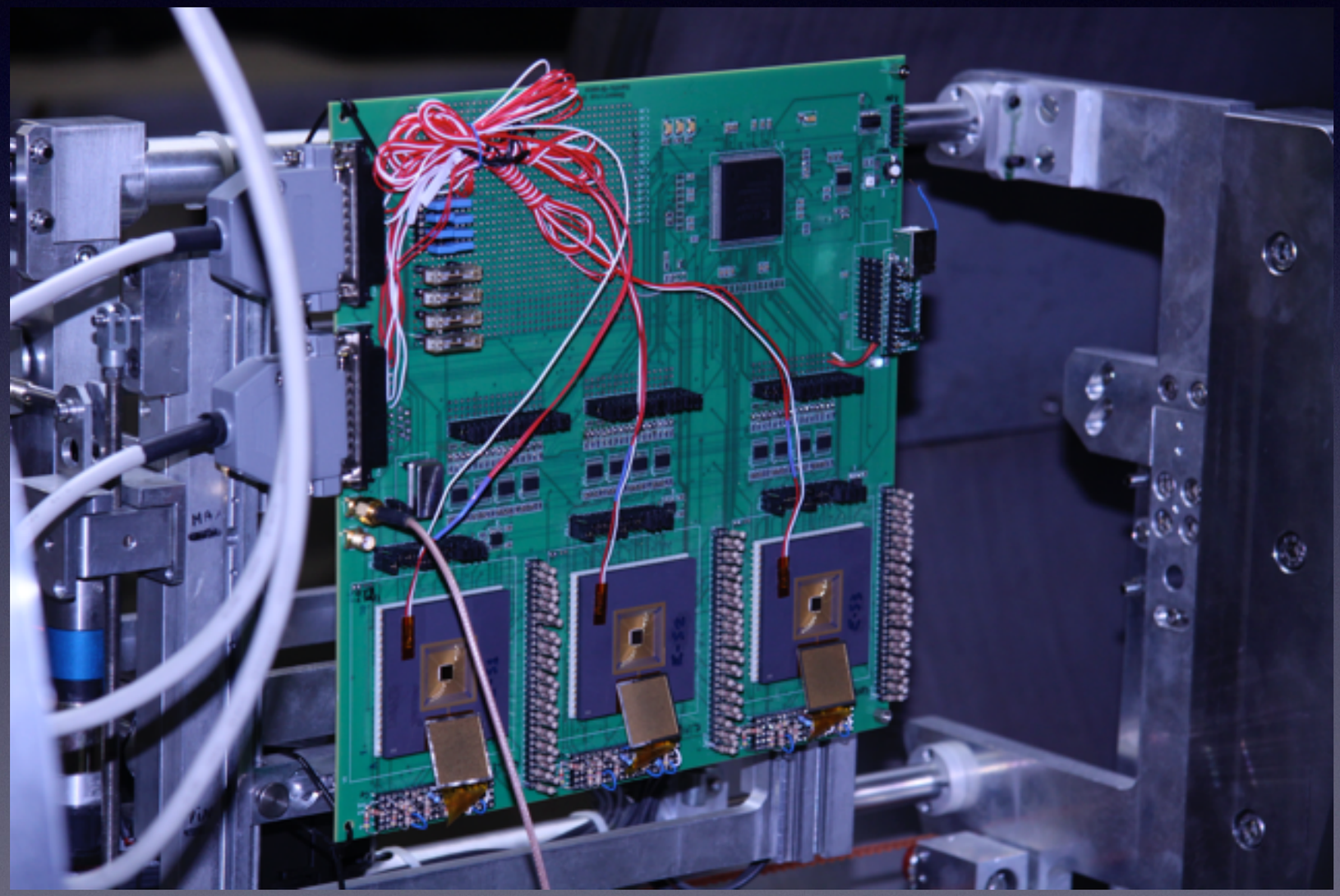
Activities

EM SEE Test



Activities
EM SEE Test

- SEE Test Setup for 3 ETM devices
- Implementation of FPGA for SEU and SET data acquisition
- High speed comparators for SETs in the analog domain



Activities
FM Design Upgrade

- Minimum modifications were required
- FM devices were fabricated in an MPW run from IHP
- ~ 300 devices were made available to SPACE-ASICS
- Devices packaged in
  - 256 CQFP package and 256 PGA package for TID and SEE tests
- Testing included:
  - SAF, IDDQ, Functional and Temperature Tests
  - TID and SEE Radiation tests

FM Lot Acceptance

Activity Flow

Establishment of Qualification Plan based on ESCC 9000

Re-design of test procedures to run with multiple devices

Test H/W Development

Production Control

Lot Acceptance

Screening Tests

Lot Functional Validation

Burn In

High/Low Temperature and Ambient test

Endurance Tests

Mechanical Tests

Environmental Tests

Assembly Capability Tests

SA Activity

HCM Activity

ALTER Activity

FM Lot Acceptance
Challenges

- SPACE ASICS had to develop the capability to manage and implement the lot acceptance test program
- A large variety test boards needed to be developed so as to accommodate testing of the device at various environments
- A lot of electrical tests were performed in house to stay with the available budget

Accomplishments

- A low power, rad hard, mixed signal Analog Digital all European ASIC has been designed and fabricated.
- Lot acceptance tests have been performed as per ESCC 9000 and ~100 components are available on stock
- SPACE-ASICS has developed the capability to provide more ETM devices if needed
- Experience was acquired for end to end development of mixed signal ASICS for space applications

ETM-RTU

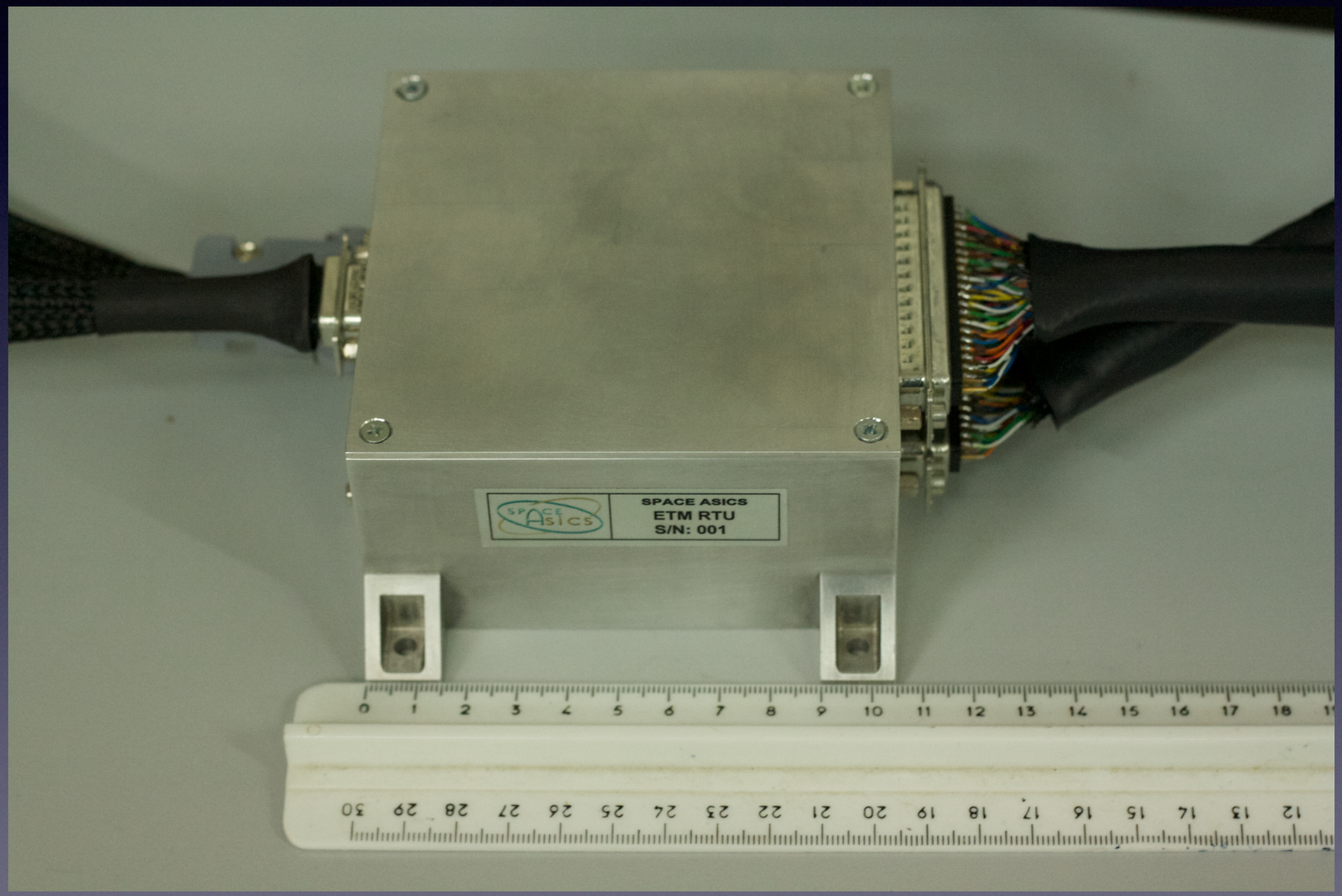
- A miniaturized telemetry acquisition unit based on the ETM ASIC has been designed, manufactured and tested by SPACE-ASICS
- ETM RTU could be suitable for applications on mini satellites.

Steps of the Activity

ETM-RTU

- Box Contains:
  - 1 ETM ASIC
  - CAN Transceiver
  - RS 422 transmitter and receiver
  - Crystal oscillator
  - Power Regulator
  - Connectors for the measurement channels and timing information
- Commercial components have been used with the same footprint as flight qualified equivalents.

ETM-RTU

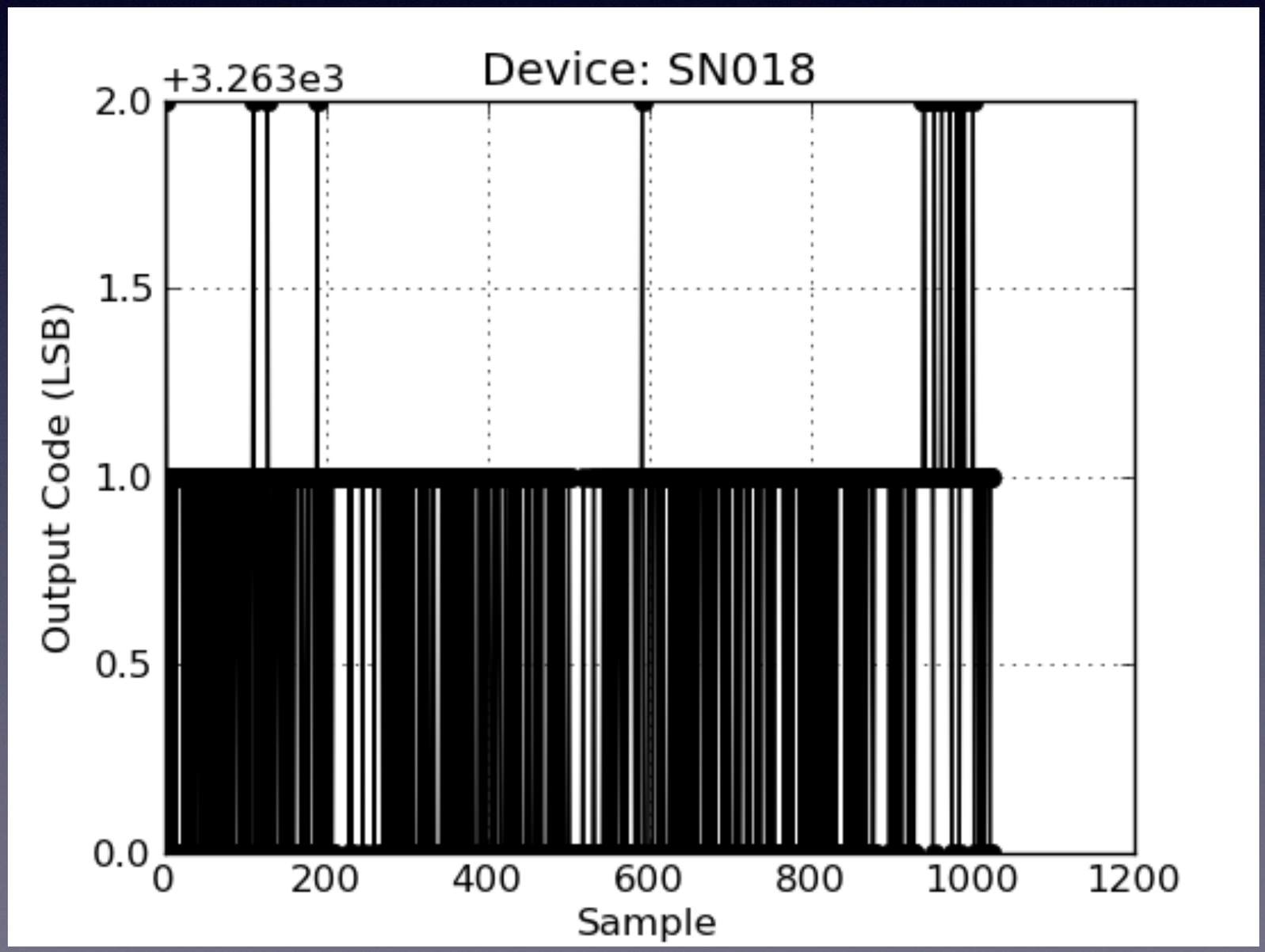


Performance Results

Performance Results

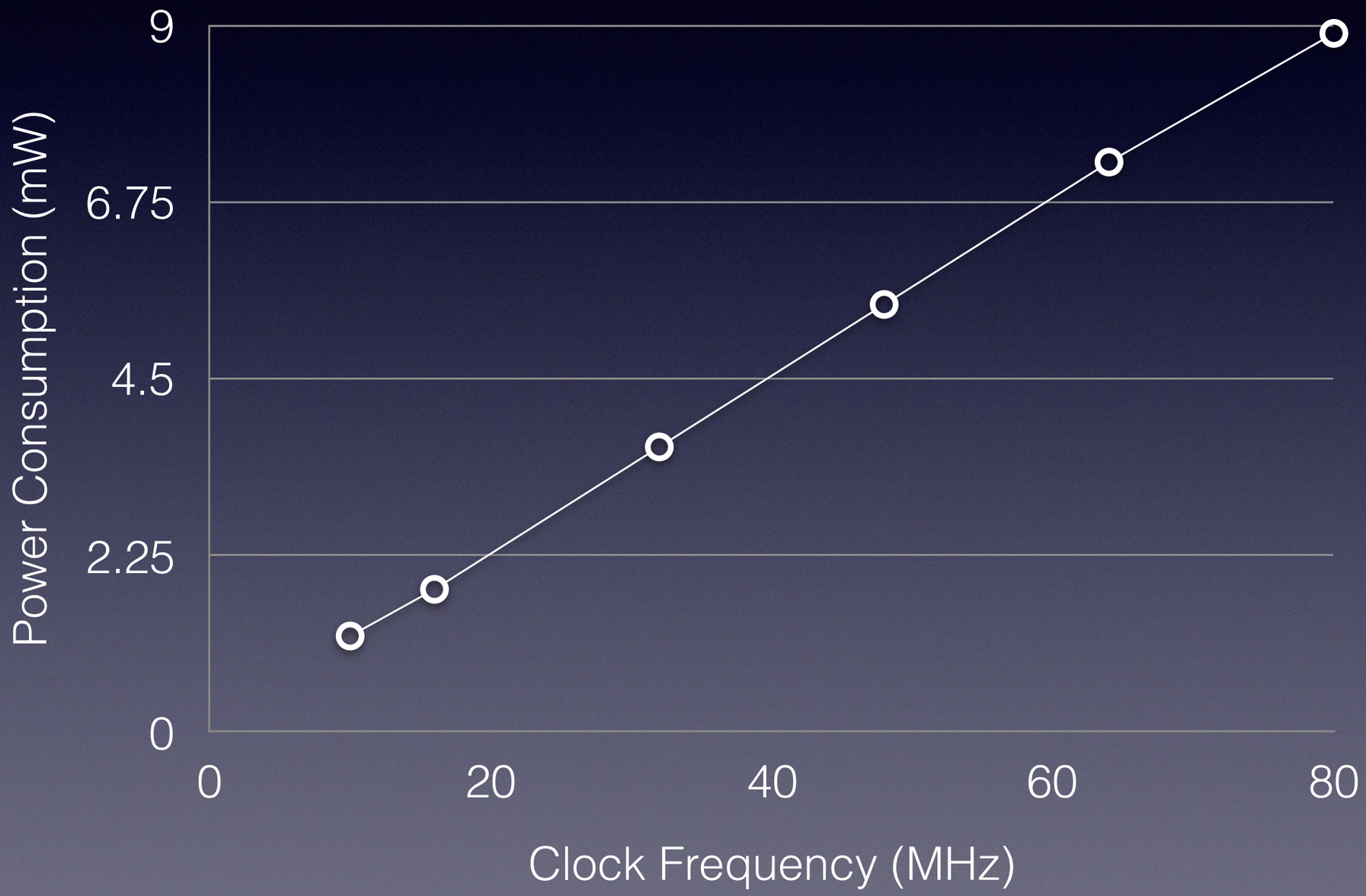
Digital Induced Noise

1024 ADC samples in RTU configuration at -55 degC @ 2 ms sampling period, and internal voltage regulator ON.



Performance Results

Digital Power Consumption

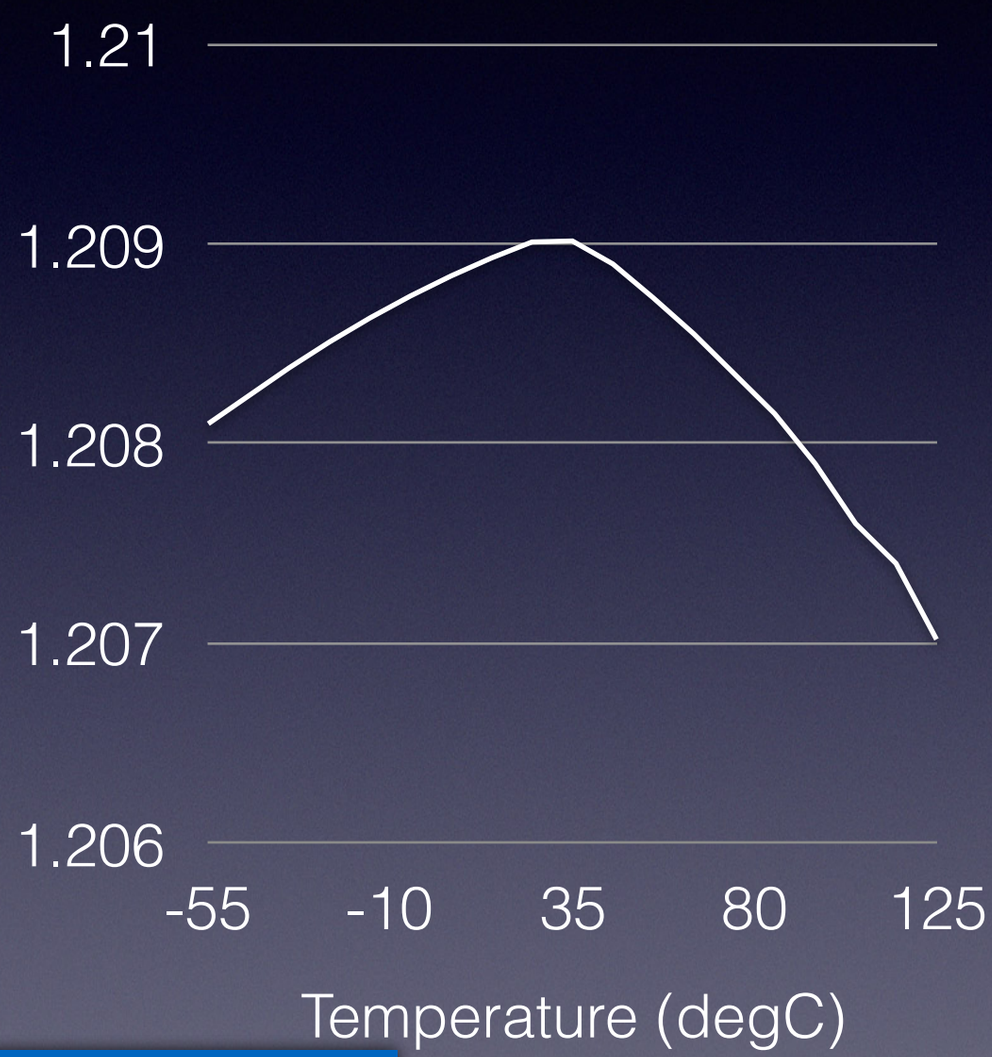


Performance Results

Voltage Reference Performance

Voltage Reference

- Untrimmed performance of 15-20 ppm/degC
- Trimmed performance of ~10 ppm/degC (as show in the figure)
- ETM Vref design is used as basis for designs in higher resolution ADCs

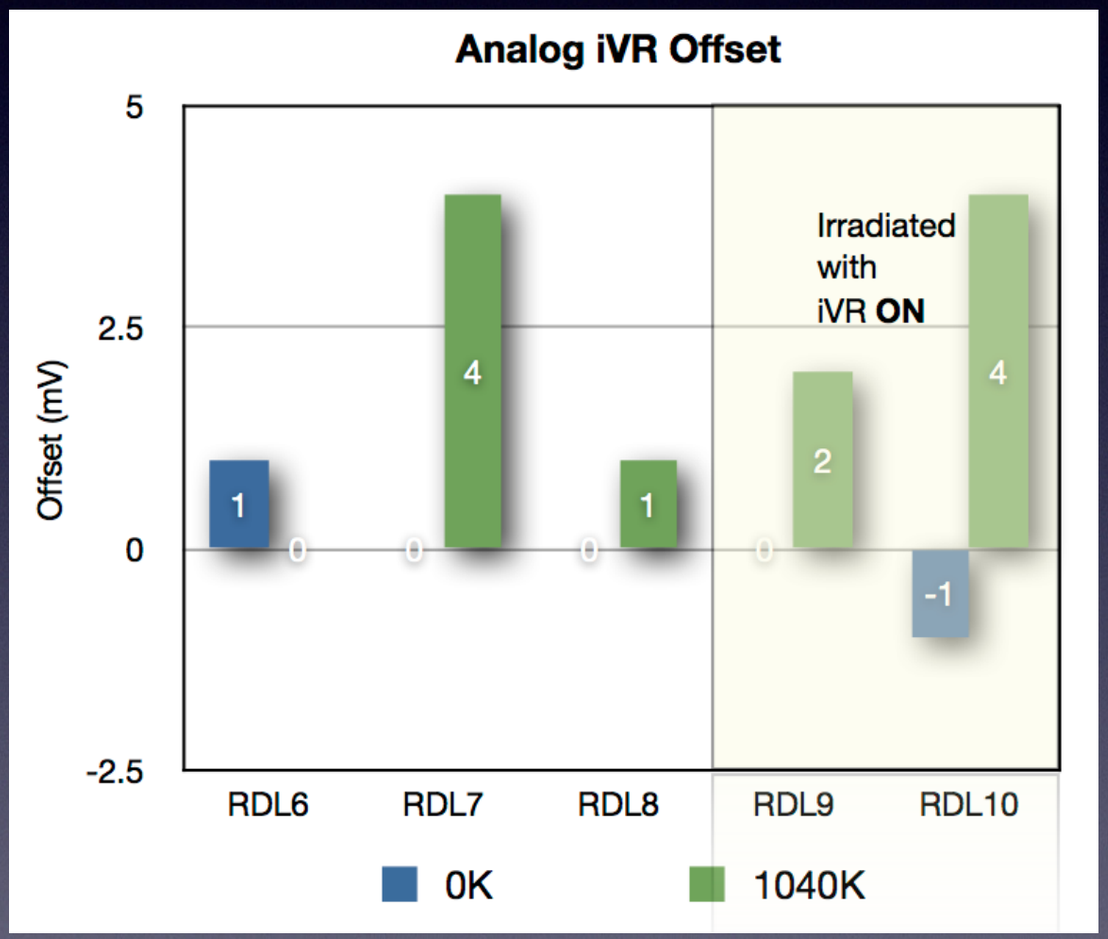


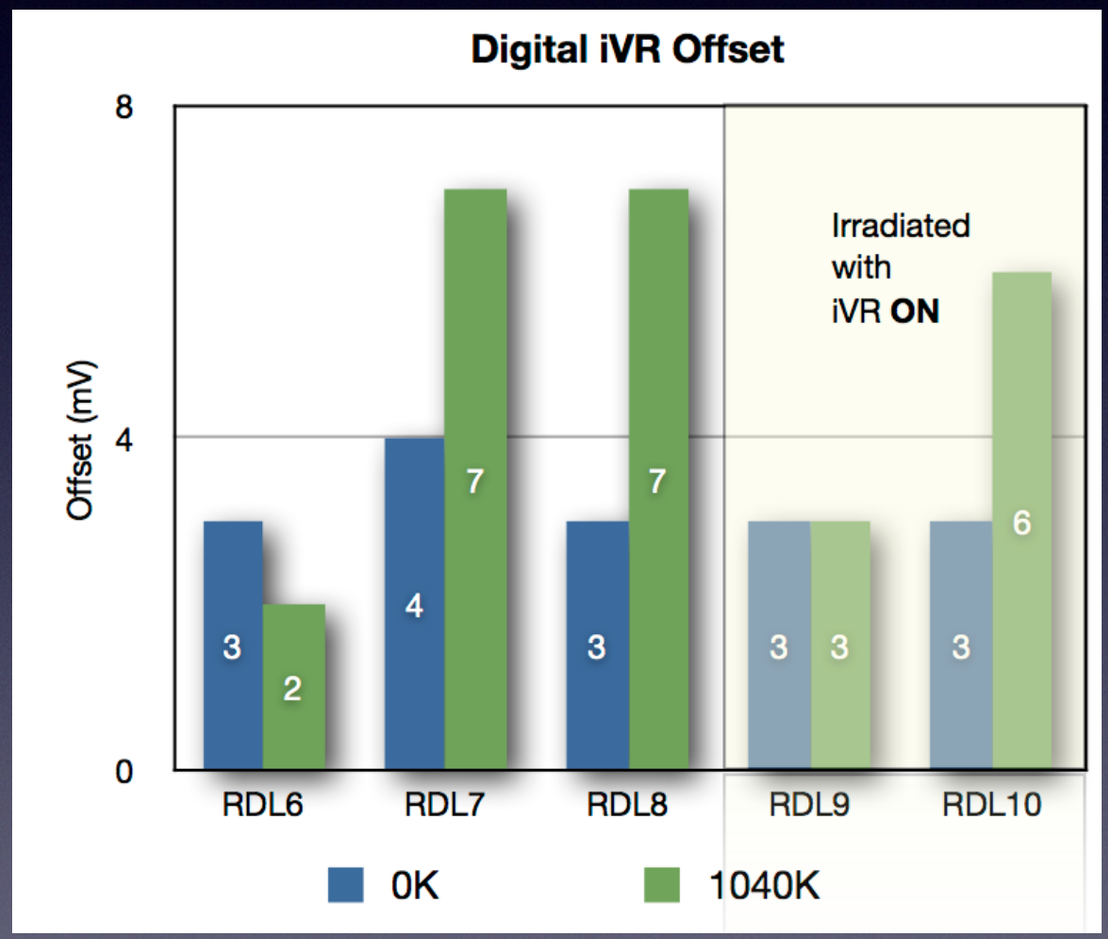
TID effects on the voltage reference

- Temperature Coefficient is increased only by a 1-2 ppm/degC at 300K.

Performance Results

Internal Voltage Regulator TID Performance



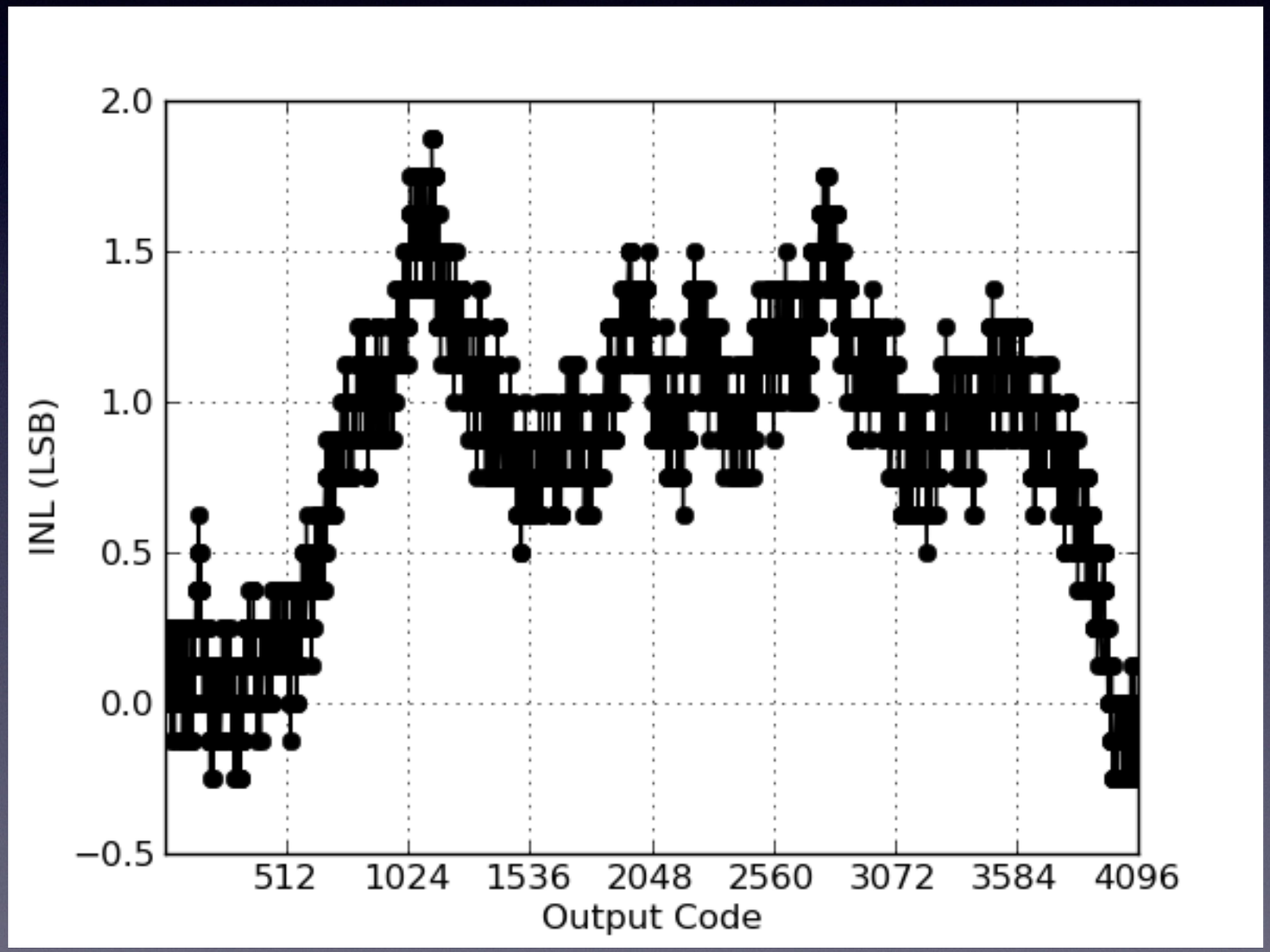


- ETM internal voltage regulator design is the basis for other ASICS that utilize multiple power supplies in the analog and digital domain.

Performance Results

ADC TID Performance

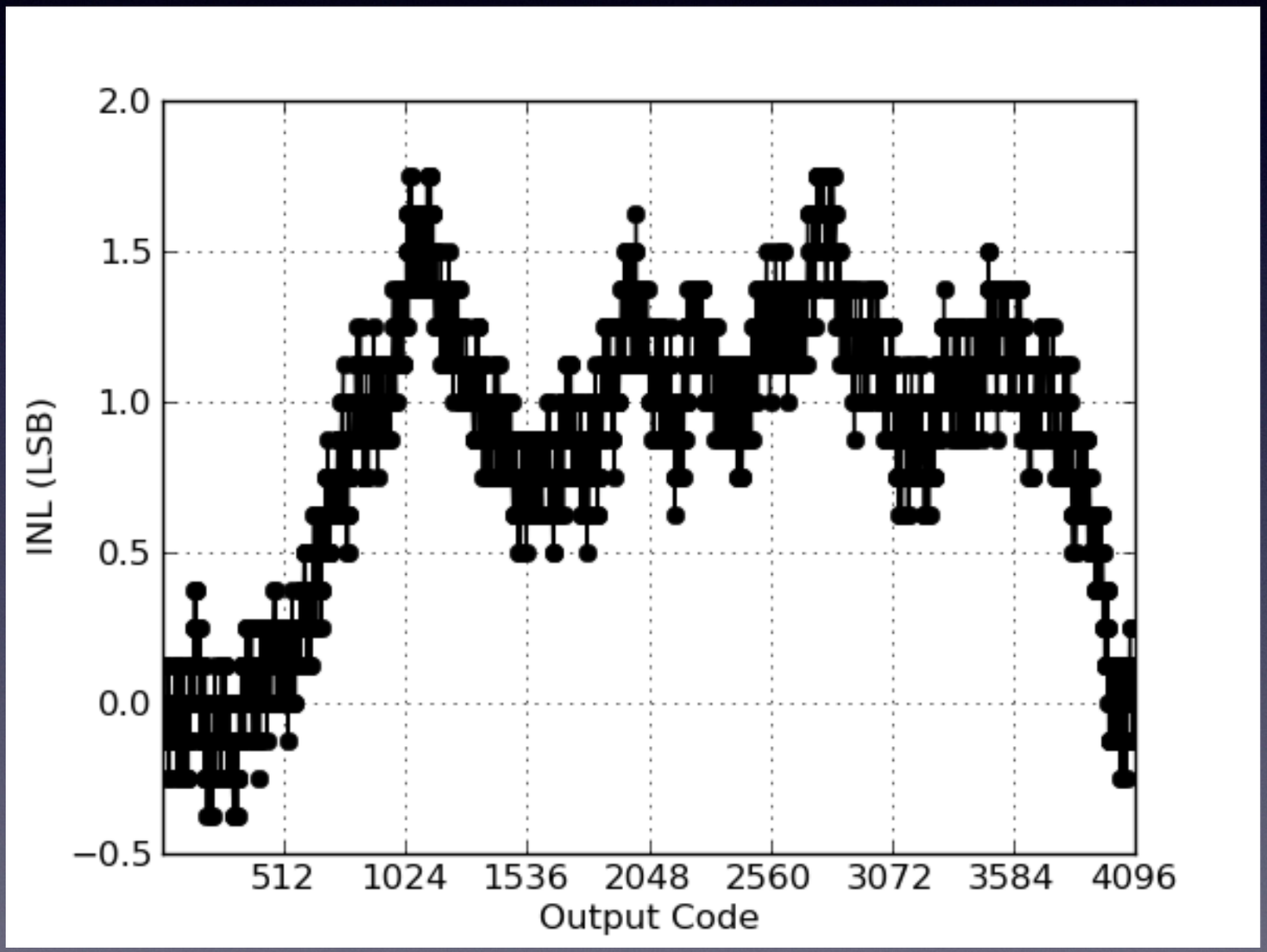
INL @ 0 KRad



Performance Results

ADC TID Performance

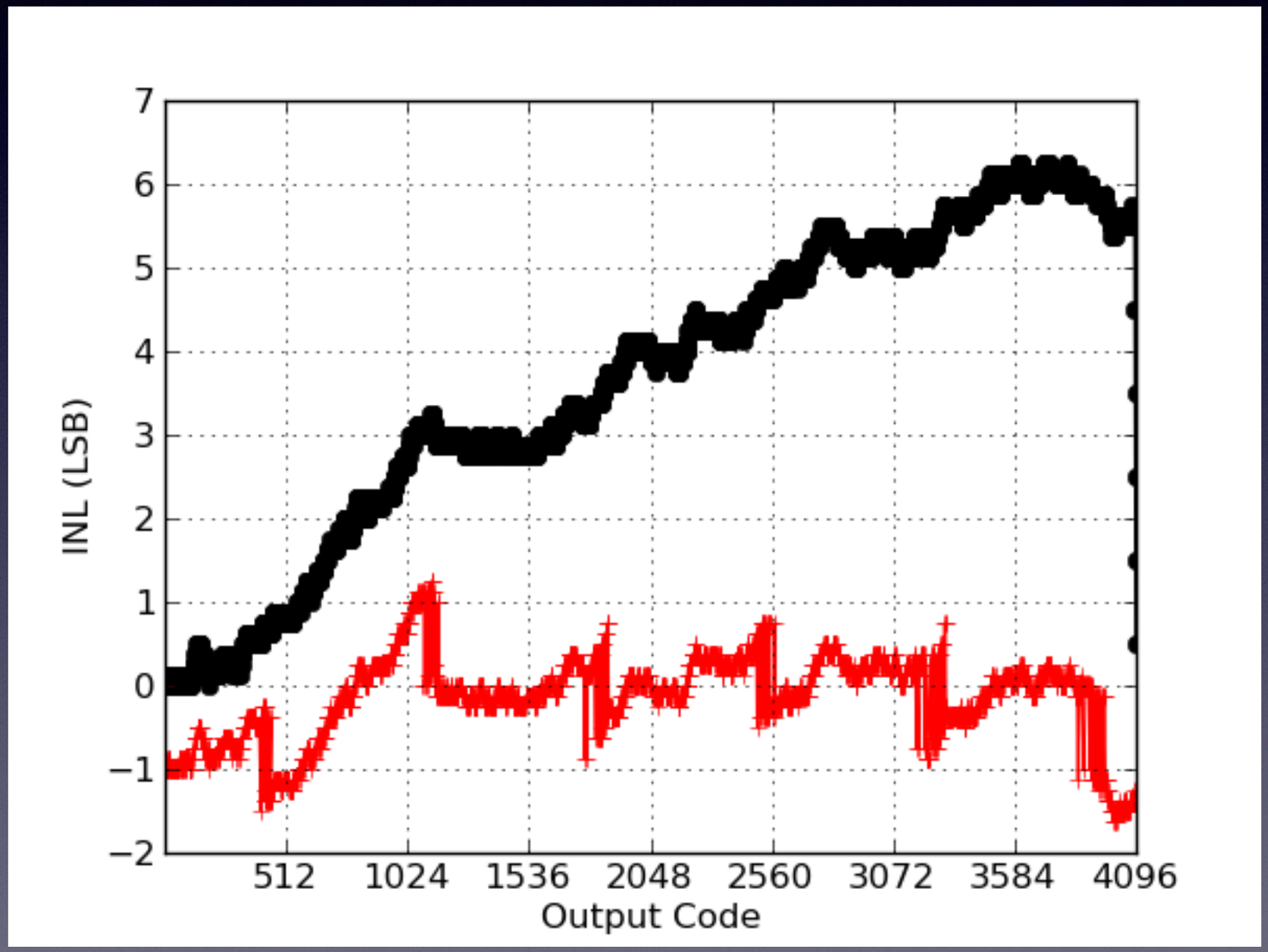
INL @ 100 KRad



Performance Results

ADC TID Performance

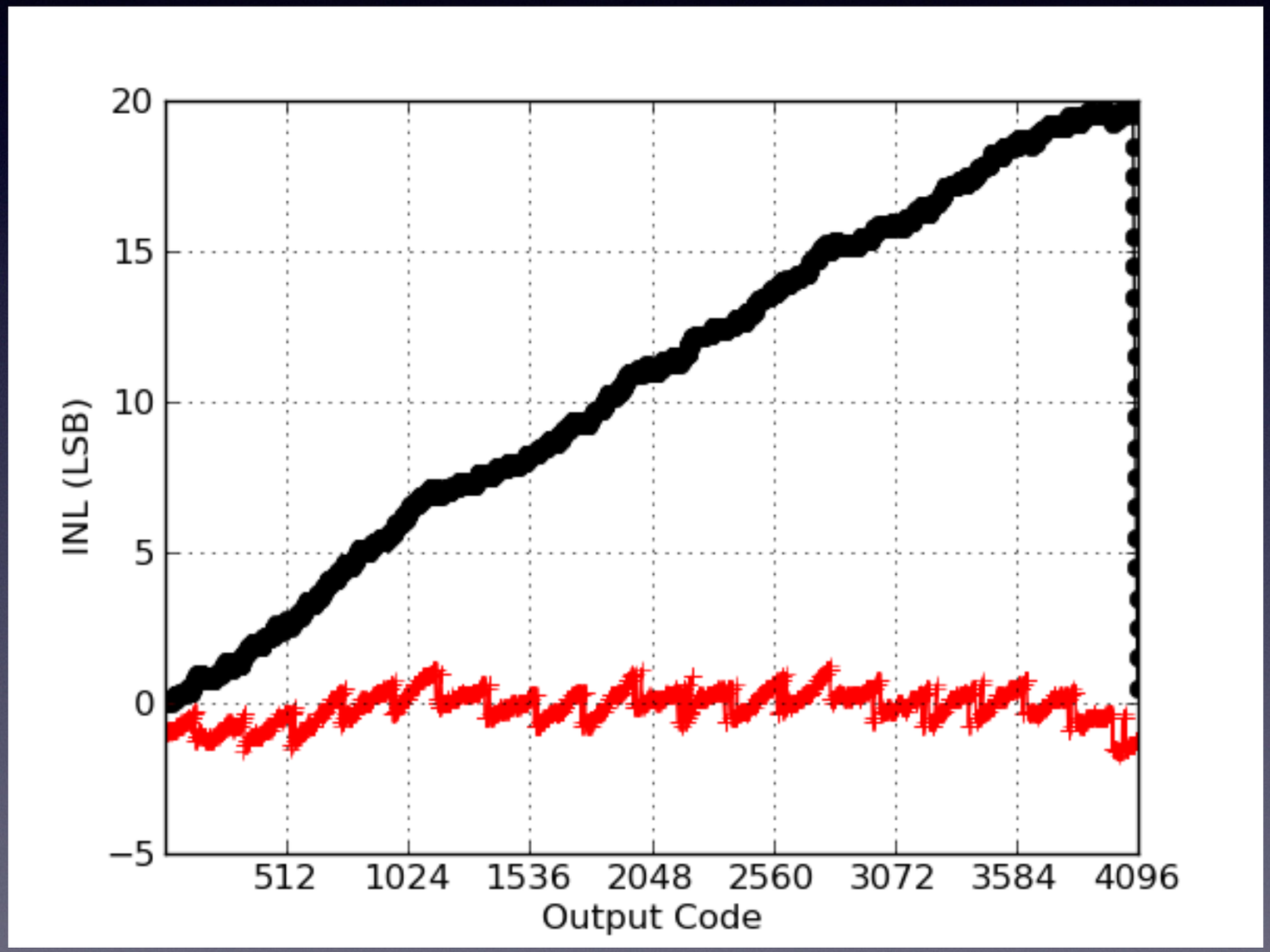
INL @ 600 KRad



Performance Results

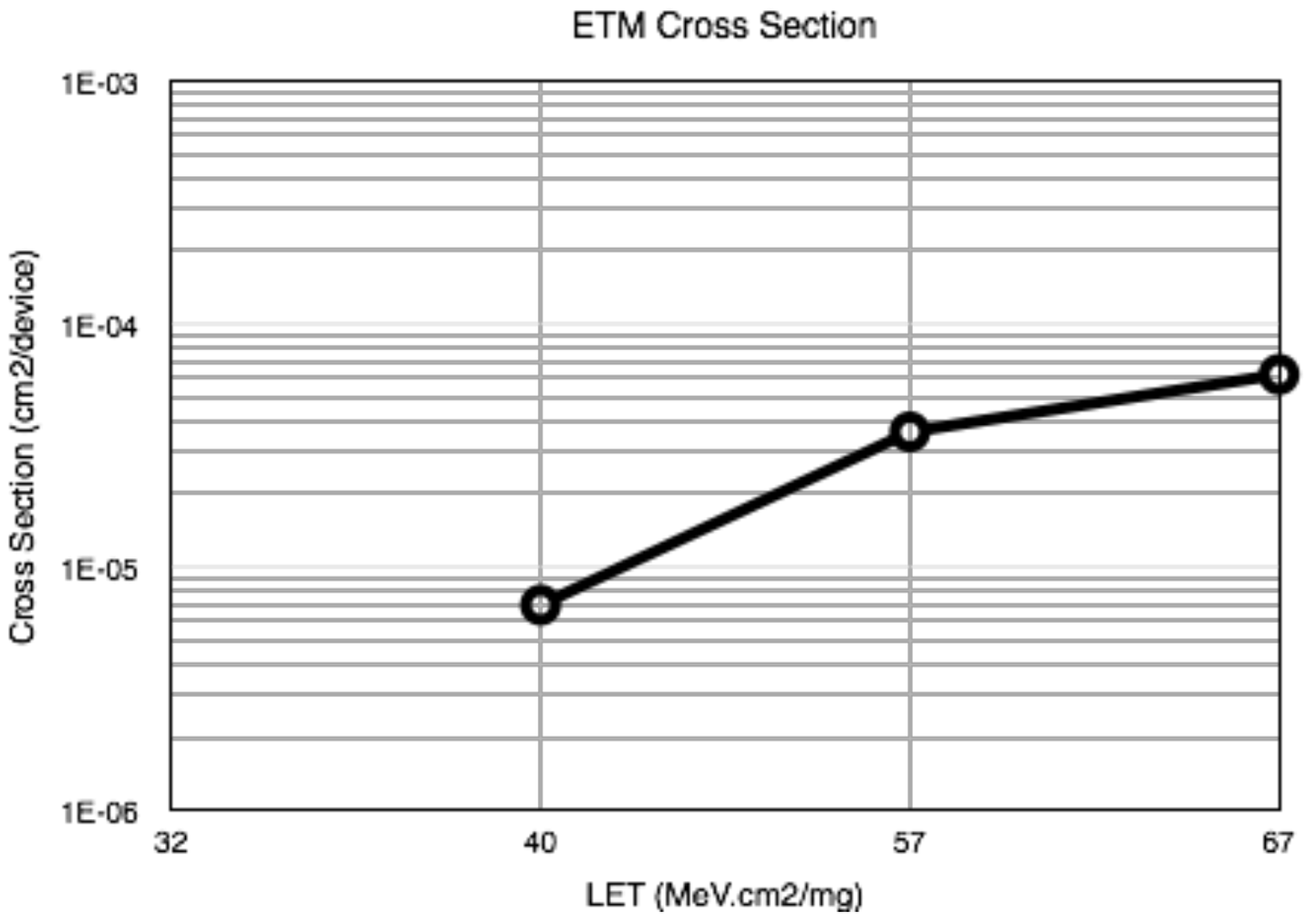
ADC TID Performance

INL @ 1 MRad



Performance Results

SEE Performance



Thank you