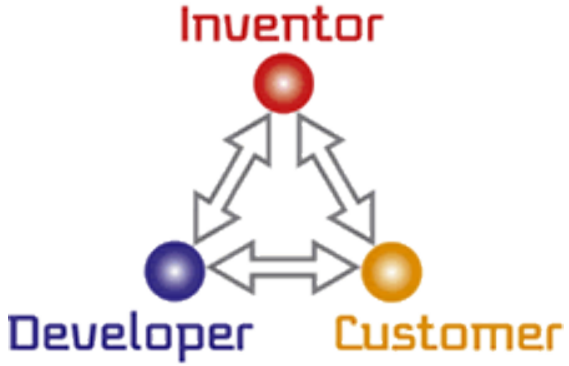
On-Line Testing and Healing Permanent Radiation Effects in Reconfigurable Systems (ITI A)



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Presentation content

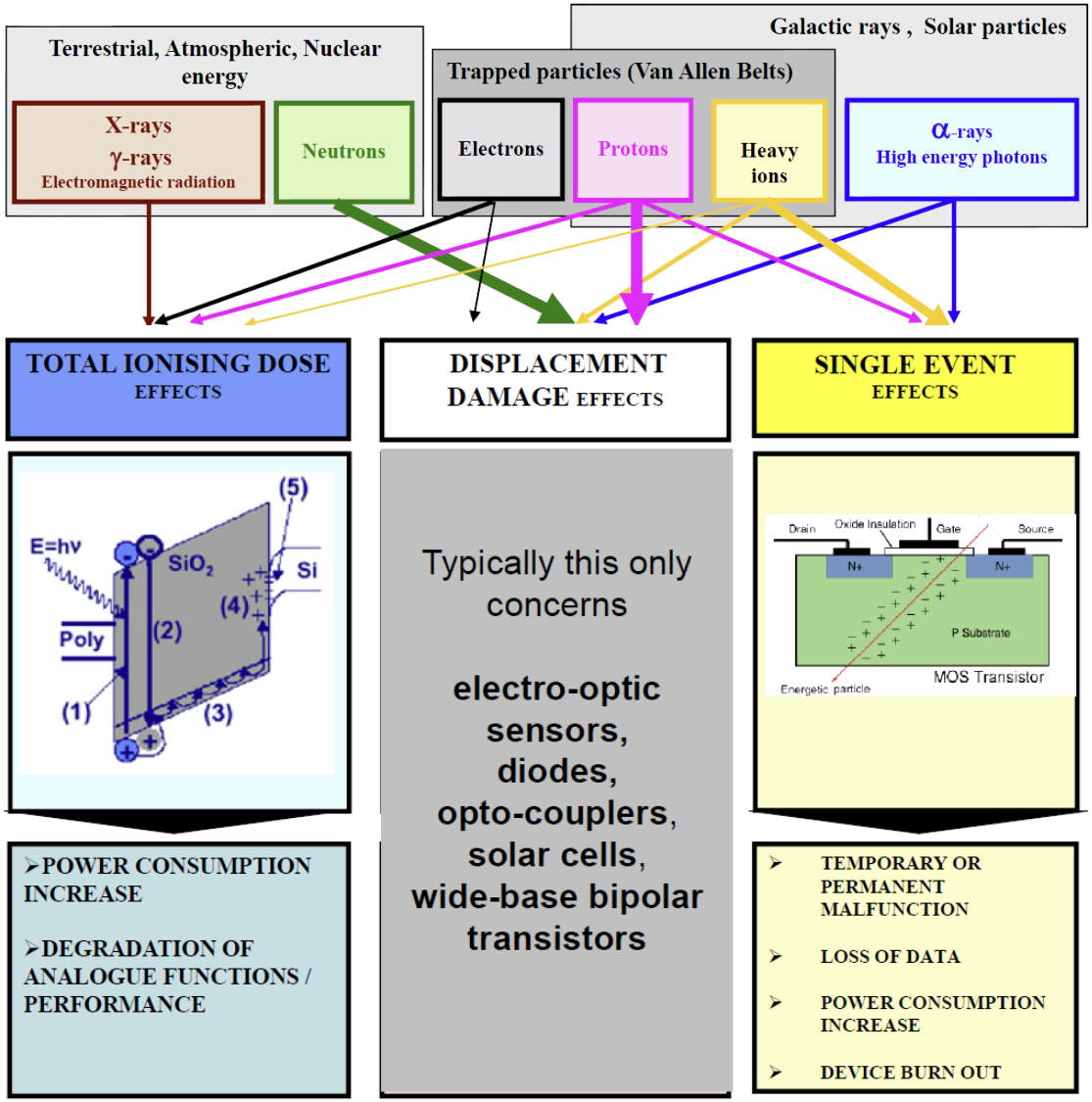
- Motivation
- Origin of the technology
- OLT(RE)^2 CAD flow
- Results
- Conclusion

Motivation
Problem

FPGAs affected by Total Ionising Dose (**TID**) and Single Event Upsets (**SEU**)

•A **single event upset** (**SEU**) is a change of state caused by ions or electro-magnetic radiation striking a sensitive node in a micro-electronic device

•**A total ionizing dose (TID)** is the amount of energy imparted by nuclear (or ionizing) radiation to unit mass of absorbing material



Source: esa Technology and strategies to counteract radiation effects, DCIS 2010

Motivation
State of Art

- **FLIPPER:** fault injection and analysis in configuration logic of **XILINX** FPGA (INAF [IT])
- **SUSANNA, JONATHAN**: fault injection and analysis in configuration logic of **ATMEL** FPGA (ESA, P di Torino [IT])
- **RORA, STAR**: SEU-protection-aware synthesis, P&R in **XILINX** FPGA (P di Torino [IT])
- **FT-UNSHADES:** fault injection and analysis in users logic of **any IC netlist** (U o Sevilla [ES])
- Fault-tolerance, space exploration and system **reconfiguration of multi-FPGA systems** (XILINX, ESA, P di Milano [IT], LuxSpace [LX], TWT [D], AST-UK [UK])
- Radiation Tests of **ACTEL-proASIC** (FLASH) (ESA, Pdi Torino [IT])

Source: Technology and strategies to counteract radiation effects, DCIS 2010

Motivation
State of Art

- **SEU emulation, simulation and mitigation analysis tools overview**

Tool Name	Developer	Tech	SEU injection	SEU sim at SW speed	SEU emu at HW speed	Monitor fault propagation	SEU weak areas finding	Recognize & check TMR	SEU in FPGA Conf mem	Improve P&R of SRAM-FPGA
FT-UNSHADES	U. Seville (E)	all	yes		yes	yes	yes		yes	
SST	ESA (NL) / U. Antonio Nebrija (E)	all	yes	yes		yes	yes			
FLIPPER	INAF (I)	Xilinx FPGA	yes		yes	yes	yes		yes	
STAR/VPLACE /RoRA	P. Torino (I)	Xilinx FPGA					yes		yes	yes
INFAULT	ESA (NL)	all					yes	yes		
SUSANNA/ JONATHAN	P. Torino (I) / ESA (NL)	Atmel FPGA					yes		yes	yes

- **Permanent Errors?**

Source: esa Technology and strategies to counteract radiation effects, DCIS 2010

Motivation
Solution: OLT(RE)^2

On-**L**ine **T**esting and Healing Permanent **R**adiation **E**ffects in **RE**configurable Systems

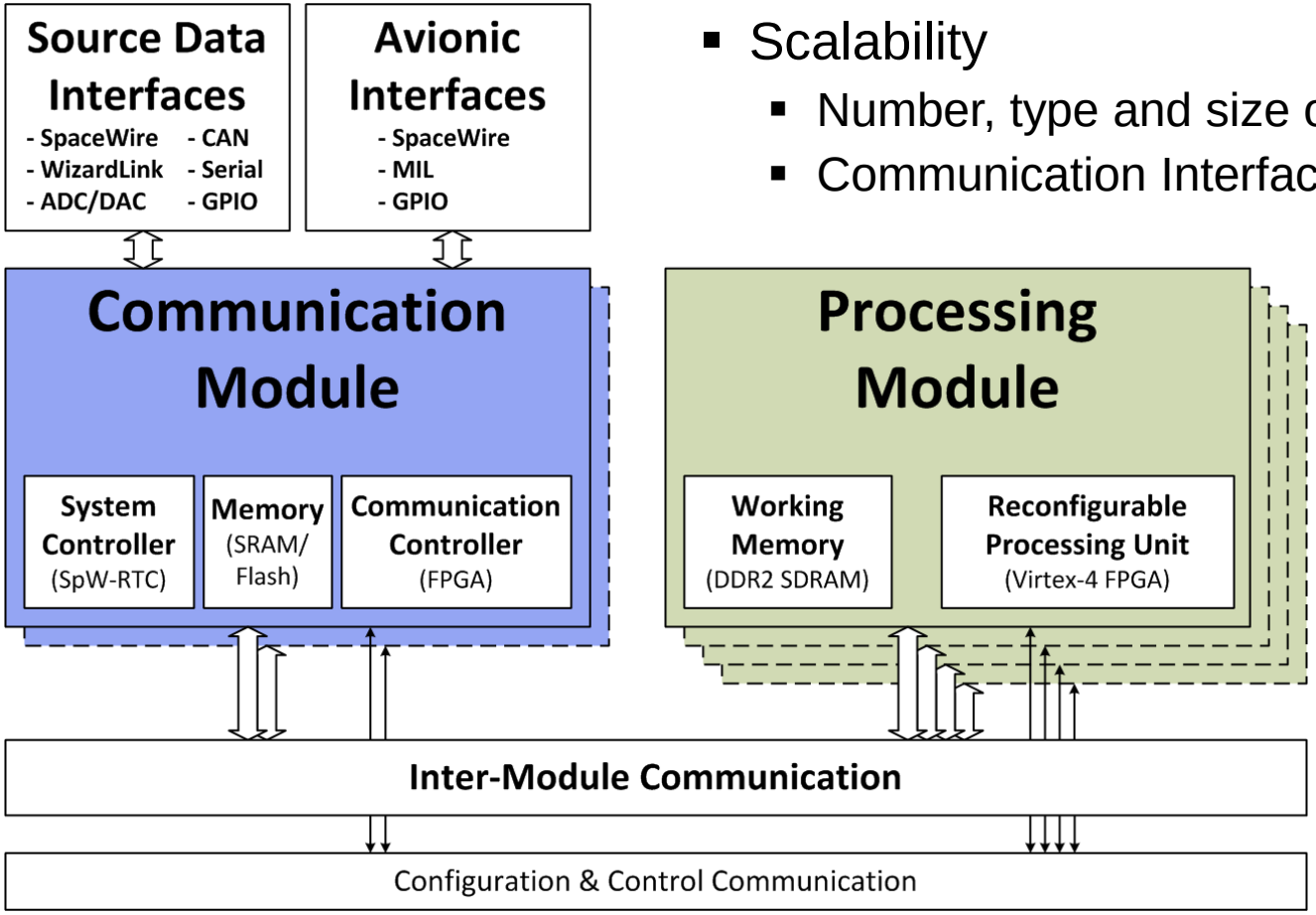
- Single Event Effect: Effect of a particle causing soft error(s)
  - ⇒ Memory elements (SEU)
  - ⇒ Transient effects (SET, SEFI, SEL, …)
- Total Ionizing Dose: effect of charge accumulation
  - ⇒ Permanent errors
- **Idea:** Flow capable to detect and patch partially damaged FPGAs used in space flight missions
- **Key Aspects:**
  - On-line testing of partially FPGAs resources
  - SEUs tools utilized for detection of permanent fault
  - Design flow suitable for Xilinx Virtex-4, -5, -6, -7 and Spartan-6 (based on DHHarMA, Dedicated packer, placer and router for homogeneous macros [FCCM 2011])

Origin of the technology

- Motivation
- Origin of the technology
- OLT(RE)^2 CAD flow
- Results
- Conclusion

Origin of technology
DRPM

DRPM – FPGAs for satellite payload processing



- Scalability
  - Number, type and size of FPGAs
  - Communication Interfaces

Partners

esa

TWT

POLITECNICO DI TORINO

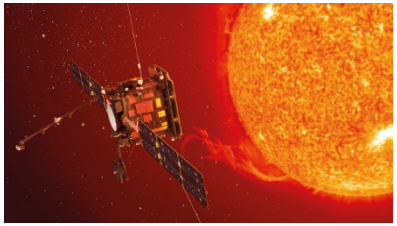
SWISS SPACE TECHNOLOGY
PRECISION ELECTRONICS FOR SPACE FLIGHT

DRPM – Dynamically **R**econfigurable **P**rocessing **M**odule

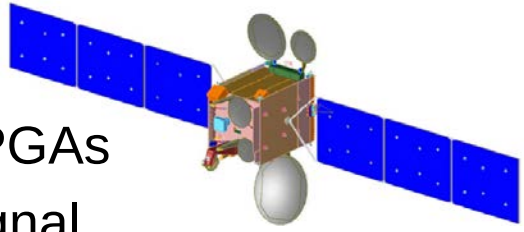
Origin of technology

Use of reconfiguration in space app

- **Solar Orbiter** (PHI DPU)**:** mission (2018-2028)
  - + Two SRAM-based **reconfigurable Virtex-4QV** FPGAs
  - + **FPGA Reconfiguration** for algorithm adaptation during mission and share resources.



- **Fraunhofer On-Board Processor** (FOBP), Heinrich Hertz Satellite, launch in 2020
  - + Two SRAM-based **reconfigurable Virtex-5QV** FPGAs
  - + **FPGA Reconfiguration** for High speed Digital Signal Processing Experiments



Innovation Content

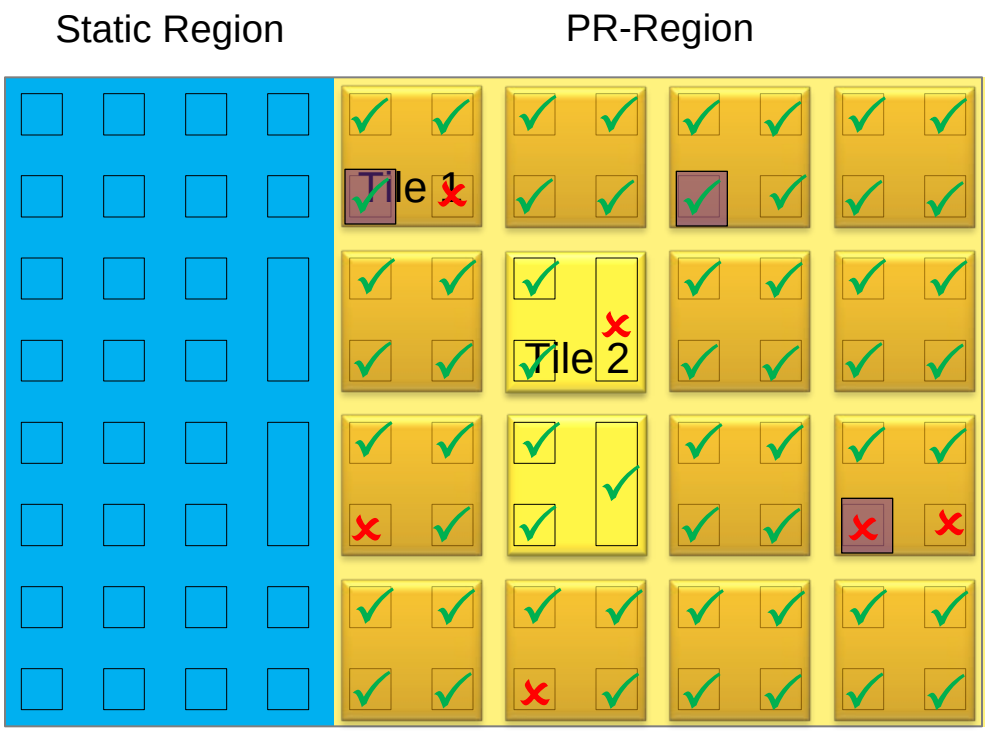
Permanent fault State of Art

- **OLT(RE)^2 main innovation:**
  - + **Online Testing of Routing Resources (using run-time reconfiguration of FPGAs)**

Title	Authors	Note
OTERA: Online Test Strategies for Reliable Reconfigurable Architectures (2010)	Bauer, Braun	Online Testing approach for logic resources **- Just logical resources**
A Novel BIST Approach for Testing Logic Resources Using Hard Macro	Zhang, Wen	Testing for logic resources with using HMs **- Just logical and offline**
Detection and Diagnosis of Faults in the Routing Resources of a SRAM based FPGAs	Jamuna, Agrawal	Testing of approach for routing resources - **offline test**
BIST for Logic and Memory Resources in Virtex-4 FPGAs	Stroud, Dhingra	Test logic and memory resources **- offline test**
System-Level Built-in Self-Test of Global Routing Resources in Virtex-4 FPGAs	Stroud, Yao	Testing of routing resources - **offline test (after manufactoring)**

Innovation Content
Solution

- **On-Line Testing of permanent Radiation Effects**
- System stays operational during tests, ideal for runtime reconfigurable systems like the DRPM
- Hierarchically approach, coarse/fine grain testing

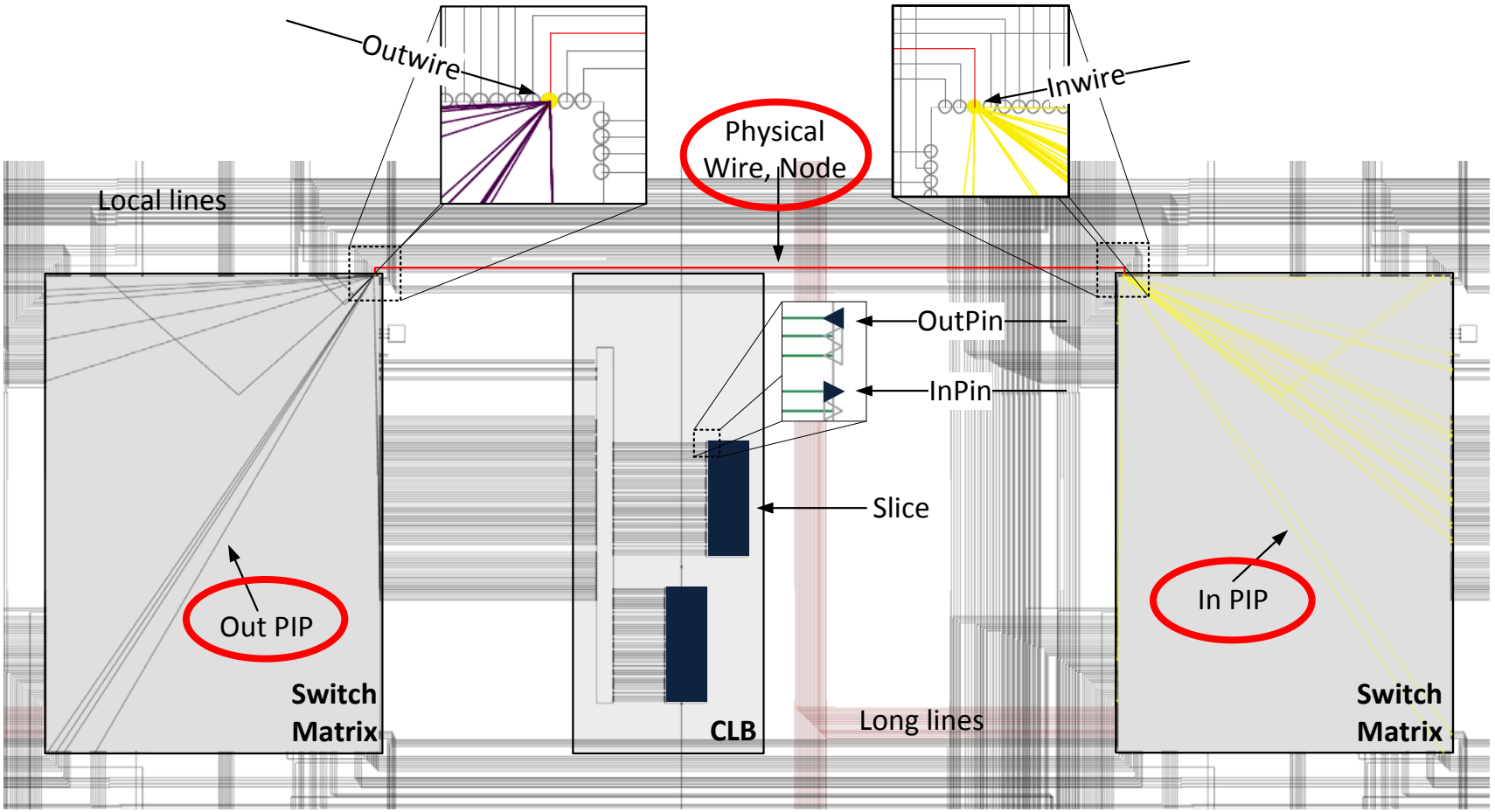


- Self-contained testing macro – can be used without clock/reset/IO
- Runtime reconfiguration used to perform test/readback results
- Faulty resources are patched – all Tiles remain operational

Details

- Motivation
- Origin of the technology
- OLT(RE)^2 CAD flow
- Results
- Conclusion

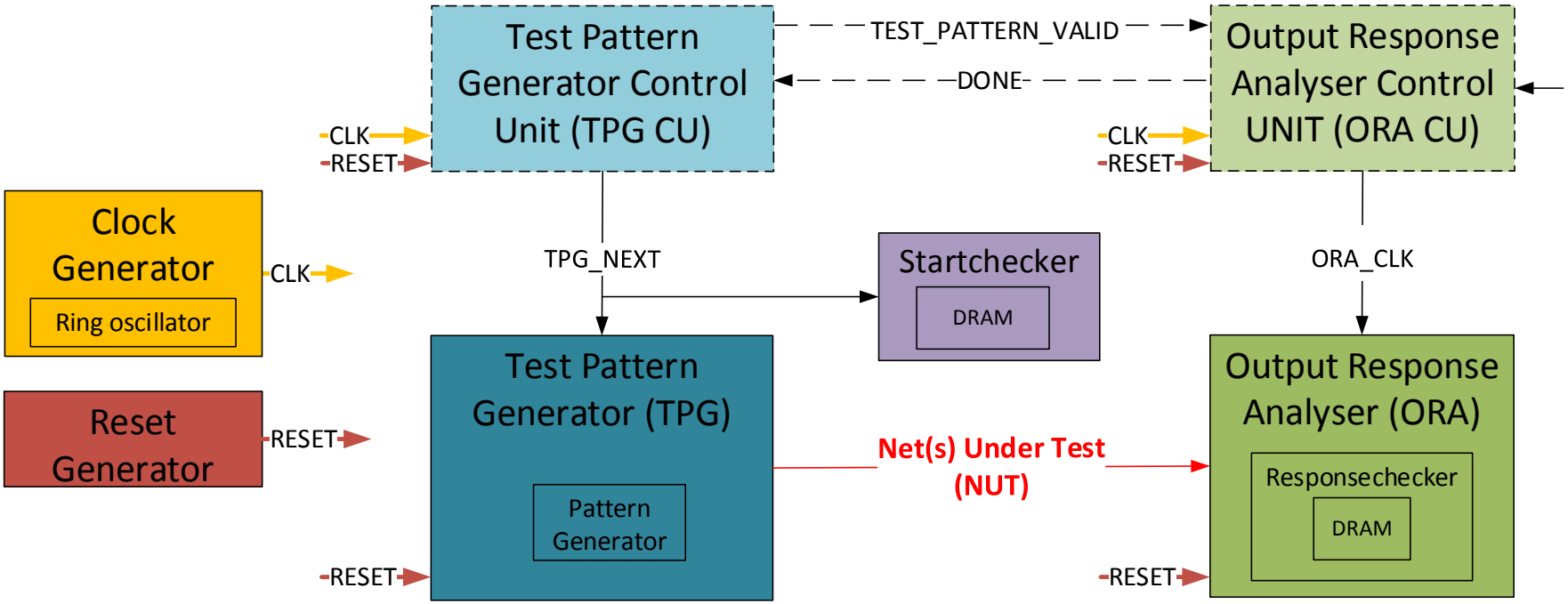
OLT(RE)²
Terminology



FPGA Editor screenshot

OLT(RE)²

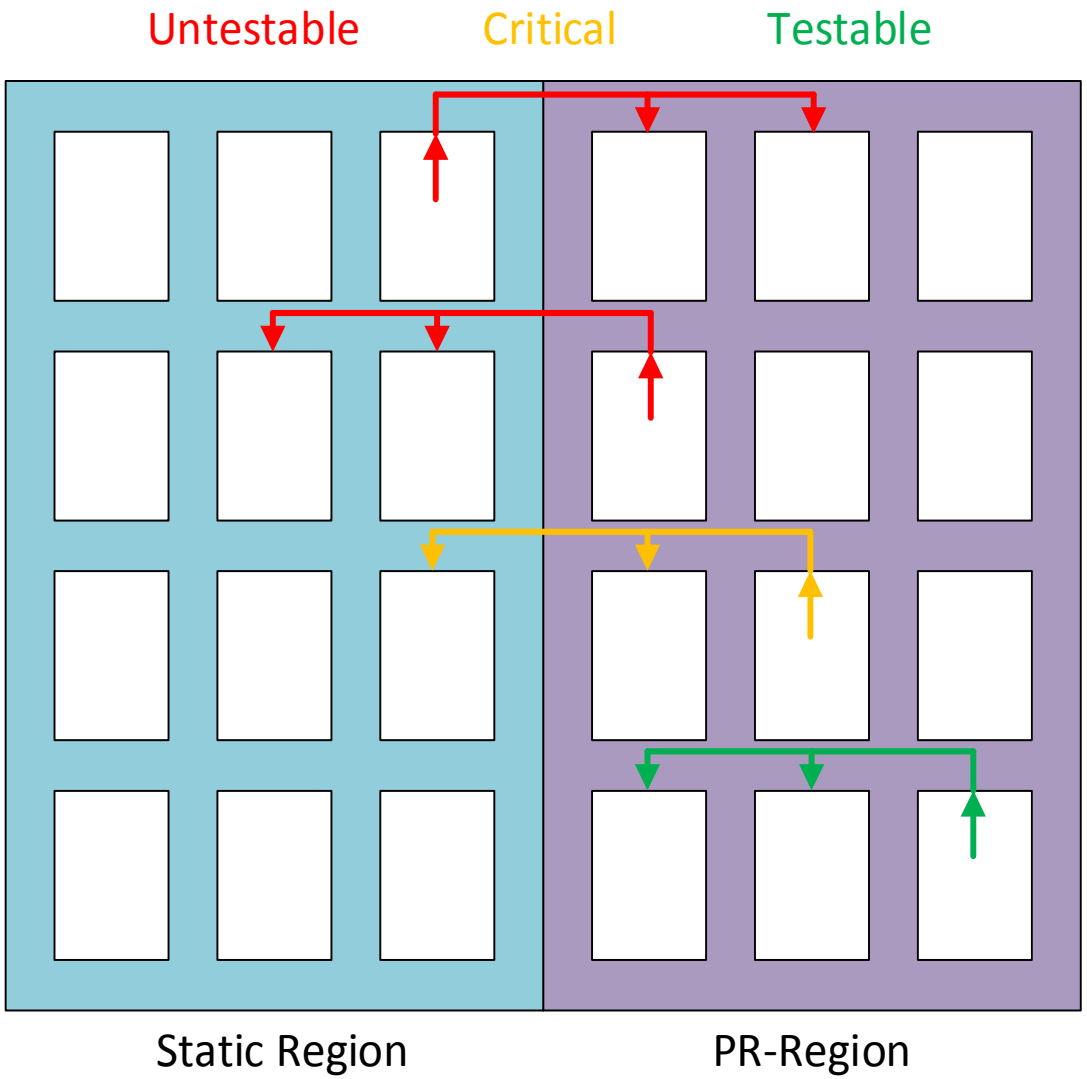
Testing circuit Architecture



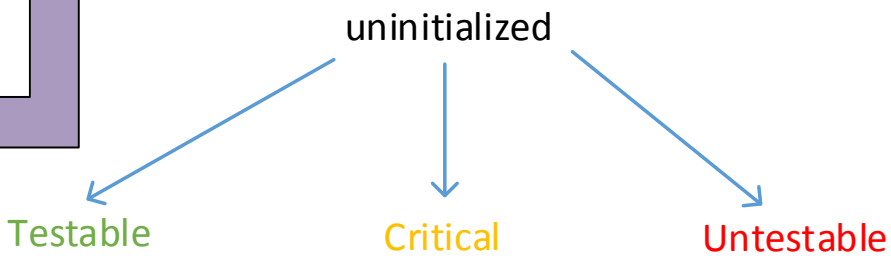
- IOB independent/self-contained circuit using ring oscillator
- Small FPGA resource footprint (~22 slices)
- Testing circuit is placed using dynamic partial reconfiguration
- Readback is used to evaluate results
- 2 different version: NUT6, NUT8

OLT(RE)^2

Classification of Routing Resources



- Initialization of the wire according to the **Inwire** and **Outwire** position

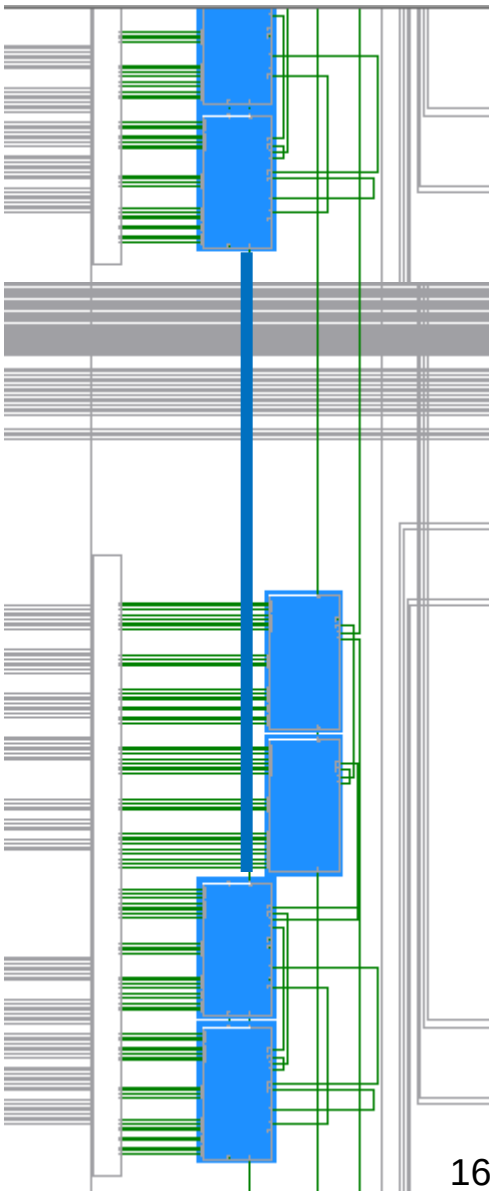


OLT(RE)²

Classification of Routing Resources

- Testable wires are also analized according to the capability of the testing circuit. If a testable resource cannot be tested with the considered testing circuit, it is marked as *unsupported*

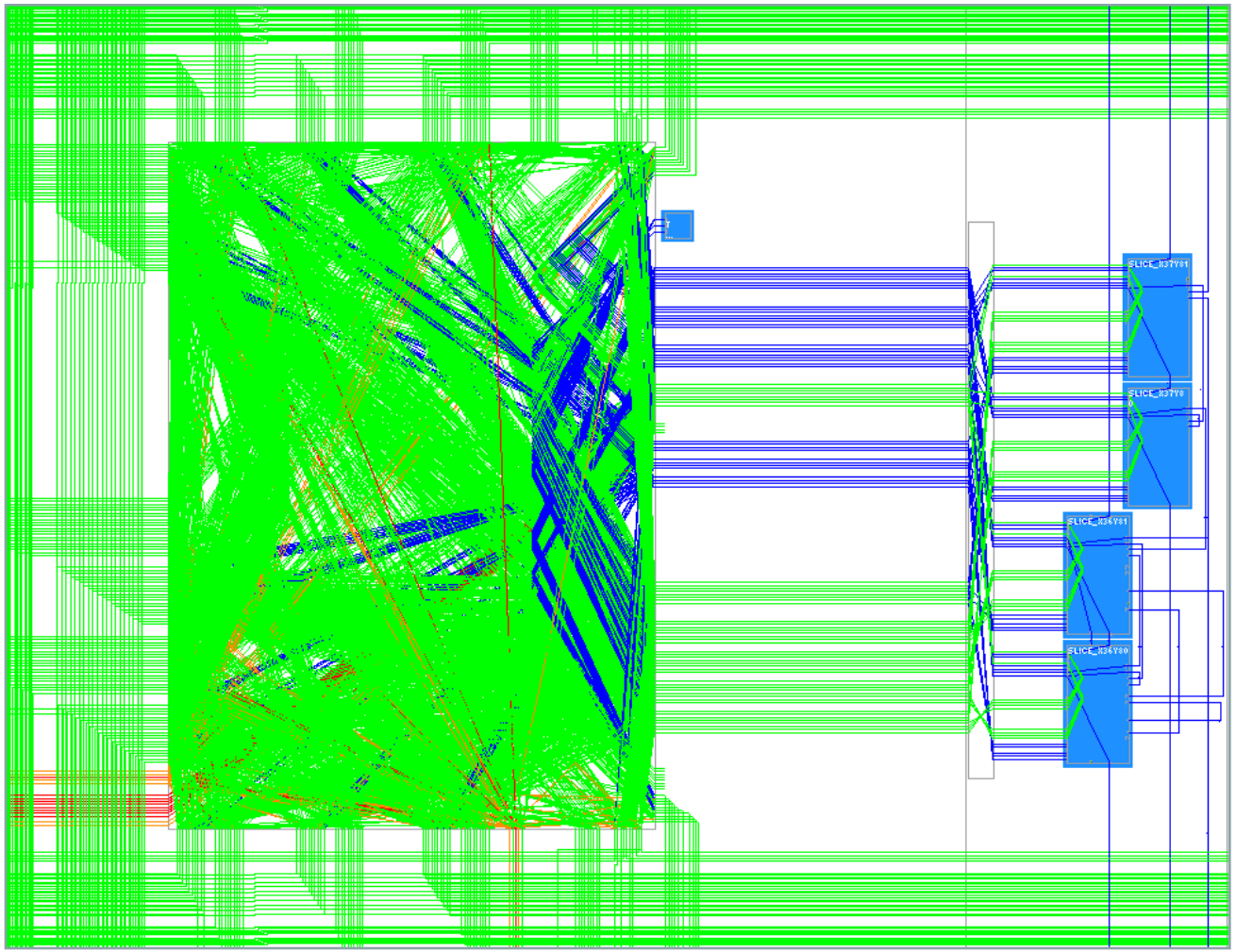
- *e.g. carrychain*



OLT(RE)^2

Classification of Routing Resources

- Untestable
- Critical
- Unsupported
- Testable

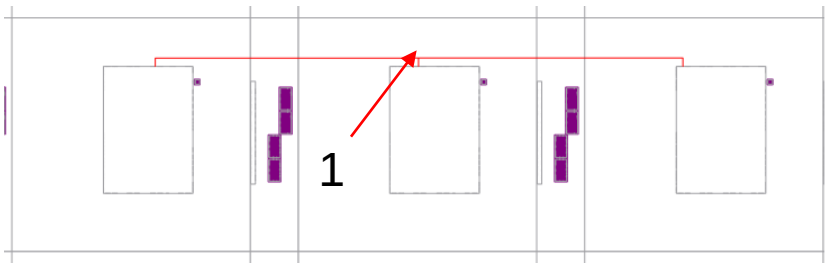


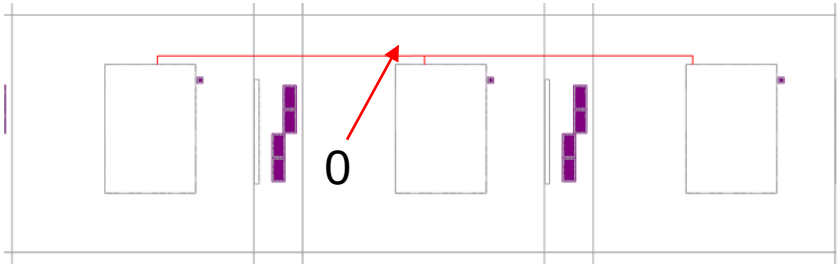
Virtex4 FX12:
INT_X23Y40
Total PIPs: **3312**
Total physical wires: **418**

OLT(RE)²

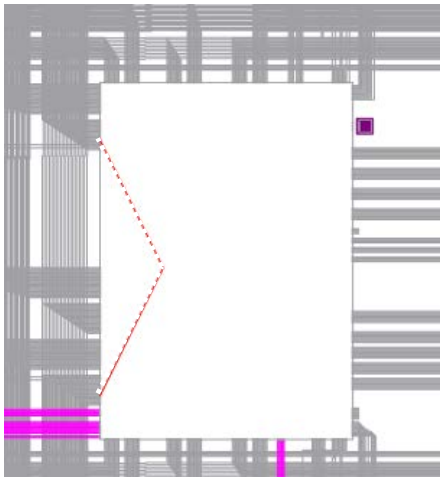
Fault Model

Complexity Level 1: Stuck-at-0 and Stuck-at-1 (wires)

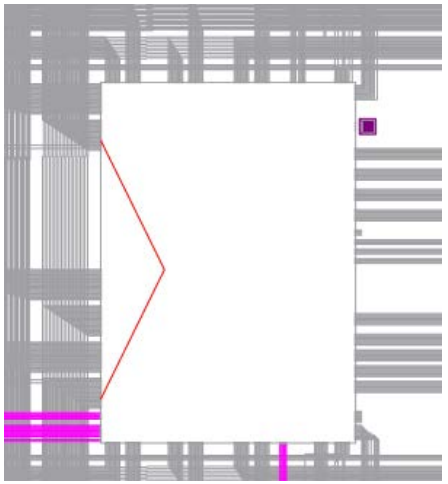




Complexity Level 2: Stuck-off (PIP)

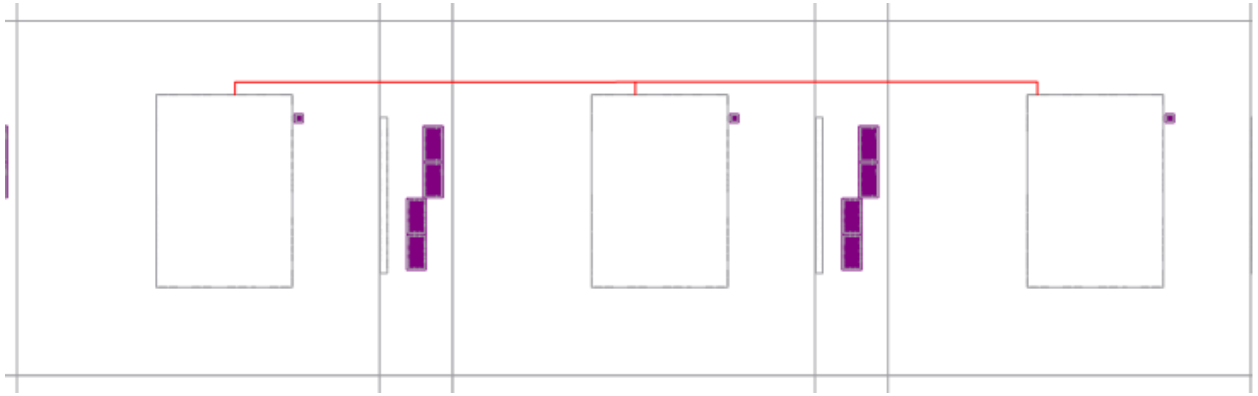


Complexity Level 3: Stuck-on (PIP)



OLT(RE)²

Wire stuck-at-0/1: Effect and verification

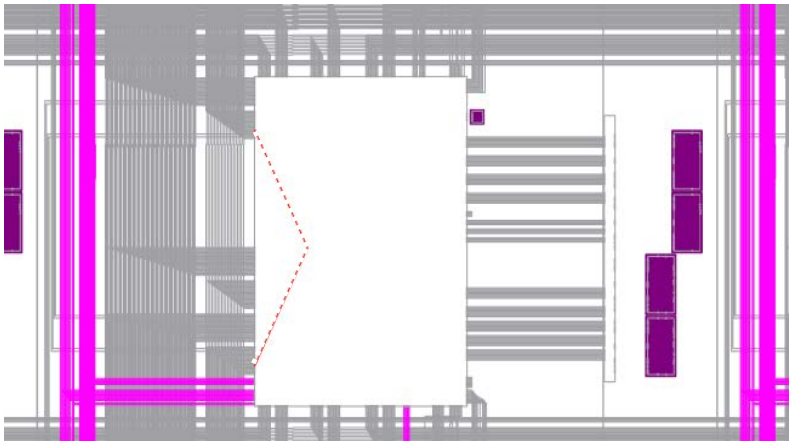


- Permanent fault effect
  If a path of a net uses a wire stuck-at-0/1, the net will be always stuck-at-0/1.

- Verification
  We verify if a wire is stuck-at-0/1 free utilizing it in a path of a NUT. If the test is passed, we verify that the wire is stuck-at-0/1 free.

OLT(RE)²

PIP stuck-off: Effect and verification

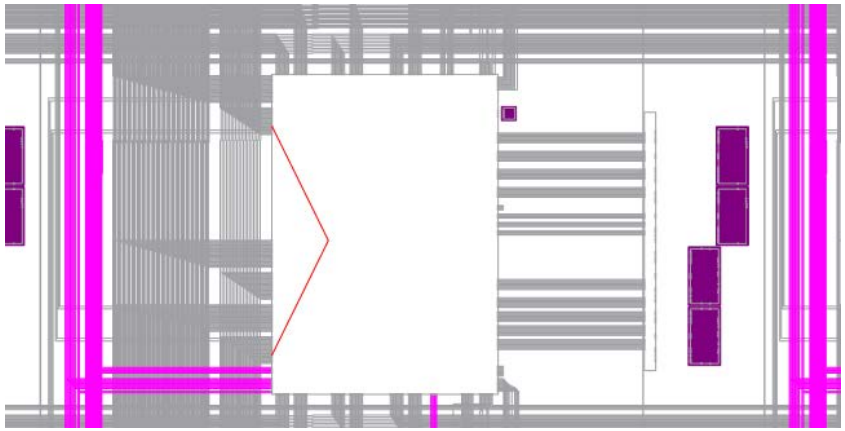


- Permanent fault effect
  If a path utilize a PIP stuck-off, the path will be unknown

- Verification
  We verify if a PIP is stuck-off free utilizing it in a path of a NUT. If the test is passed, we verify that all PIPs of the NUTs are stuck-off free.

OLT(RE)²

PIP stuck-on: Effect and verification



- Permanent fault effect

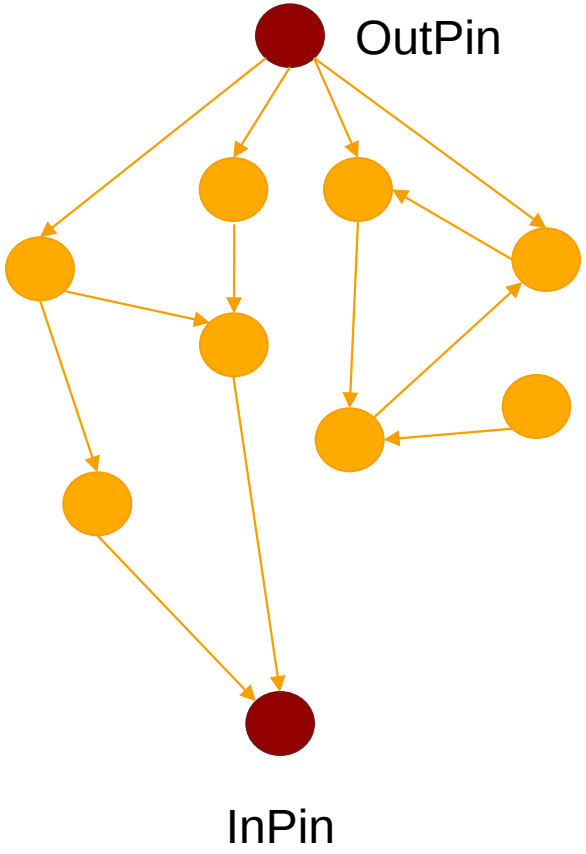
  This PIP can create an antenna or short two nets of the design. The result of the short can be either a wired-AND short or a wired-OR short

- Verification

  If a test was successfully run, we verify that all PIPs that could create a short among the NUTs are PIPs stuck-on free.

OLT(RE)²
Graph Model

- Directed cyclic graph

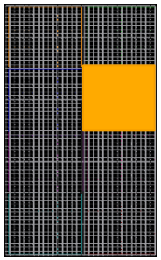


Nodes: Physical Wires

Arcs: PIP

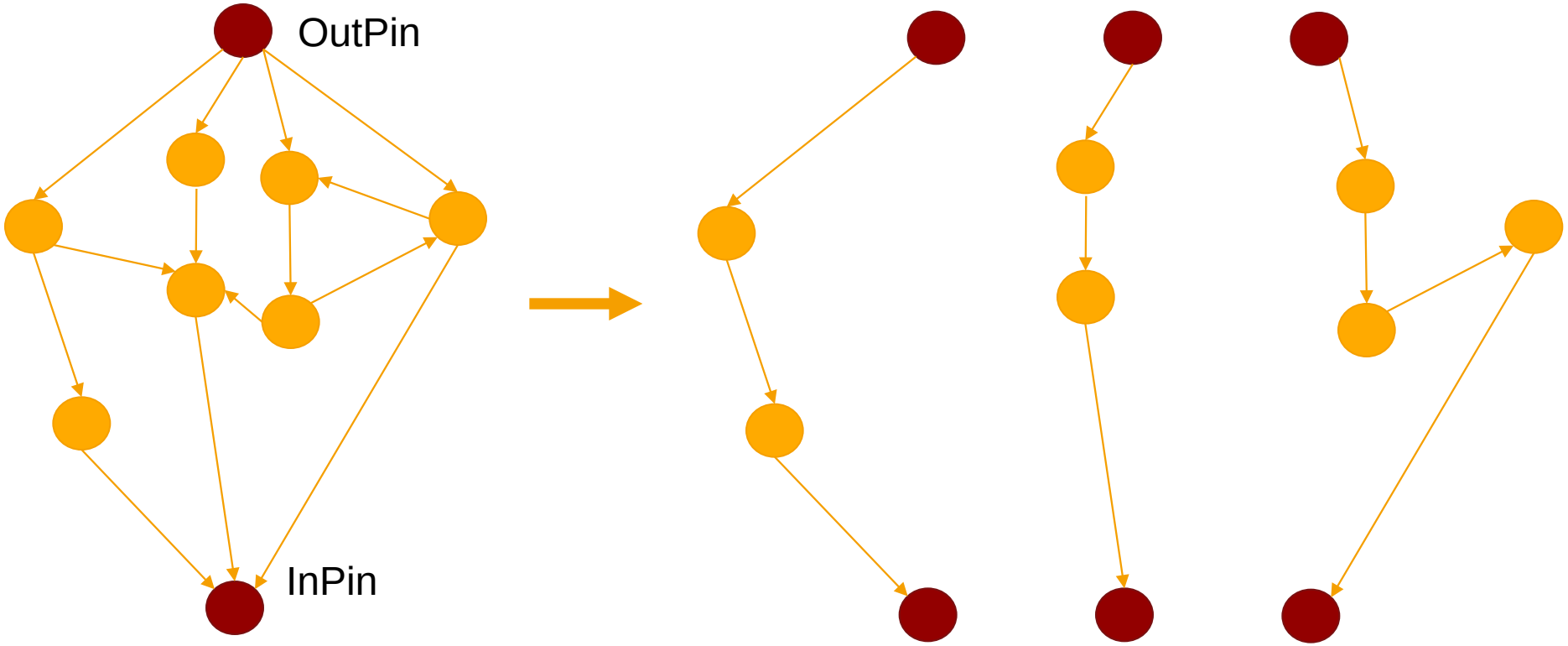
e.g. Virtex-4 FX12, 240 Switch Matrix

Graph dimension:
39,777 Nodes
456,783 Arcs



OLT(RE)²
Level 1 Fault Coverage

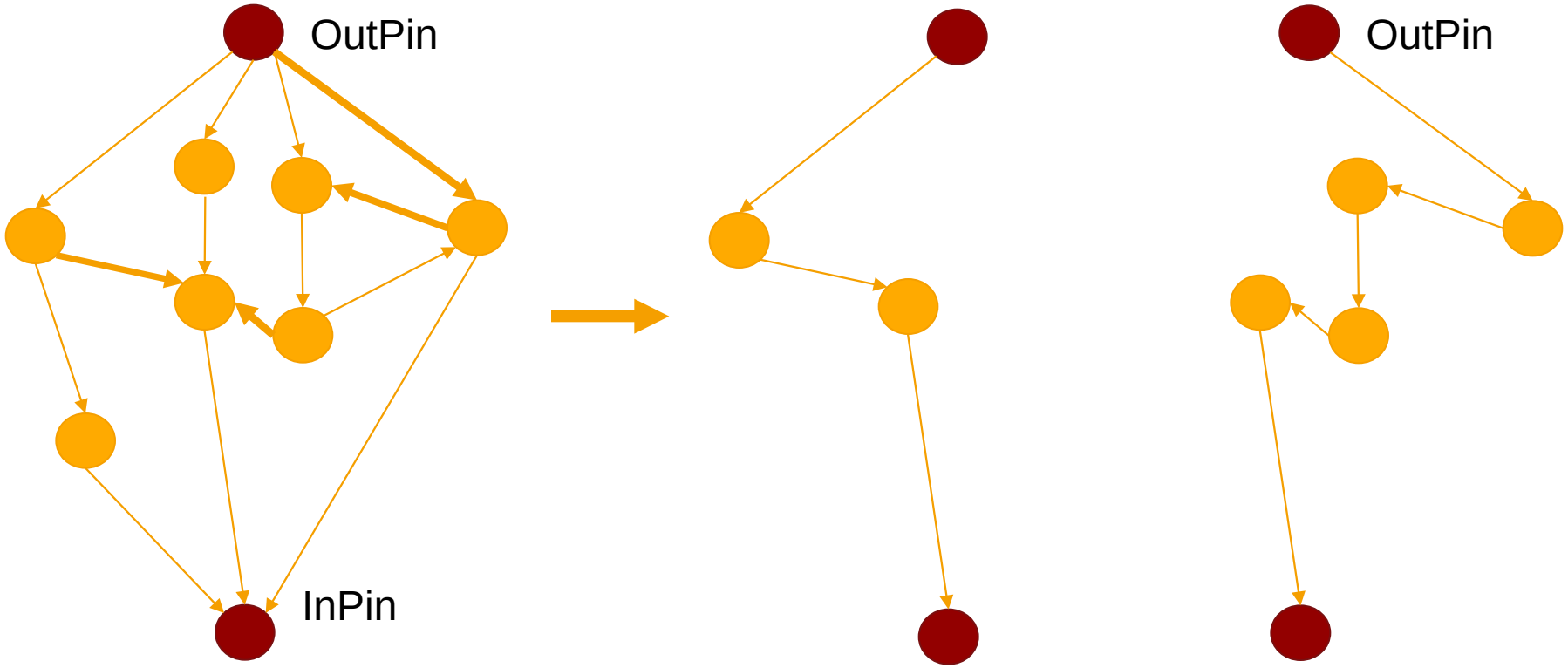
- Cover all the nodes (PhysicalWires) of the Graph



- This step verify that all wires are stuck-at-0/1 free

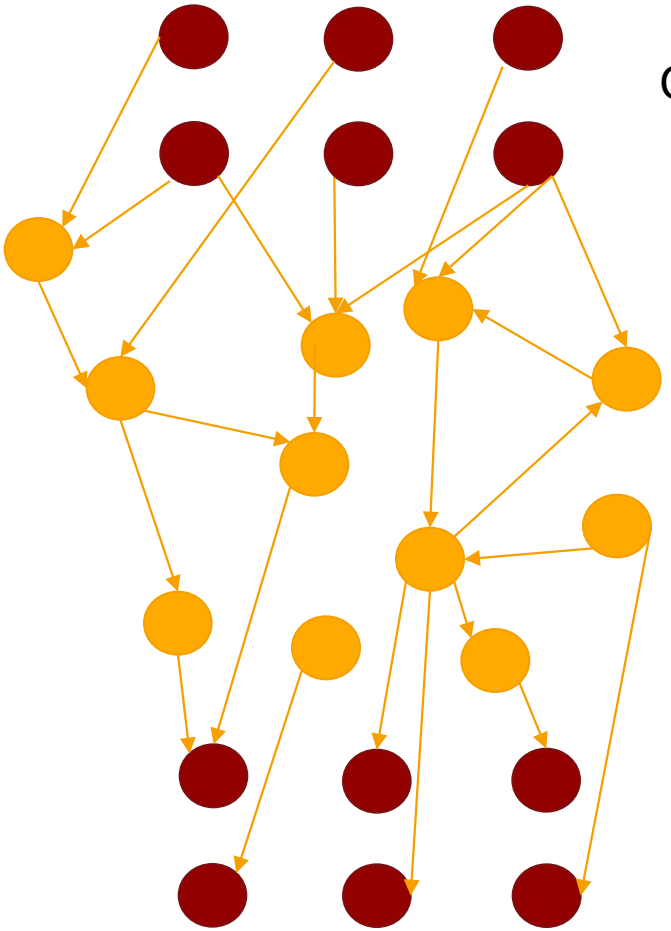
OLT(RE)²
Level 2 Fault Coverage

- Cover all the edges (PIPs) of the Graph



- This step verify that all the PIPs are stuck-off free

OLT(RE)²
Level 3 Fault Coverage



OutPins

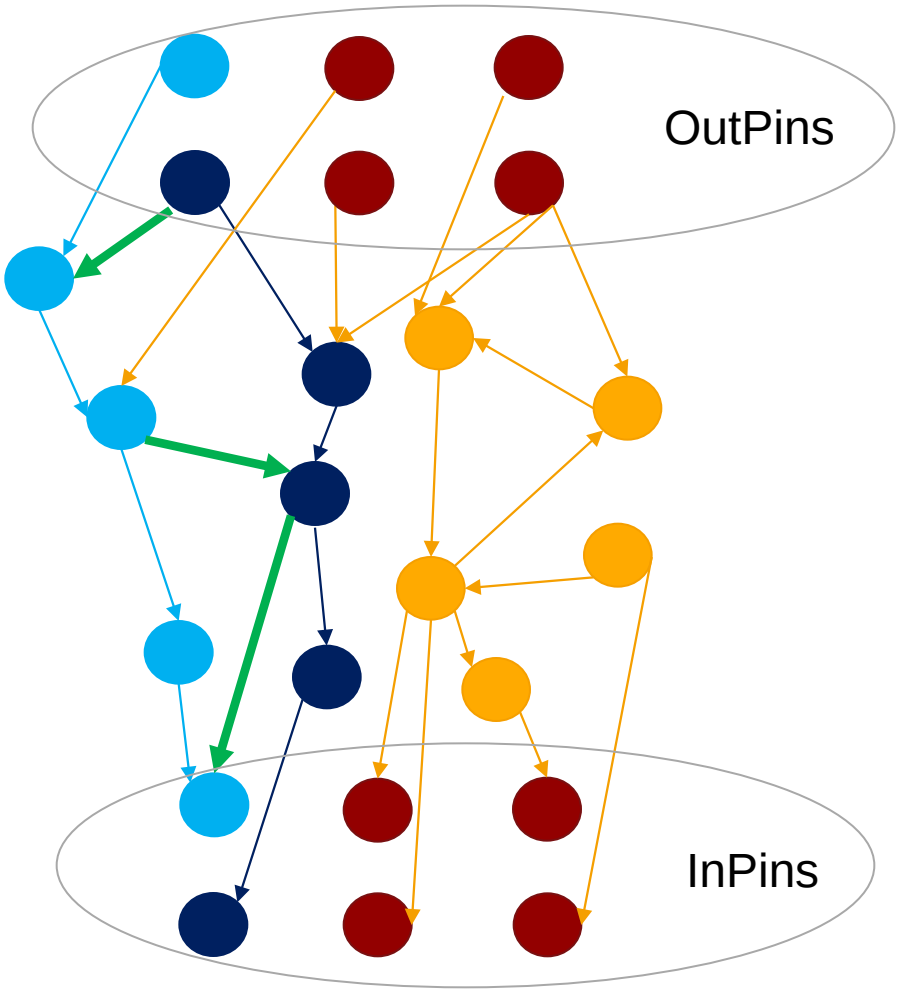
InPins

Nodes: Physical Wires

Arcs: PIP

OLT(RE)²
Level 3 Fault Coverage

- Test of Stuck-on.



Route of NUT 1

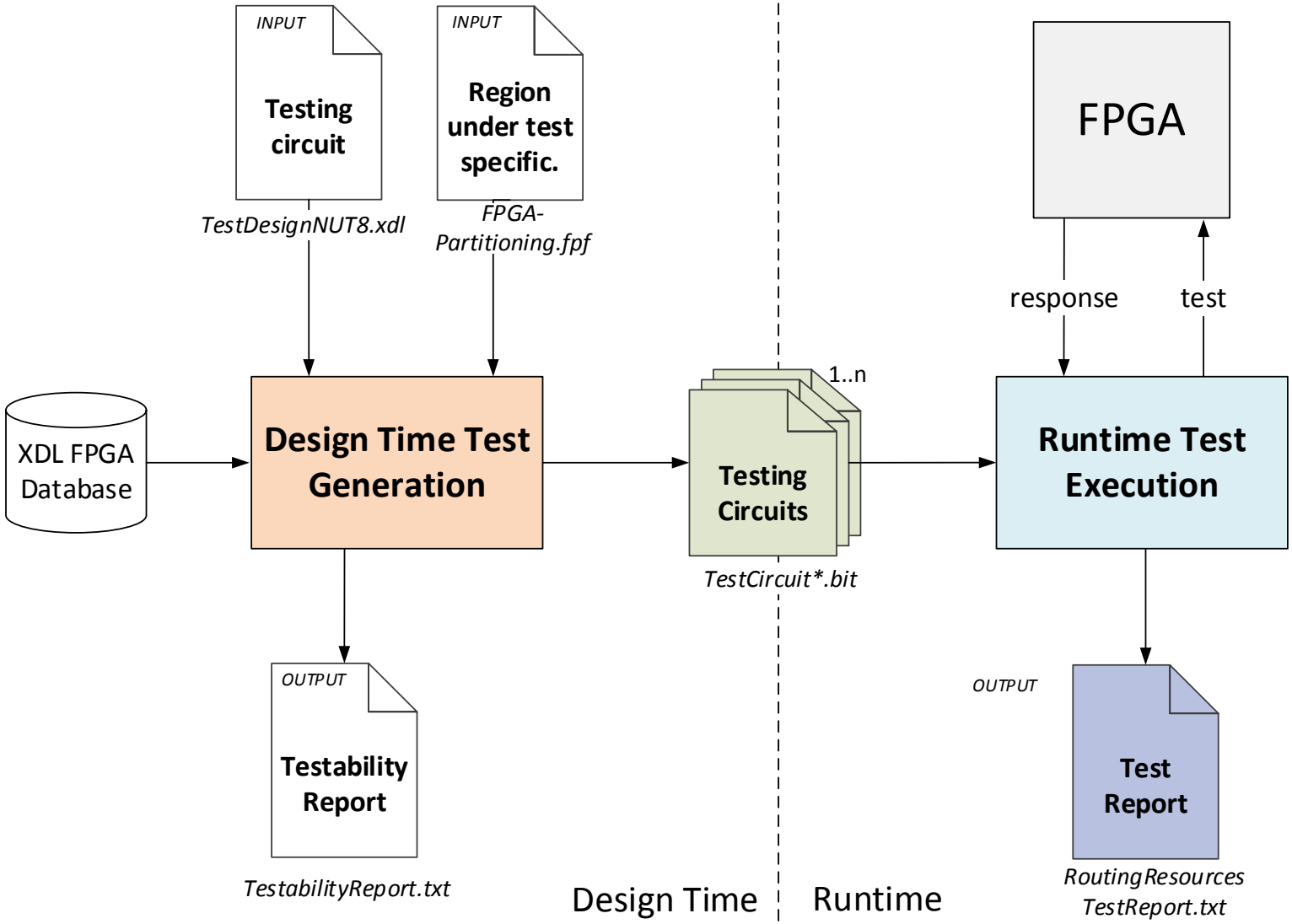
Route of NUT 2

PIPs that create a short among the two routed nets

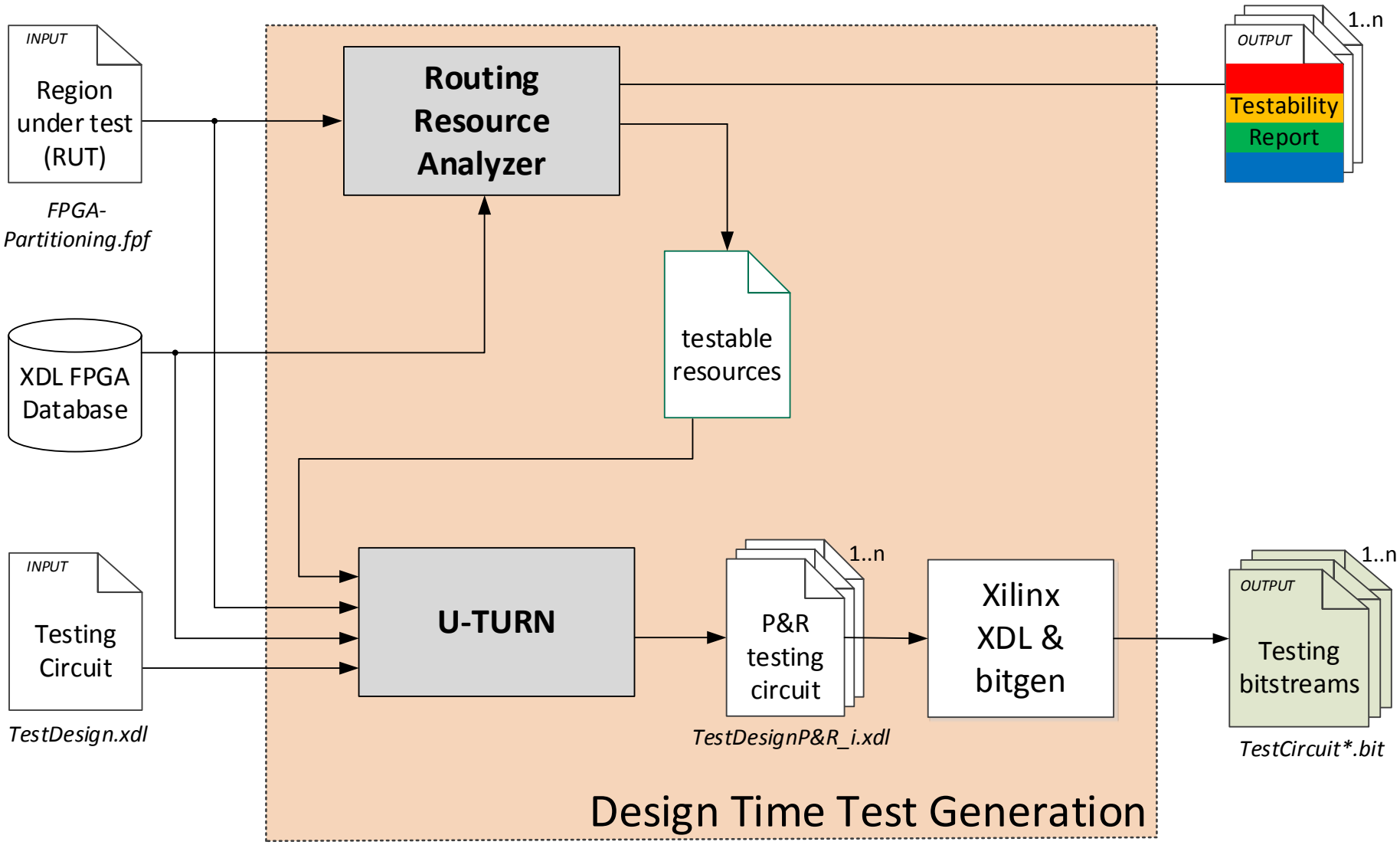
This step verify that green PIPs are stuck-on free

OLT(RE)²

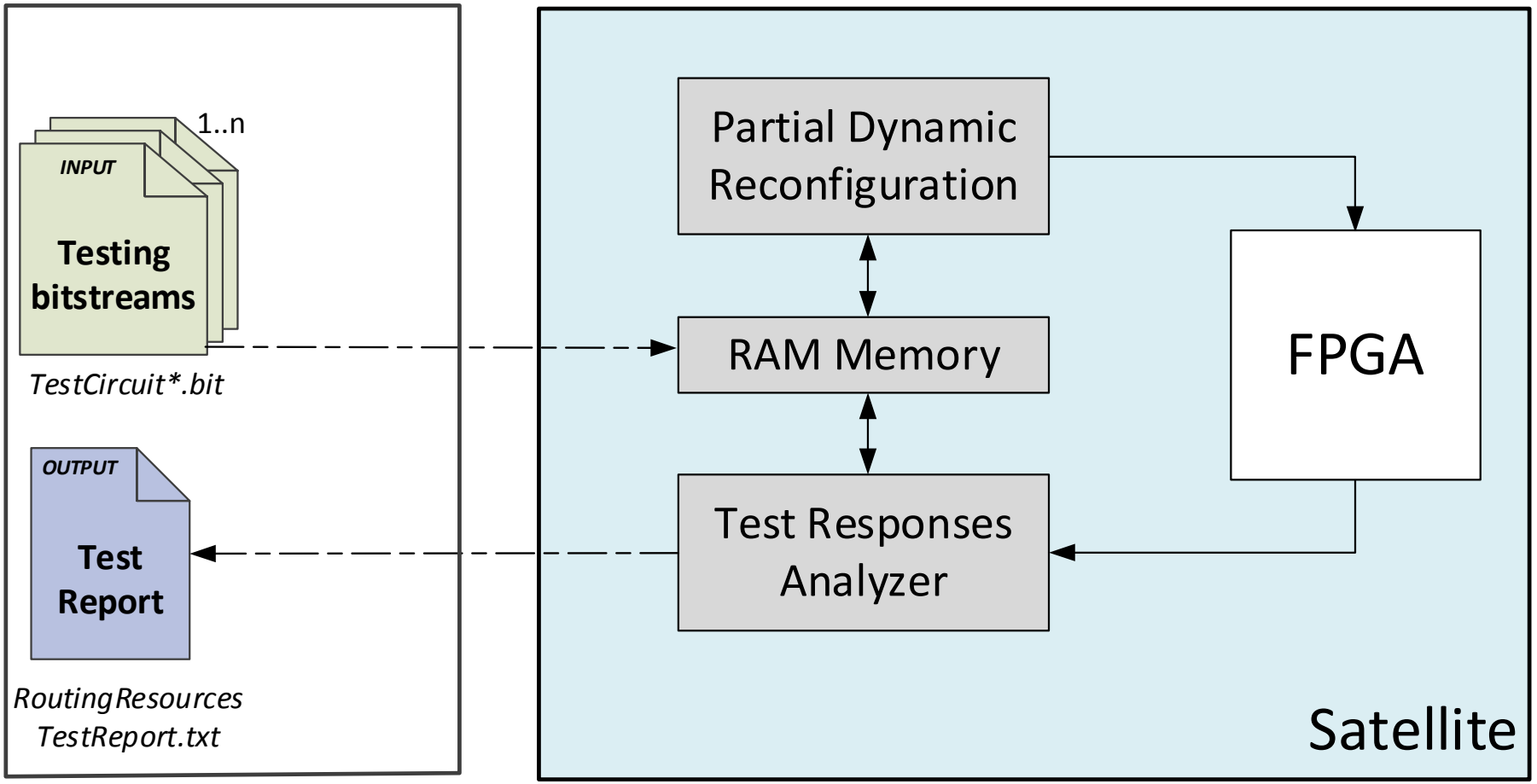
The Compleate Flow



OLT(RE)²
Design Time Flow



OLT(RE)²
Runtime Flow



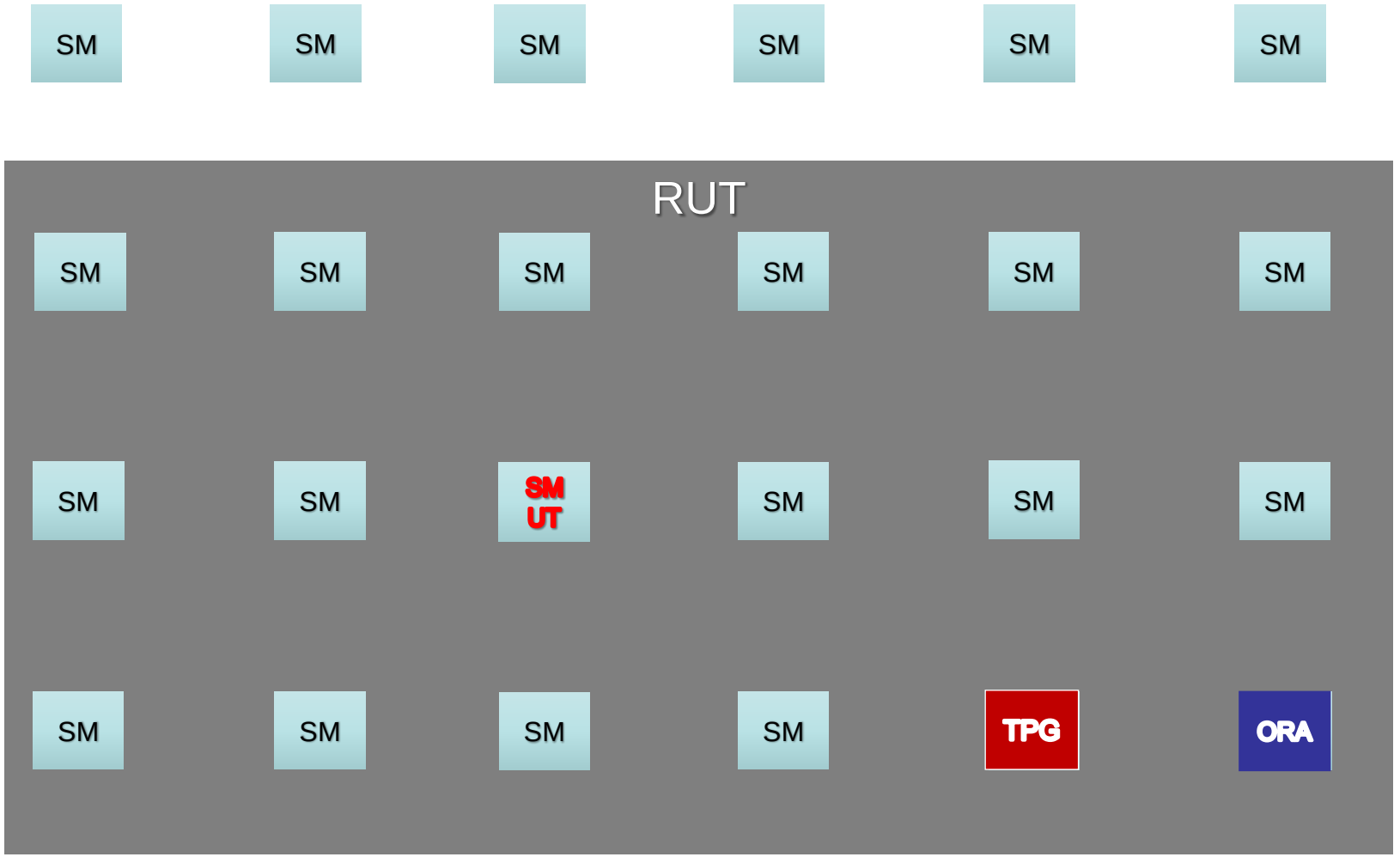
OLT(RE)²

U-TURN Routing Algorithm

- **General Goal:**
  - Maximize the number of physical wires used for the net under test (NUT)
- **Idea:**
  - Increment number of wires in the NUT by leaving and returning to one switch matrix under test (SMUT)

OLT(RE)²

U-TURN Routing Algorithm



SM(switch matrix)

SMUT(switch matrix under test)

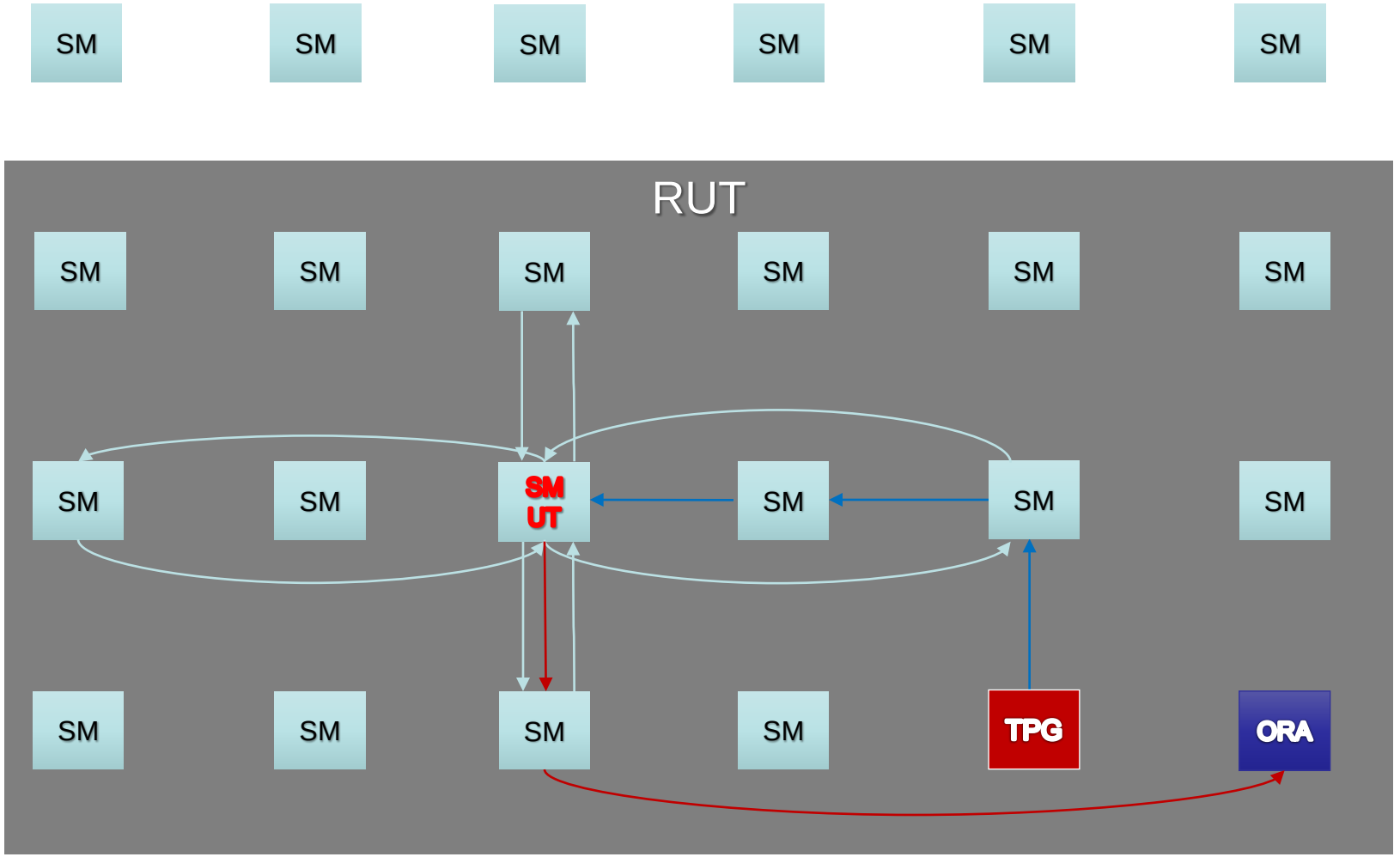
RUT (region under test)

TPG (test pattern generator)

ORA (output response analyzer)

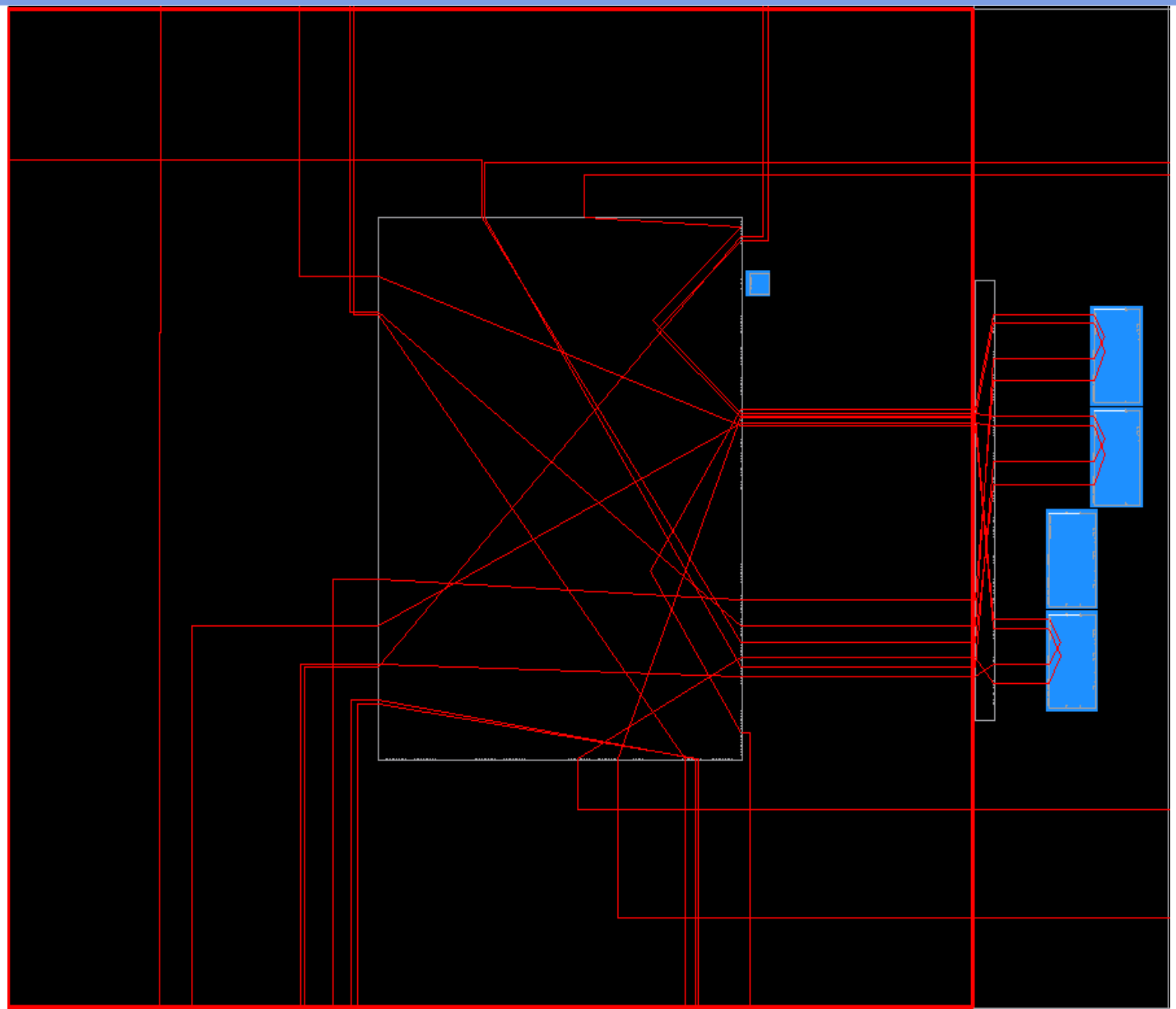
OLT(RE)²

U-TURN Routing Algorithm



OLT(RE)²

U-TURN Routing Algorithm



Virtex4 FX12
target: **INT_X23Y40**

PIPs in NUT
105

physical wires in NUT
105

- Motivation
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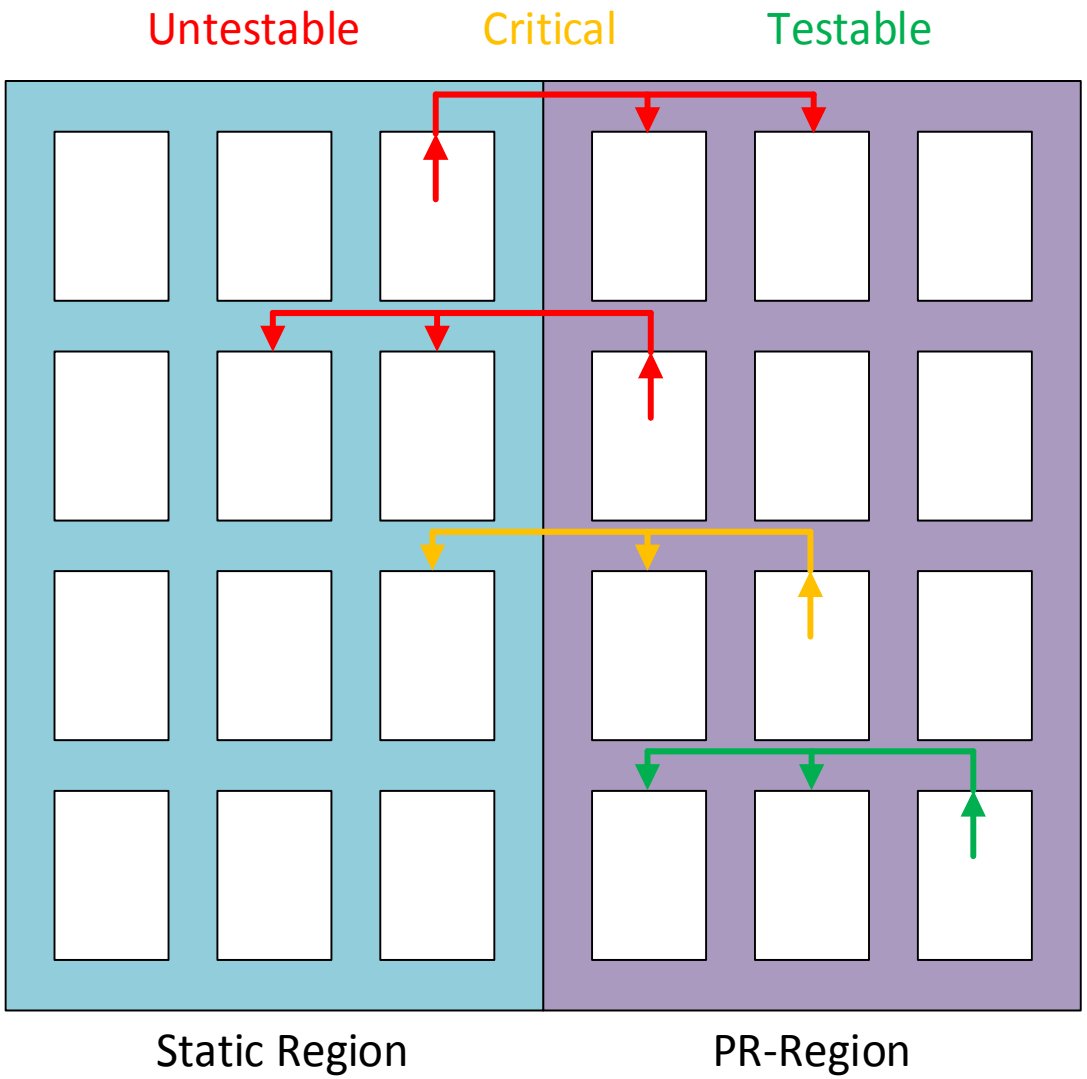
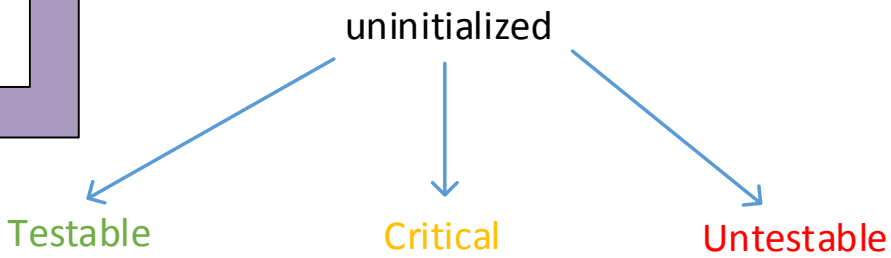
Results

Routing Resource Categorization

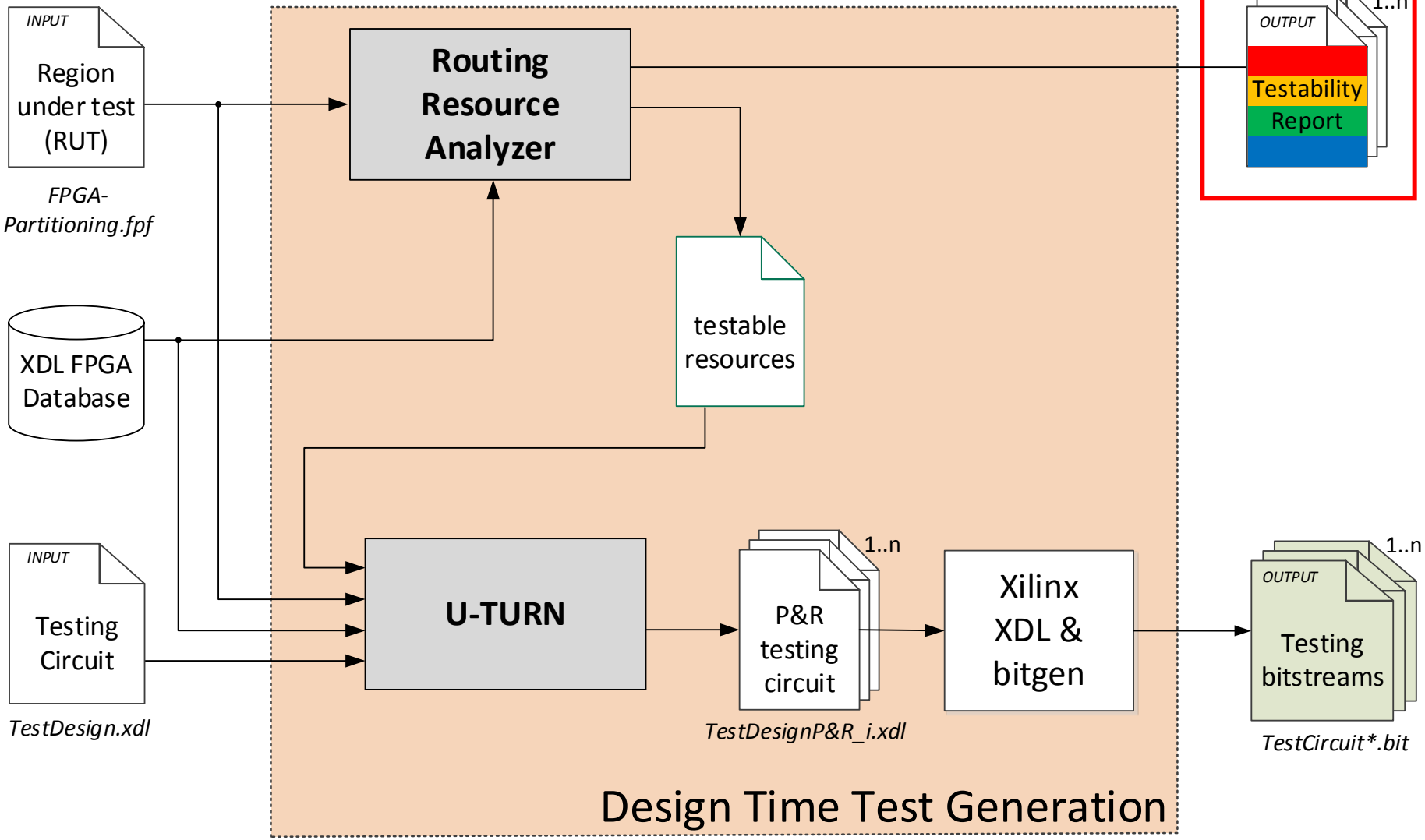


- Initialization of the wire according to the **Inwire** and **Outwire** position



Results

Routing Resource Analysis



Results

Routing Resource Analysis

Routing resource report

Physical wires testability report

Region : Rec0_a
[North 19, South 35, West 16, East 30]

Physical Wires: 81581
Testable physical wires: 39777 (48.75%)
Critical physical wires: 3398 (4.16%)
Untestable physical wires: 7170 (8.78%)
Unsupported physical wires: 31236 (38.28%)

Tile: INT @ [49,26]

Wire: BEST_LOGIC_OUTS0	Testable
Wire: BYP_INT_B5	Testable
Wire: BYP_INT_B7	Testable
Wire: E2BEG6	Testable
…	
Wire: LH0	Critical [26,5],[26,11]
Wire: LV0	Critical Base1
…	
Wire: LH12	Untestable [26,11]
Wire: LV12	Untestable Base0
…	

PIPs testability report

Region : Rec0_a
[North 19, South 35, West 16, East 30]

PIPs: 831057
Testable PIPs: 456783 (54.96%)
Critical PIPs: 78635 (9.46%)
Untestable PIPs: 104876 (12.61%)
Unsupported PIPs: 190763 (22.95%)

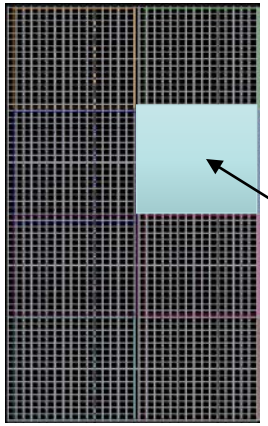
Tile : INT @ [49,26]
Critical Resources
Wire: LH0 [26,5],[26,11]
Critical OutPIPs (18)
E2END2 -> LH0
E2MID1 -> LH0
Critical InPIPs (11)
LH0 -> E6BEG2
LH0 -> E6BEG3
…
Untestable Resources
Unsupported Resources
…

Results

Routing Resource Analysis

Fault coverage heat map (Test Circuit Independent)

INT	CLB	INT	CLB	INT	CLB	INT	CLB	INT	DSP	INT	CLB	INT	CLB	INT	CLB	INT	CLB	INT	BRAM	INT	CLB	INT	CLB	INT	CLB	INT	CLB	INT	IOIS	R_T
27	87	40	98	47	98	48	98	46		48	98	52	98	52	98	52	98	41		52	98	52	98	52	98	52	98	48	58	77
42	100	59	100	68	100	70	100	68		70	100	74	100	74	100	74	100	66		74	100	74	100	74	100	74	100	69	58	100
50	100	68	100	78	100	80	100	79		80	100	84	100	84	100	84	100	77		84	100	84	100	84	100	84	100	79	58	100
52	100	70	100	81	100	83	100	82	100	83	100	88	100	88	100	88	100	74	100	88	100	88	100	88	100	88	100	83	58	100
52	100	70	100	81	100	83	100	79		83	100	88	100	88	100	88	100	72		88	100	88	100	88	100	88	100	83	58	100
52	100	70	100	81	100	83	100	81		83	100	88	100	88	100	88	100	79		88	100	88	100	88	100	88	100	83	58	100
55	100	74	100	85	100	87	100	86		87	100	92	100	92	100	92	100	85		92	100	92	100	93	100	93	100	88	58	100
56	100	74	100	85	100	88	100	87	100	88	100	93	100	93	100	93	100	79	100	93	100	93	100	94	100	94	100	89	60	100
0		0		0		0		0		0		0		0		0		0		0		0		0		0		0	31	
56	100	74	100	85	100	88	100	84		88	100	93	100	93	100	93	100	77		93	100	93	100	94	100	94	100	91	63	100
56	100	74	100	85	100	87	100	85		87	100	93	100	93	100	93	100	84		93	100	93	100	93	100	93	100	88	60	100
52	100	70	100	81	100	83	100	82		83	100	88	100	88	100	88	100	80		88	100	88	100	88	100	88	100	83	58	100
52	100	70	100	81	100	83	100	82	100	83	100	88	100	88	100	88	100	74	100	88	100	88	100	88	100	88	100	83	58	100
52	100	70	100	81	100	83	100	79		83	100	88	100	88	100	88	100	71		88	100	88	100	88	100	88	100	83	58	100
50	100	68	100	78	100	80	100	78		80	100	84	100	84	100	84	100	75		84	100	84	100	84	100	84	100	79	58	100
42	100	60	100	69	100	70	100	70		70	100	74	100	74	100	74	100	68		74	100	74	100	75	100	75	100	70	58	100
28	88	41	98	48	98	49	98	49	100	49	98	53	98	53	98	53	98	45	100	53	98	53	98	53	98	54	98	51	58	96



Virtex-4 FX12

Total TCI physical wires: 81,581
 # Testable TCI : 71,013 (87%)
Critical: 3,398 (4%)
Untestable: 7,170 (9%)

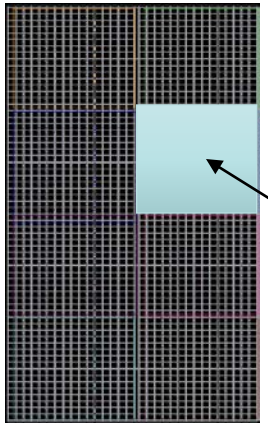
Total TCI PIPs: 831,057
 # Testable TCI: 647,546 (78%)
Critical: 78,635 (9%)
Untestable: 104,876 (13%)

Results

Routing Resource Analysis

Fault coverage heat map (Test Circuit Dependent)

INT	CLB	INT	CLB	INT	CLB	INT	CLB	INT	DSP	INT	CLB	INT	CLB	INT	CLB	INT	CLB	INT	BRAM	INT	CLB	INT	CLB	INT	CLB	INT	CLB	INT	IOIS	R_T
78	55	78	48	81	48	77	48	25		78	48	82	48	82	48	78	48	34		79	48	82	48	82	48	78	48	28	0	95
78	48	78	48	80	48	76	48	24		76	48	82	48	82	48	77	48	30		77	48	82	48	82	48	77	48	27	0	93
81	48	80	48	82	48	78	48	27		78	48	83	48	83	48	79	48	33		79	48	83	48	83	48	79	48	29	0	93
81	48	81	48	83	48	79	48	29	0	78	48	84	48	84	48	80	48	38	0	80	48	84	48	84	48	80	48	32	0	93
81	48	81	48	83	48	79	48	30		79	48	84	48	84	48	80	48	40		80	48	84	48	84	48	80	48	32	0	93
81	48	81	48	83	48	79	48	30		79	48	84	48	84	48	80	48	36		80	48	84	48	84	48	80	48	32	0	93
82	48	82	48	83	48	80	48	32		79	48	85	48	85	48	81	48	38		81	48	85	48	85	48	81	48	35	0	93
82	48	82	48	83	48	80	48	32	0	79	48	85	48	85	48	81	48	41	0	81	48	85	48	85	48	81	48	35	0	93
																													0	
82	48	82	48	83	48	80	48	33		79	48	85	48	85	48	81	48	43		81	48	85	48	85	48	81	48	34	0	93
82	48	82	48	83	48	80	48	33		79	48	85	48	85	48	81	48	39		81	48	85	48	85	48	81	48	35	0	93
81	48	81	48	83	48	79	48	29		79	48	84	48	84	48	80	48	35		80	48	84	48	84	48	80	48	32	0	93
81	48	81	48	83	48	79	48	29	0	79	48	84	48	84	48	80	48	38	0	80	48	84	48	84	48	80	48	32	0	93
81	48	81	48	83	48	79	48	30		78	48	84	48	84	48	80	48	39		80	48	84	48	84	48	80	48	32	0	93
81	48	80	48	82	48	78	48	28		78	48	83	48	83	48	79	48	33		79	48	83	48	83	48	79	48	29	0	93
79	48	78	48	81	48	76	48	24		76	48	82	48	82	48	77	48	29		77	48	82	48	82	48	77	48	27	0	93
80	54	79	48	81	48	78	48	24	0	78	48	83	48	83	48	79	48	33	0	80	48	83	48	83	48	79	48	28	0	96



Region Under Test

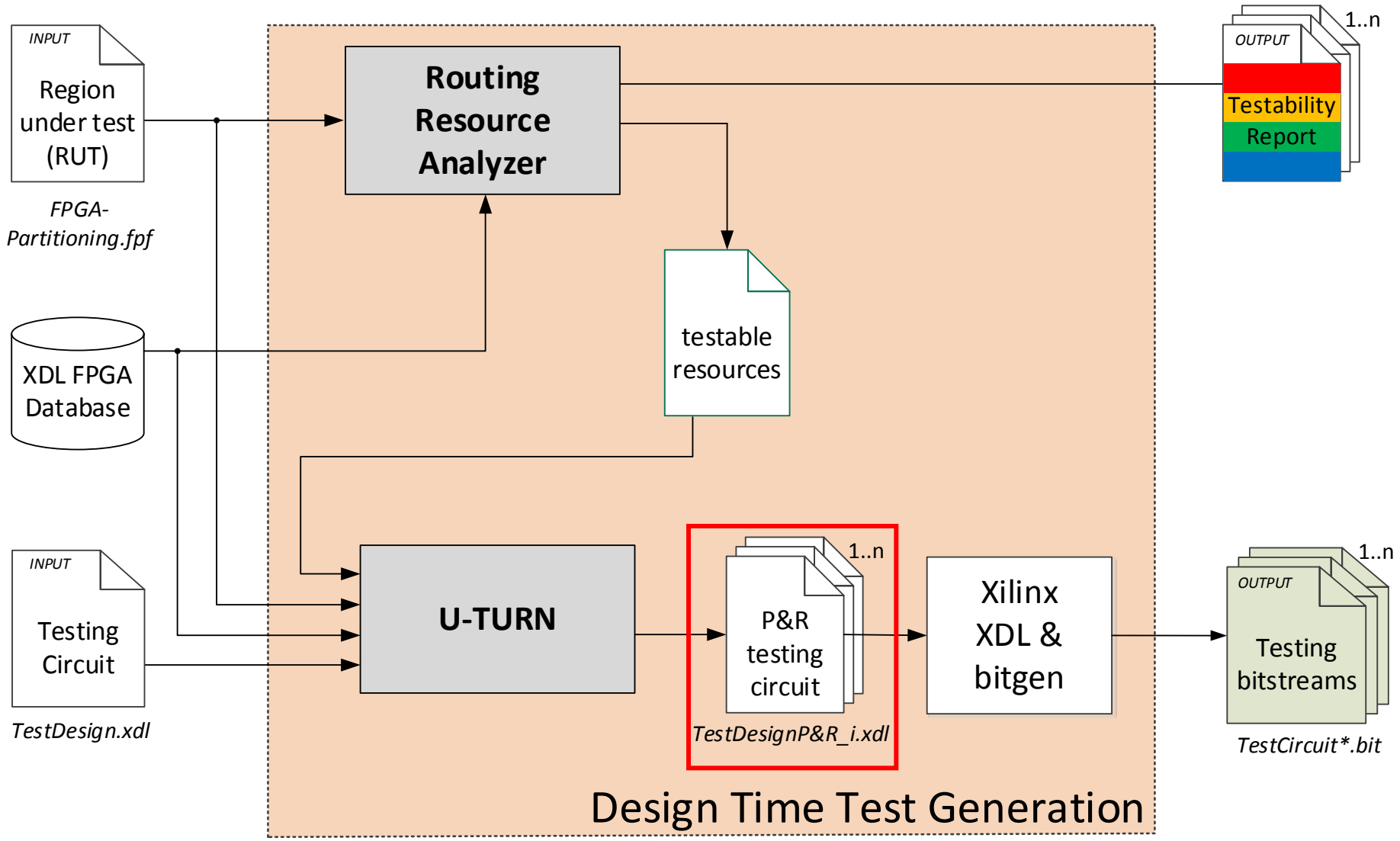
Virtex-4 FX12

Total TCI physical wires: 81,581
Testable TCI Physical wires: 71,013
 # Testable TCD: 39,777 (56%)
 # Unsupported: 31,225 (44%)

Total TCI PIPs: 831,057
Testable TCI PIPs: 647,546
 # Testable TCD: 456,783 (71%)
 # Unsupported: 190,664 (29%)

Results

Routing Resource Analysis



Results

Testing Circuit Evaluation

Routing resources fault coverage

Xilinx Virtex-4 FX100

Test design	Testing circuits	testable wires			testable PIPs				
		available	L1: stuck-at-0/1		available	L2: stuck-off		L3: stuck-on	
	#	#	#	[%]	#	#	[%]	#	[%]
NUT6	1,351	***111,179***	110,327	99.23	***1,317,736***	301,044	22.85	102,248	7.76
NUT8	846	***111,179***	110,167	99.09	***1,317,736***	315,883	23.97	181,952	13.81

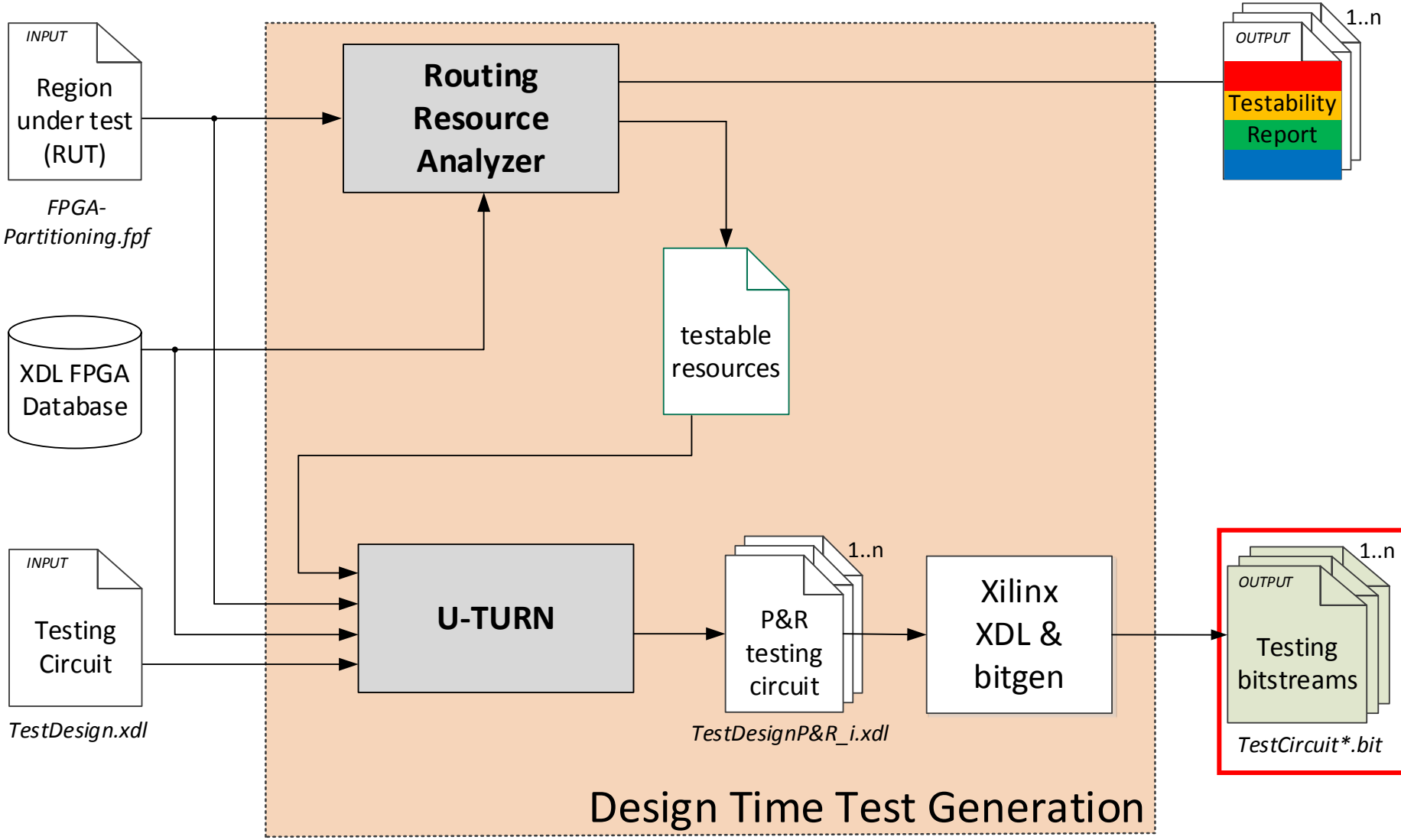
OLT(RE)² execution time and size of the testing circuits

Step	Testing circuits	Total		One testing circuit	
- Test design	#	Time	Size	Time	Size
		[h:m::s]	[MB]	[s]	[KB]
Routing Resource Analyzer		00:01::15	25.7	-	-
U-TURN					
- NUT6	1,351	03:07::35	72.0	8.33	53.29
- NUT8	846	02:20::05	60.3	9.93	71.28

Hardware: Intel i7-4770K @ 3.5 GHz with 16 GB DDR3 @ 1.333 GHz; OS: Xubuntu 14.04 (64bit)

Results

Routing Resource Analysis



Results

Testing Circuit Evaluation

Time and file size analysis

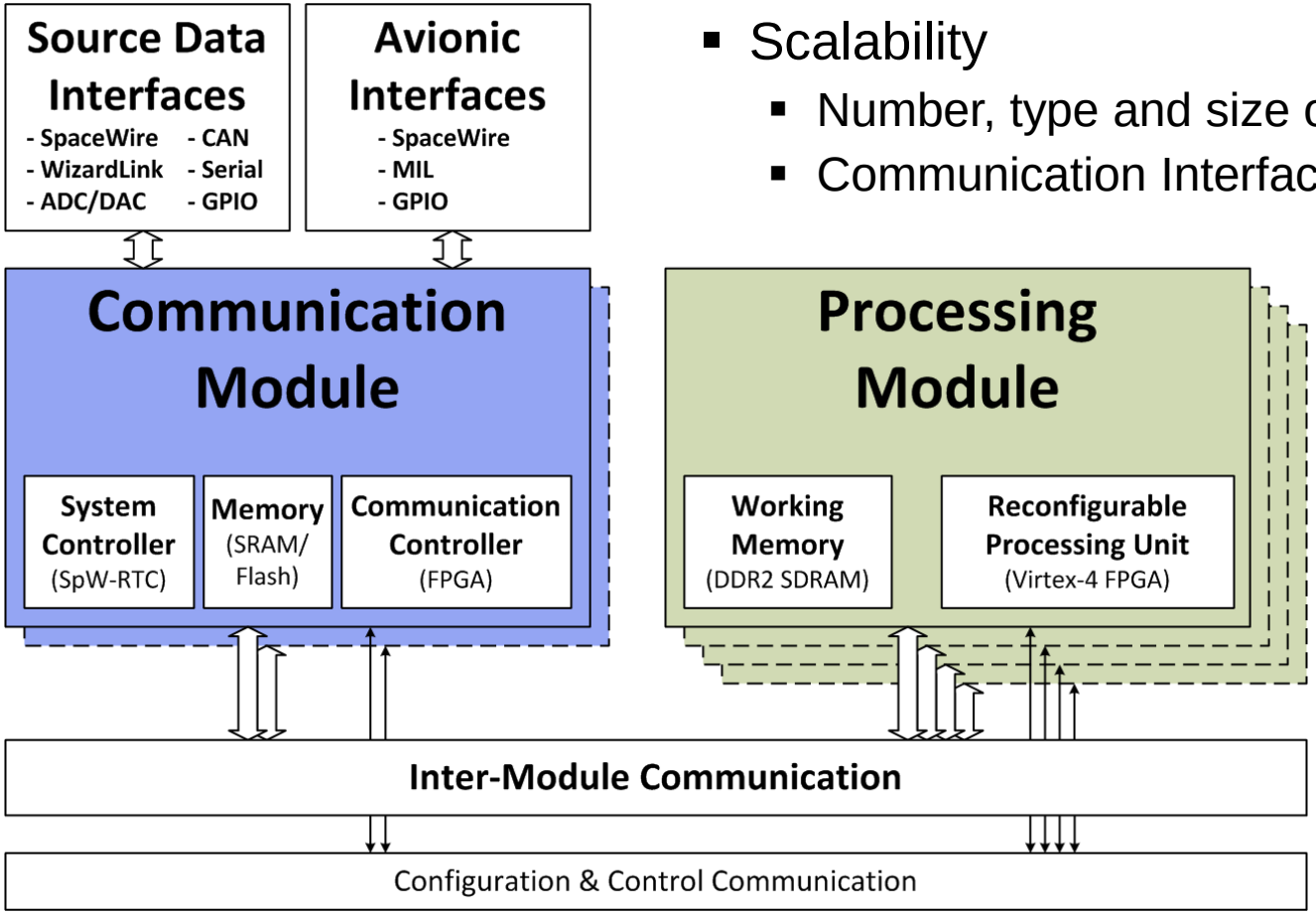
Step		**Total**		**One testing circuit**	
- **Test design**	Testing circuits	Time	Size	Time	Size
	#	[h:m::s]	[MB]	[s]	[KB]
Create testing circuit design|hard macros files					
- NUT6	1,351	00:22::01	17.0	0.98	12.58
- NUT8	846	00:16::19	13.5	0.96	15.96
Create testing circuit bitstreams					
- NUT6	1,351	02:28::36	50.5	6.60	37.38
- NUT8	846	01:35::00	35.9	6.74	42.43

Hardware: Intel i7-2600 @ 3.4 GHz with 12 GB DDR3 @ 1.333 GHz
Software/OS: Xilinx ISE 14.7, Win7 SP1 64bit
6 threads

Results

Testing Circuit Evaluation

DRPM – FPGAs for satellite payload processing



- Scalability
  - Number, type and size of FPGAs
  - Communication Interfaces

Partners

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TWT

POLITECNICO DI TORINO

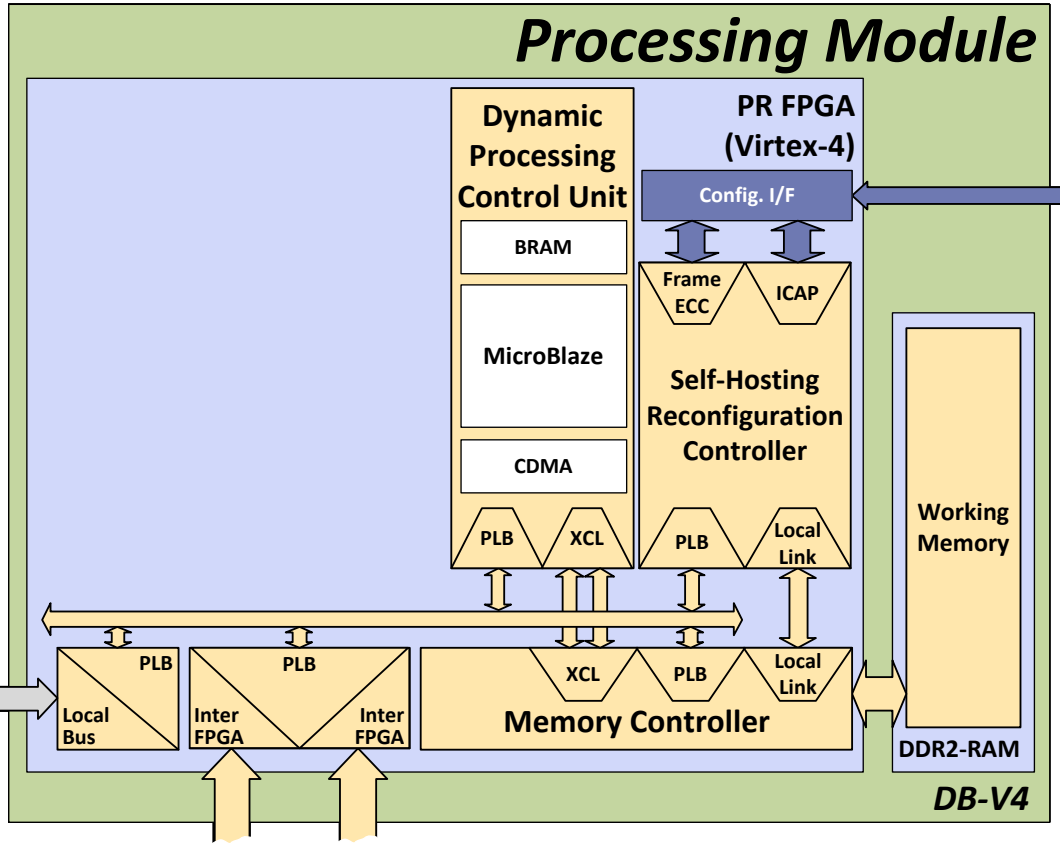
SWISS SPACE TECHNOLOGY
PRECISION ELECTRONICS FOR SPACE FLIGHT

DRPM – Dynamically **R**econfigurable **P**rocessing **M**odule

Results

Testing Circuit Evaluation

Testing platform DRPM



- PR FPGA (XC4VFX100)
- 4 GByte DDR2 SDRAM

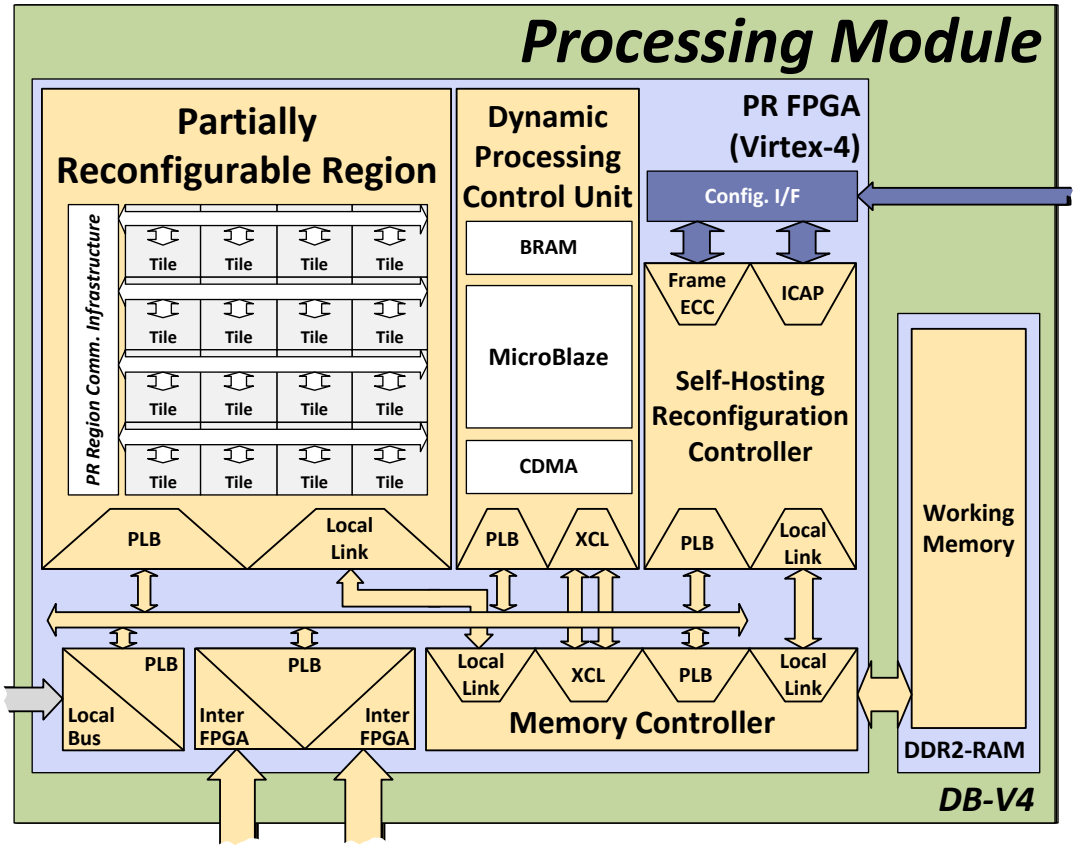
Static Region

- Multi Port Memory Controller
- Communication
  - PLB, Local Link, LocalBus
- Self-Hosting Reconf. controller
  - Performs partial reconfig., readback (ICAP) and scrubbing (FrameECC)
- Dynamic Proces. Control Unit
  - Configures/maintains IP cores

Results

Testing Circuit Evaluation

Testing platform DRPM



- PR FPGA (XC4VFX100)
- 4 GByte DDR2 SDRAM

Partially Reconfigurable Region

- Tiled PR-region
  - Region under test

Results
Testing Circuit Evaluation

Performed Tests

1. *Component test*

- Test regarding open faults: influence of opens for all (sub)components of the testing circuit

⇒ Verification of the testing circuits, find weak points of the test design

2. *Routing resources test*

- Normal operating mode

⇒ Verification that the routing resources of an area of the FPGA are free of permanent errors

3. *Fault injection test*

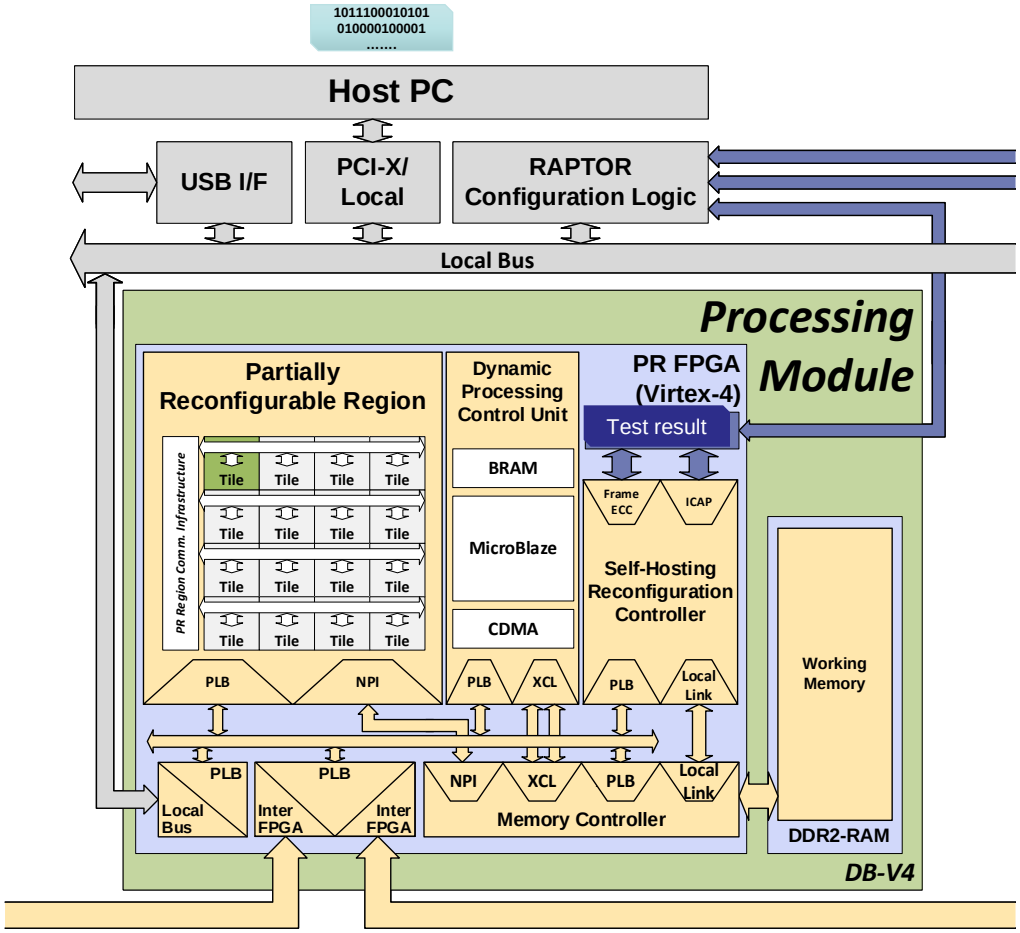
- Test of stuck-at-0/1 faults within one NUT

⇒ Verification of the fault detection capability of the test designs

Results

Testing Circuit Evaluation

Hardware Test Design Flow



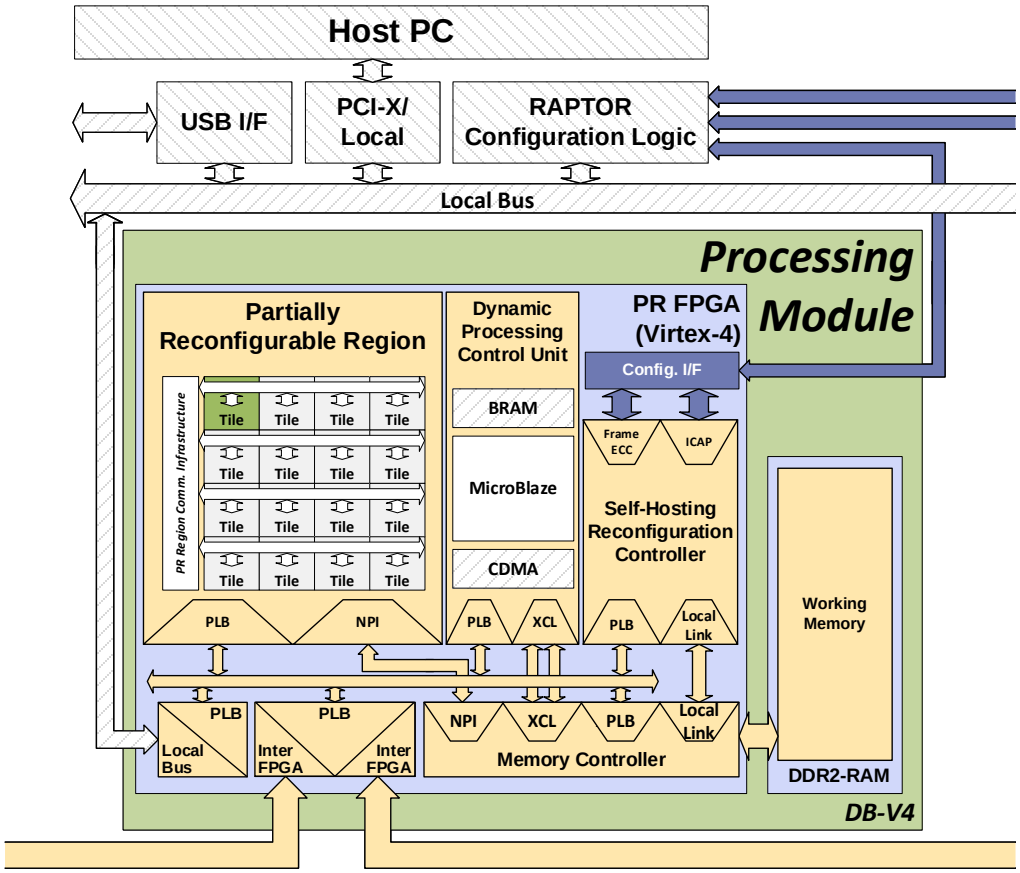
Performed Tasks

1. (External) transfer of a partial bitstream
2. (Internal) transfer and partial reconfiguration
3. Execution of the testing circuit
4. Readback of distr. memory with results
5. Transfer of the result to the host PC

Results

Testing Circuit Evaluation

Hardware Test Design Flow



Performed Tasks

1. (External) transfer of ***all*** partial bitstreams
2. (Internal) transfer and partial reconfigurations
3. Execution of the testing circuits
4. Readback of distr. memory with results
5. Transfer of the result to the host PC

Results

Testing Circuit Evaluation

The test result can be divided into 3 categories

1. *TNS: test not started* in case the injected fault prevents the test circuit to operate at all
2. *TSFD: test started and fault detected* in case the test correctly started and a fault has been detected
3. *TSFND: test started and fault not detected* in case the test correctly started and a fault has not been detected

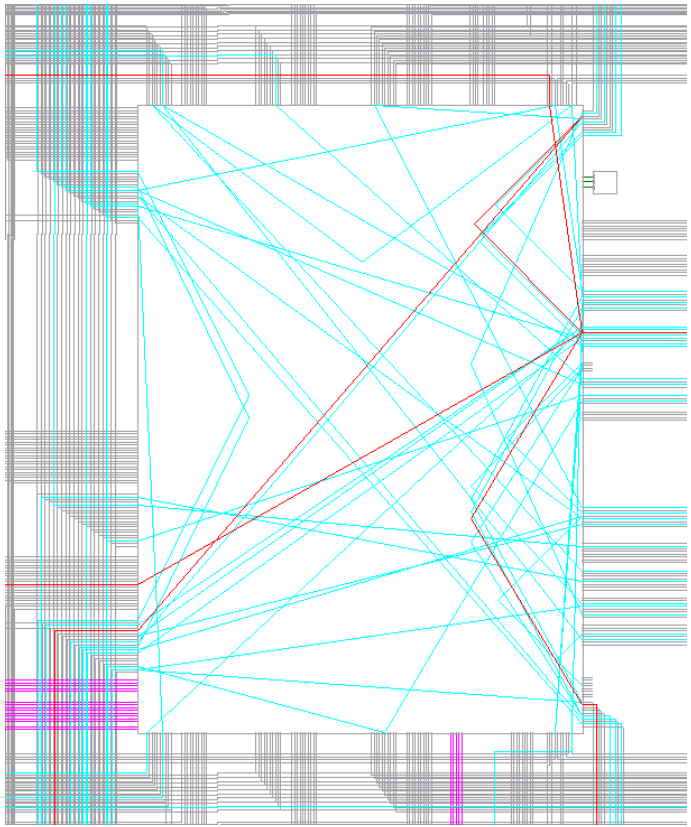
Results

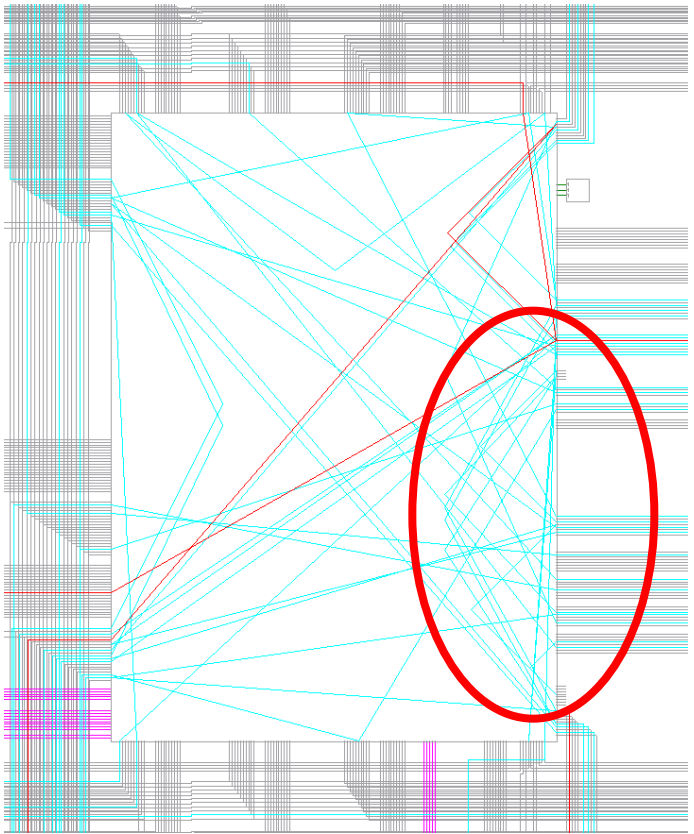
Testing Circuit Evaluation

1. Component test

- Influence of opens for all (sub) components of the test design
- A net consists of wires connected by PIPs, where each of these PIPs can be seen as a crucial element

=> Remove important PIPs for all nets of the test design





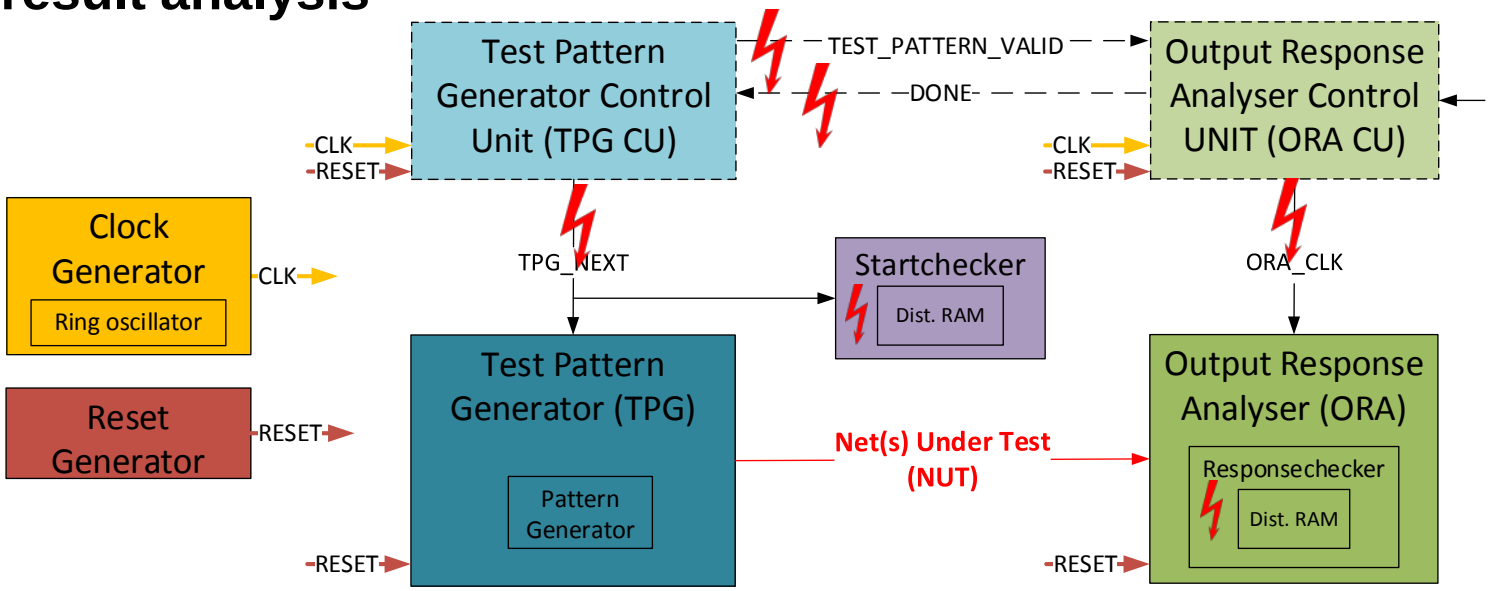
Results

Testing Circuit Evaluation

1. Component test

Test designs	Injected faults	positive results				negative results	
		TNS_p	$TSFD_p$	Total		$TSFND_n$	
	#	#	#	#	%	#	%
NUT6	36	11	18	29	80.56	7	19.44
NUT8	43	10	26	36	83.72	7	16.28

Test result analysis



1. An error in controlling signals results in a blocking condition
2. An error in connections to the result DRAMs indicates a malfunctioning

Results

Testing Circuit Evaluation

2. Routing resources test

Test designs		negative results				positive results	
		TNS_n		$TSFD_n$		$TSFND_p$	
	#	#	%	#	%	#	%
NUT6	1,351	0	0.00	0	0.00	1,351	100.00
NUT8	846	0	0.00	0	0.00	846	100.00

Test result and performance analysis

- All testing circuits are executed and no faults are detected

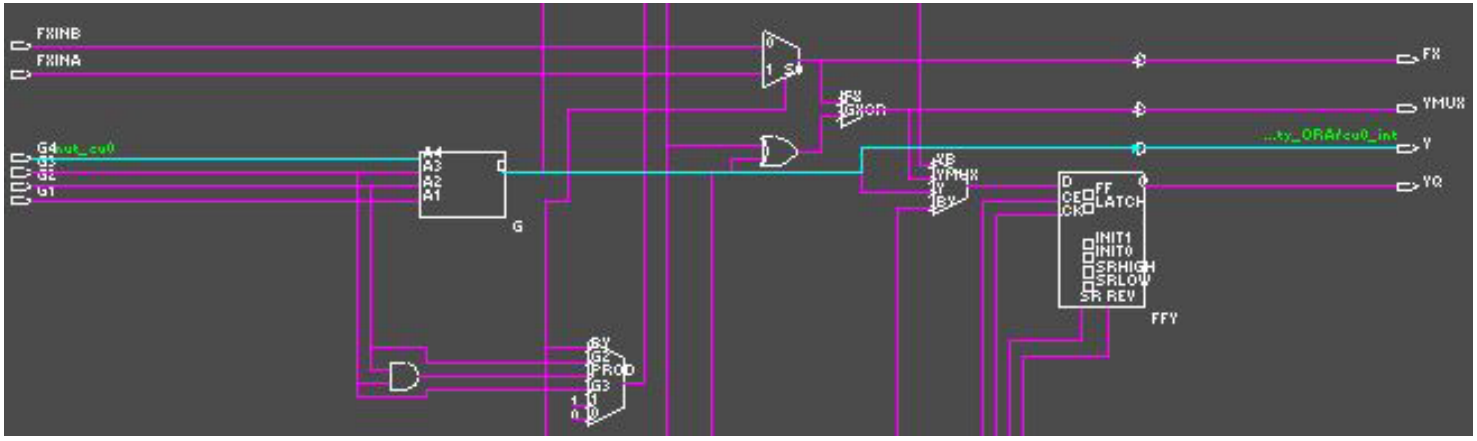
Test design	Testing circuits	Total time	One complete hardware test run		
			bitstream transfer	result analysis	complete test run
	#	[s:ms]	[ms::us]	[ms::us]	[ms::us]
NUT6	1,351	37:732	2::530	1::331	27::280
NUT8	846	26:118	2::281	1::373	30::281

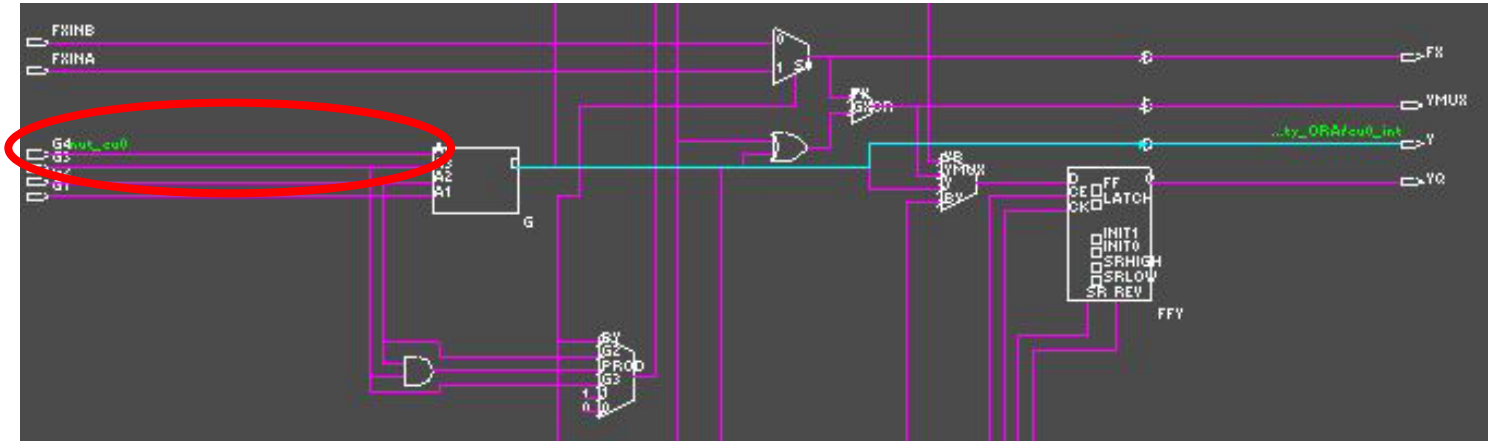
Results

Testing Circuit Evaluation

3. Fault injection test

- Verify the fault detection capability of the test designs
- Fault injection by changing the content of a source LUTs for one NUT





Results

Testing Circuit Evaluation

3. Fault injection test

Test designs		positive results				negative results	
		TNS_p		$TSFD_p$		$TSFND_n$	
	#	#	%	#	%	#	%
NUT6	1,351	0	0.00	1,351	100.00	0	0.00
NUT8	846	0	0.00	846	100.00	0	0.00

Test result analysis

- ***100%*** of the injected faults are detected

Conclusion & Further developments

Conclusion

Development of coarse-grained test designs for perm. fault detection

- Independent test designs (NUT6|8) following a parity-based approach
- Small FPGA resource footprint (~22 slices on a Xilinx Virtex-4)

Categorization of routing resources

- Reports and heat maps of testable, untestable, critical and unsup. resources

Modelling of permanent faults

- Classification by fault detection effort (level 1 to level 3)

Routing algorithm U-TURN

- Maximize the number of routing resources used for the net under test

Hardware verification of the fault detection capability of the test designs

- Test of stuck-at-0/1 of the physical wires and diagnosing on the DRPM

=> **100%** of the stuck-at-0/1 faults are detected by the testing circuits

Conclusion & Further developments

Further developments

Fine-grained test designs & analysis

- Explicitly identify the faulty routing resources
- Create patching hard macros to exclude faulty routing resources to prevent further usage

Development of further coarse-grained test design

- Support of BRAM and DSP components to increase the fault coverage of the routing resources

Reduce number of testing circuits

- Exploit homogeneity of the FPGA architecture to use bitstream relocation

Further hardware tests

- Test already (by software) supported Xilinx FPGA families

Innovation Triangle Initiative

esa

Thank you for your attention.

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Politecnico di Torino

Testing Circuit Evaluation
Device utilisation

Test designs	LUTs			FFs	Slices
	Logic	DRAM	Shift register		
NUT6	23	3	1	11	19
NUT8	35	3	1	11	24

NUT6	LUTs			FFs
components	Logic	DRAM	Shift register	
ORA	2	2	0	2
ORA CU	2	0	0	0
Ring Oscillator	6	0	0	1
StartChecker	1	1	0	0
ResetGenerator	0	0	1	0
TPG	10	0	0	4
TPG CU	2	0	0	4
TOTAL	23	3	1	11

NUT8	LUTs			FFs
components	Logic	DRAM	Shift register	
ORA	12	2	0	2
ORA CU	2	0	0	0
Ring Oscillator	6	0	0	1
StartChecker	1	1	0	0
ResetGenerator	0	0	1	0
TPG	12	0	0	4
TPG CU	2	0	0	4
TOTAL	35	3	1	11

=> Very small FPGA resource footprint

Results

Testing Circuit Evaluation

Routing resources fault coverage

Family	Device	#Testing Circuits	#PW Sa	#PIP Soff	#PIP Son	SA	SOff	SOn
Spartan-6	LX9	4,179	25,504	268,364	255,940	25,242 (98.97%)	255,771 (95.30%)	243,091 (94.97%)
Virtex-4	FX12	8,058	38,784	444,476	427,792	38,784 (100.00%)	439,074 (98.78%)	427.646 (99,97%)
	FX100	38,245	111,179	1,317,736	1,270,955	111,179 (100.00%)	1,305,778 (99.09%)	1,248,119 (98.20%)
Virtex-5	LX20T	19,562	79,425	941,323	900,205	79,225 (99.74%)	929,720 (98.76%)	887,975 (98.64%)
Virtex-6	LX130t			4,130,930	3,973,033			