COTS based computer for on board systems – System Contract

Brice Dellandrea⁽¹⁾, Guy Estaves⁽²⁾, Giorgio Magistrati⁽³⁾

- ⁽¹⁾ Thales Alenia Space, 5 Allée des Gabians, BP99, 06156 Cannes, France
- ⁽²⁾ Thales Alenia Space, 26 Av Jean François Champollion, 31100 Toulouse, France
- ⁽³⁾ European Space Agency, Keplerlaan 1, 2201 AZ Noordwijk, Netherlands

ABSTRACT

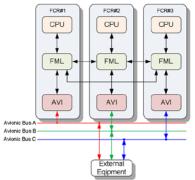
The COTS based computer (CoCs) activity has been subject to separate contracts, all synchronized by ESA: a system contract, detailed here, and three GSTP aiming at developing different solutions of COTS-based on-board computers (respectively Hi-V, Hi-R and Hi-P) and a COTS software, bringing together TAS France, ADS France, ADS Germany, TAS Italy and DTSO.

The global objective of the COTS studies was to provide demonstration of the capability to use COTS computers in space applications, considering the mandatory space qualification levels and showing the impacts in term of design, validation, qualification and procurement processes.

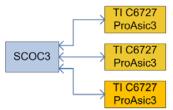
This demonstration resulted in the development of CoCs models including hardware and software components:

- The Hi-R (Highly Reliable) coping with reduced delay of outages (few seconds cumulated over 30 days),
- The Hi-V (Highly Available) coping with no outage with a better probability than 10-7 over 1 hour,
- The Hi-P (Highly Performant) coping with very high demand of CPU performance and with reduced delay of outage.

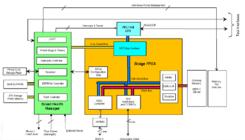
They all had a different set of input requirements which resulted in very different architectures:



Hi-V architecture (triplication & voting)



Hi-P architecture (rad-hard OBC & companion COTS DSPs)



Hi-R architecture (PowerPC with embedded SW&HW protections)

This presentation will consist in showing the system aspects of this study, from initial requirements to COTS screening & RAMS analyses, up to failure injection proces and the final evaluation using a CoCs software specially designed to add a protective layer between the application software and the COTS hardware.