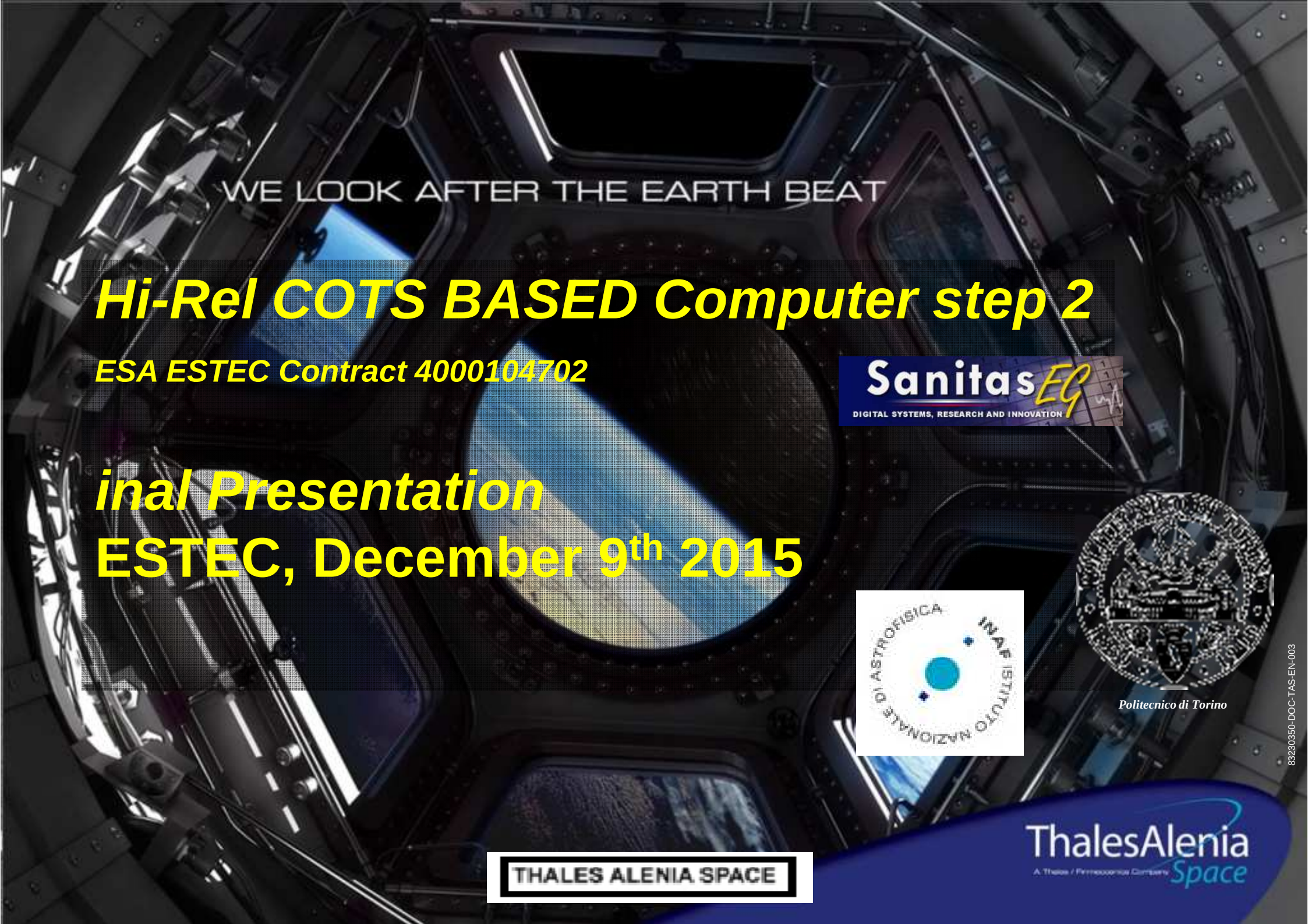


# Hi-Rel COTS BASED Computer step 2

***ESA ESTEC Contract 4000104702***

SanitasEG
DIGITAL SYSTEMS, RESEARCH AND INNOVATION

# inal Presentation

# ESTEC, December 9th 2015

INAF ISTITUTO NAZIONALE DI ASTROFISICA

*Politecnico di Torino*

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83230350-DOC-TAS-EN-003

# Summary



- 1 Hi-Rel cots experience overview TAS-I
- 2 Hi-Rel cots board overview SANITAS
- 3 Hi-Rel cots EGSE overview INAF
- 4 Hi-Rel  cots SW test overview Politecnico di Torino
- 5 Conclusions and possible future developments TAS-I

# 1- Hi-Rel cots experience overview

# Project Team



- Prime Contractor: ThalesAlenia Space (A Thales / Finmeccanica Company) — *Milan Site*

- Subcontractors:

***SME company***
- Board and Basic SW development

***Dept. of Automation and Computer Engineering of Politecnico di Torino (PoliTo):***
- Benchmark SW development

***Institute INAF-IASF Milano***
- EGSE Development

- Consultant:

***Ulisse Consortium / University of Rome 2 "Tor Vergata"***
- DDR-II ECC Development

- ESA Technical Officer: Claudio Monteleone (TEC-EDD)

- Thank to Hi-rel cots project new power PC applications for space on board computer with demanding computing needs has been developed

- The project objectives to build and test a Power PC board computer has been achieved and new applications has been developed with this board architecture



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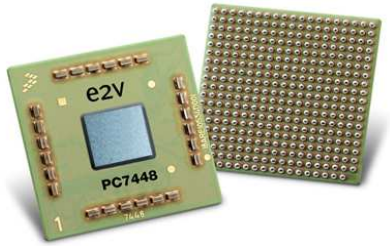
- Single board Computer to be fly in **Meteosat third Generation Payload computer** has been developed.
  - For MTG specific radiation test campaigns demonstrated adequacy of PC7448 E2V freescale versus GEO environment.
  - For MTG Technologies for cooling power dissipation of CPU based on power PC has been faced and under development

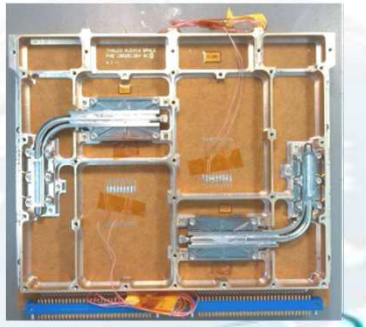
- **VISNAV** ESA project for high performance imaging processing devoted to imaging space navigation system
  - planetary landing systems
  - rovers navigation
  - Satellite & micro satellite maneuvers
  - robotics

# SBC single board Computer based on Power PC7448 for MTG



- ✓ **Main features:**
  - CPU: PPC 7448 1GHz 2.3 Dhrystone MIPs/MHz
  - Dual Boot ( on flash)
  - RAM: 1Gbyte RSE (64+16)
  - EEPROM: 512Kx16 +8 (EDAC code 16+8)
  - FLASH: 8M16
  - 6xSpiceWire: 200Mbps/each
  - Mil-BUS1553B
  - GPIO:
    - 24 output
    - 32 input
    - 2x16 PWM
  - Jtag/COP for emulation
  - Test interface
  - Power demand: 16W typical
  - Package: BGA 360 (assembly qualified)
  - Cooling: Heat pipe
  - TID: 110kRad @ LDR
  - SEE: tested @ 15MeV 20Ne, 40Ar, 84Kr, 129Xe



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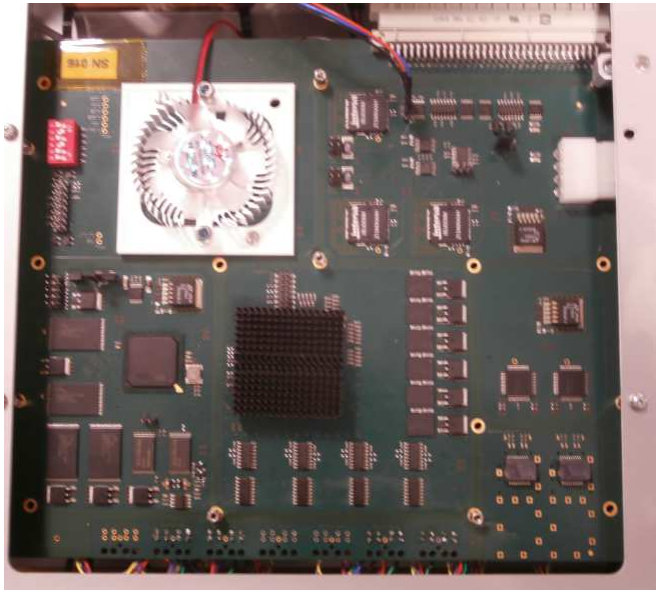
# VISNAV





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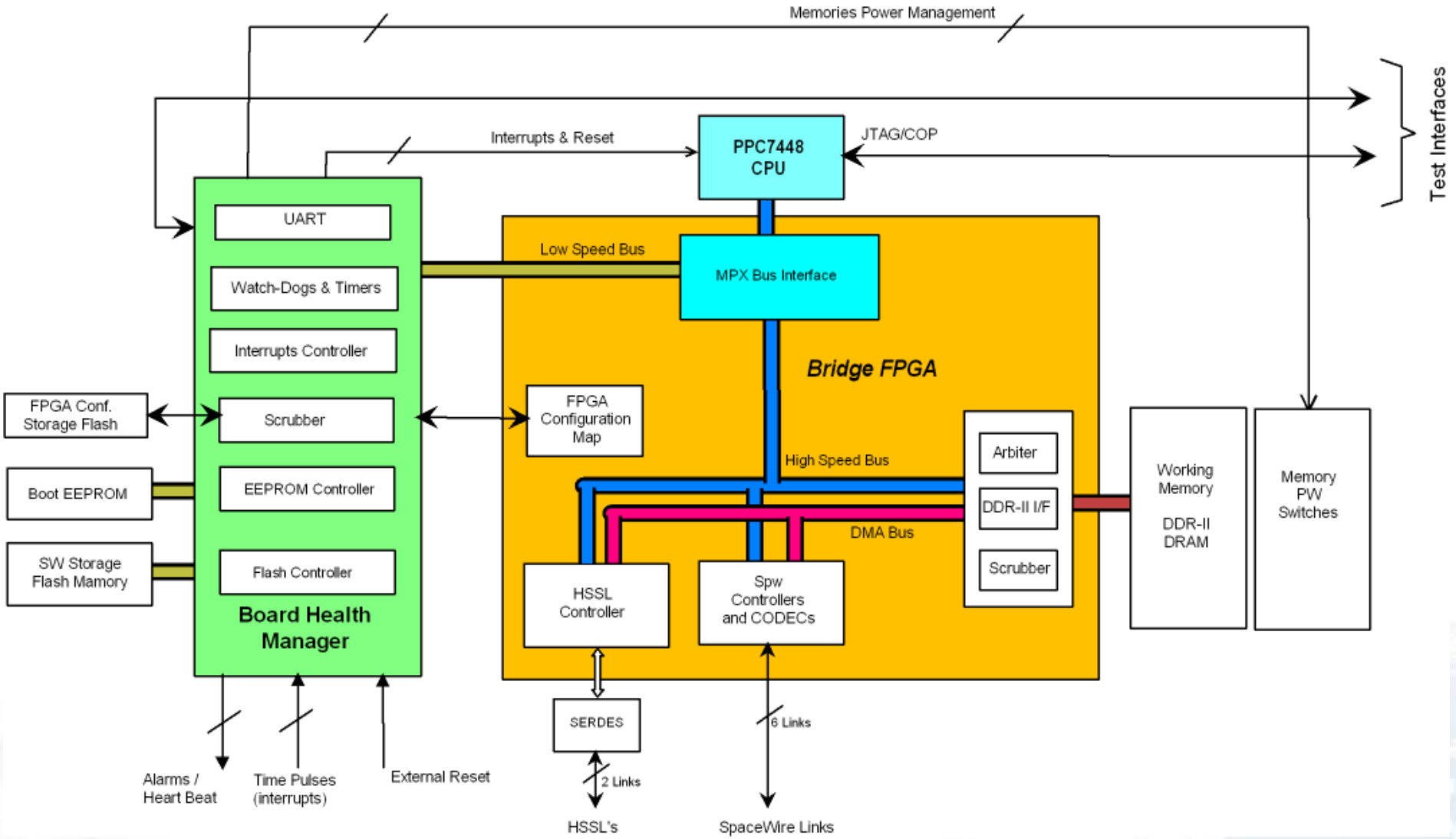
# 2- Hi-Rel cots Board overview

# PM Block Diagram





# Hi-Rel Cots  board Main Characteristics



- **CPU:**
  - Freescale PowerPC PC7448 on Silicon-on-Insulator 90 nm process
  - Performance 2.3 MIPS / MHz (Drystone 2.1 method) (*)
  - 2300 MIPS @ 1 GHz (*)
  - 32 KB L1 cache for Instructions, with Parity
  - 32 KB L1 cache for Data, with Parity
  - 1 MB L2 cache ECC protected
  - Four Integer Units (IUs)
  - A five stages Fully IEEE Compliant FPU for single and double precision operations
  - Four Vector units (SIMD machine, typical task for DSP application) Altivec™

- **MEMORIES:**
  - Up to 256 kBytes EEPROM Boot Memory (or 64 kBytes PROM)
  - Up to 32 Mbytes Flash for Software Storage
  - 512 Mbytes DDR-II DRAM as Working Memory, RS protected,
  - High Memory access throughput for CPU and peripherals (> 500 Mbytes/sec)
  - DMA Accesses to/from peripherals

(*) Data from Freescale manufacturer

# Hi- rel cots board Interfaces



**High Speed Interfaces**

- 6 x Spacewire Links (up to 200 Mbps)
- 2 x HSSL:
  - 1Gbit Ethernet
  - UDP Layer
  - standard Message frames (about 1500 bytes data max size)
- Communications through:
  - DMA to/from Memory
  - Mail-boxes (small data sets, typically 1/2 kBytes)

**Discrete Interfaces**:

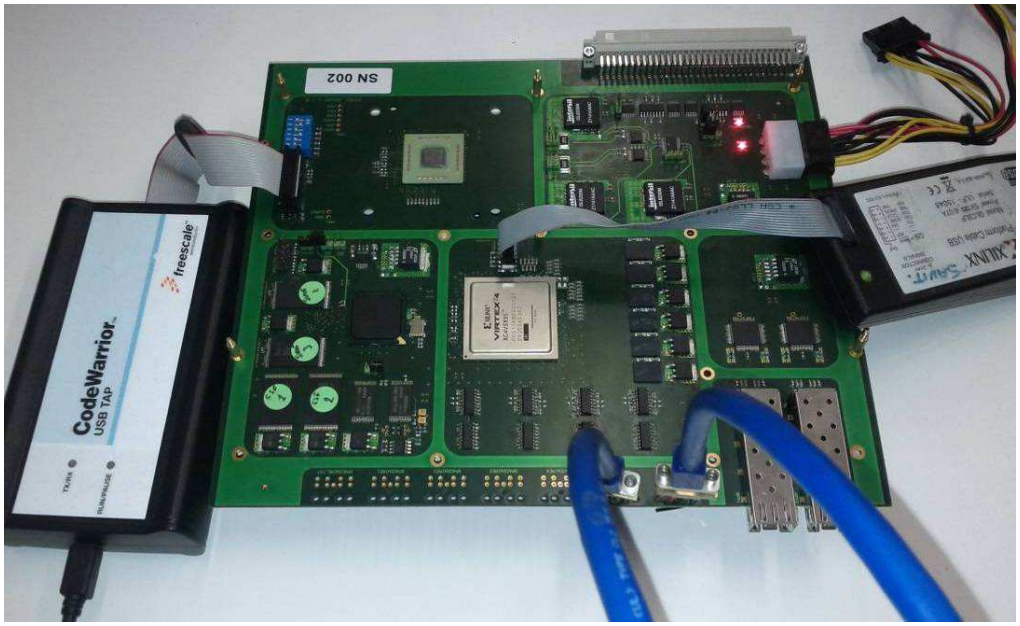
- 4x External Interrupts (I)
- 4x Pulse Outputs (O)
- External Reset (I)
- Alarms (O)
- Heart-Beat (O)

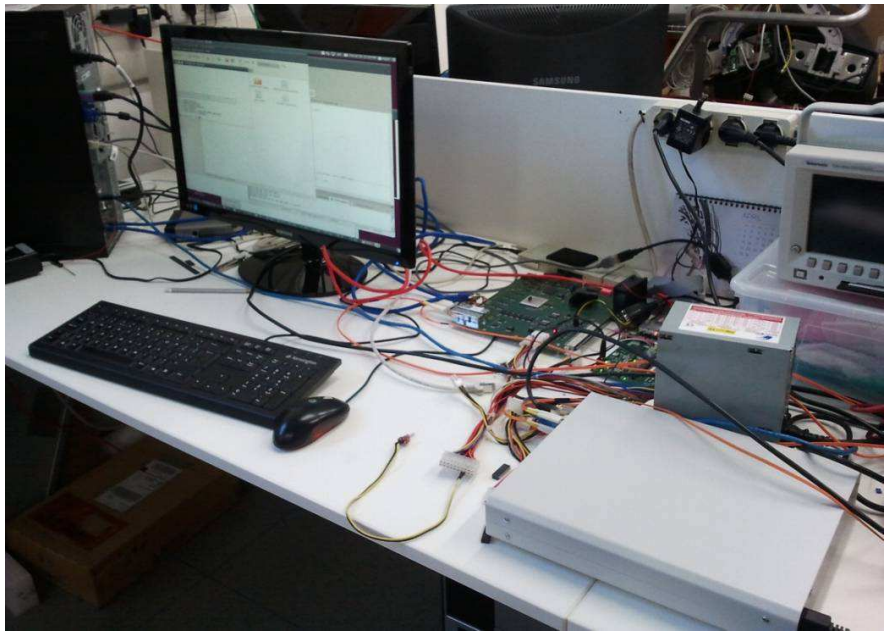
**Test Interfaces:**

- CPU JTAG/COP Interface
- RS232 UART:
  - Loading of SW in NVM
  - Communication with CPU
  - Access to FPGA registers

# Hi-rel cots PM Board view





- Extended Double Eurocard Form factor: 233 x 200 $mm^2$
- Mass: < 850 gr (including stiffening frame)
- Power Consumption: ~ 17 W @ 1 GHz Core Clock (measured)



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# Basic Software



- Development Tools
  - Boot software and drivers developed in C and assembler
  - Boot software and drivers developed and compiled using CodeWarrior 8.8 Development Tool by Freescale
- Boot software developed on the basis of the initialization functions provided by Freescale for the PCC74xx processors
  - Boot operations organized in: initialization, self-check, and start of the User SW application
- Simple SW drivers developed to access and manage the PM basic functions
  - SW driver have been grouped by PM architectural resource (e.g. I/O interfaces, timers, memories, etc.)

# 3- Hi-Rel cots EGSE

# Hi-rel cots board EGSE




- Powerful workstation PC, including
  - 6 SpaceWire ports
  - 1 Lauterbach Debugger tool
  - XILINX JTAG probe
  - ACTEL JTAG probe
  - 1 pci Digital I/O board
  - 1 Ethernet board with two Gigabit ports
- Microsoft Windows 7, 32 bit
- Microsoft Visual C++ 2010 Express Development Environment



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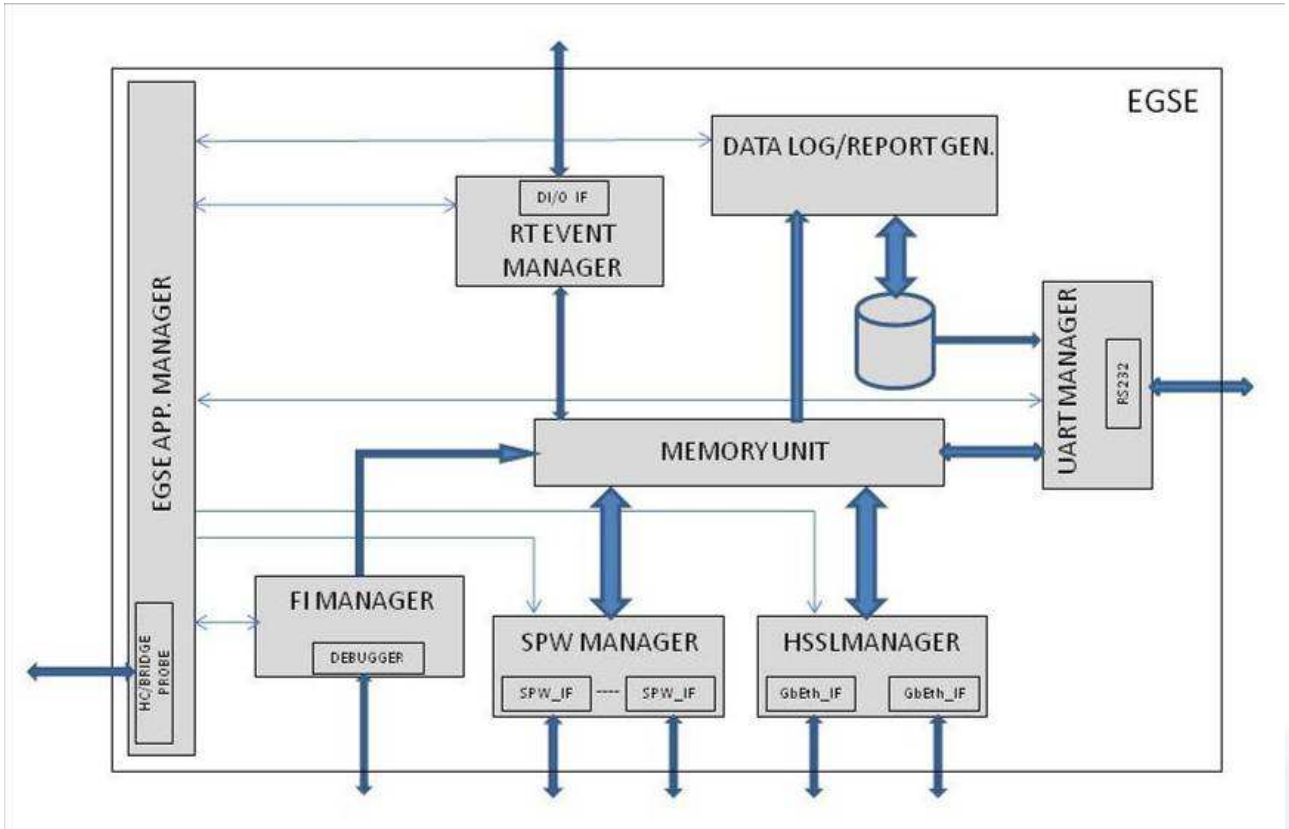
# What's EGSE for



- PM Board testing/verification
  - To test specific resources of the PM board, such as memory, communications links, and data interfaces
- Benchmarking
  - To test PM board performances when selected benchmarks are applied
- Fault injection
  - To test the response of the PM board in presence of SEU like faults

# EGSE Block Diagram

- Modular approach
- Functional blocks that can be used in any applications, for instance PM Board testing, as basic atomic ingredients
  - uart_manager
  - spacewire_manager
  - hssl_manager
  - rt_event_manger
- Avoid rewriting the same code multiple times, code can be reused



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# Verification Tests



- The objective is to show that implemented functions comply with all high level requirements.
- Implemented functions are verified by a set of procedures mainly running on the board processor and ruled by the EGSE
- Tests have been grouped in the following categories reflecting PM board and FPGAs specification:
  - Memories resources (including registers)
  - Communication buses
  - Data exchange interface functions
  - Board control, time and fault management
  - Test interfaces
  - Debug and fault injection specific function



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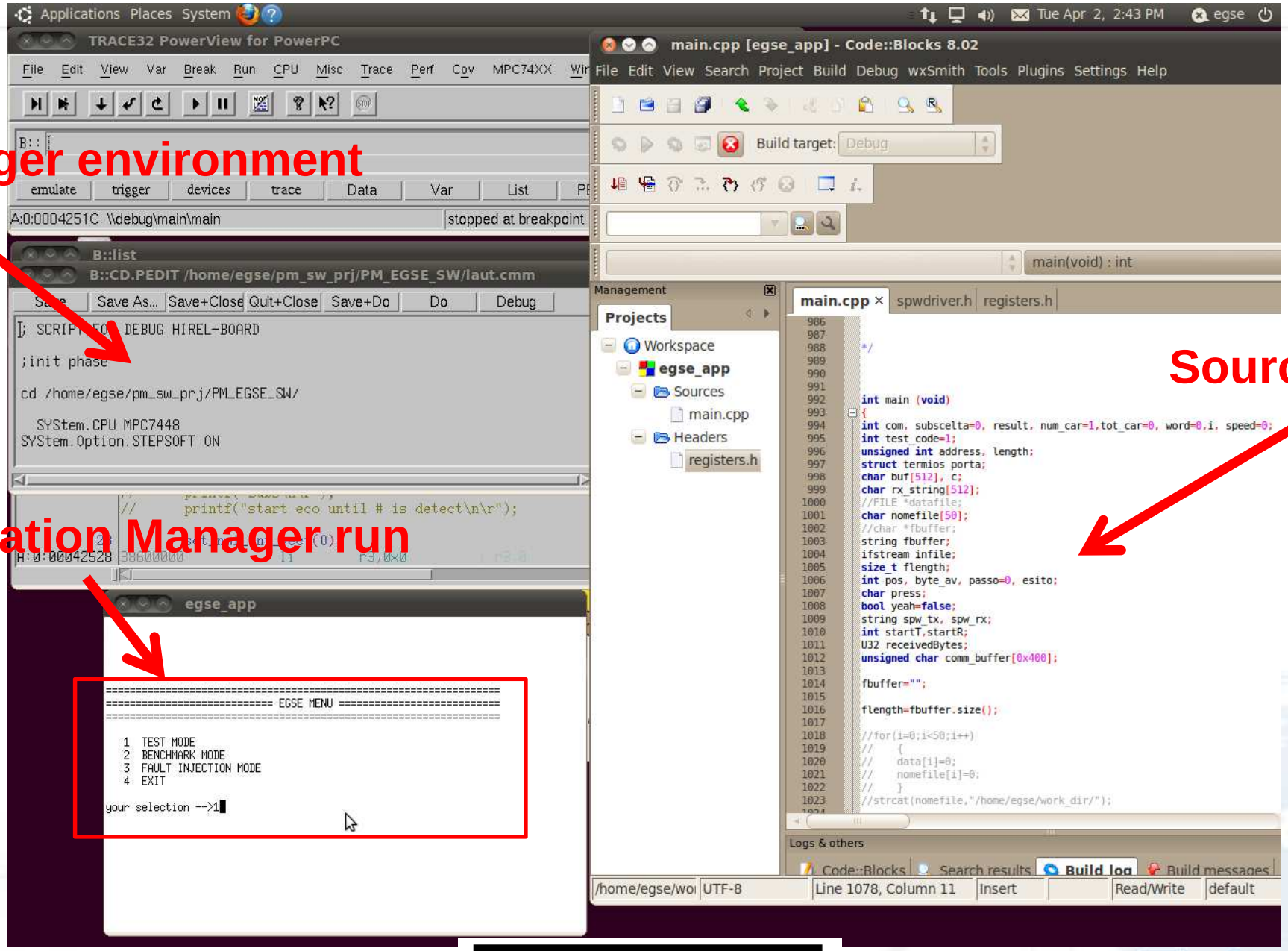
# EGSE Operation





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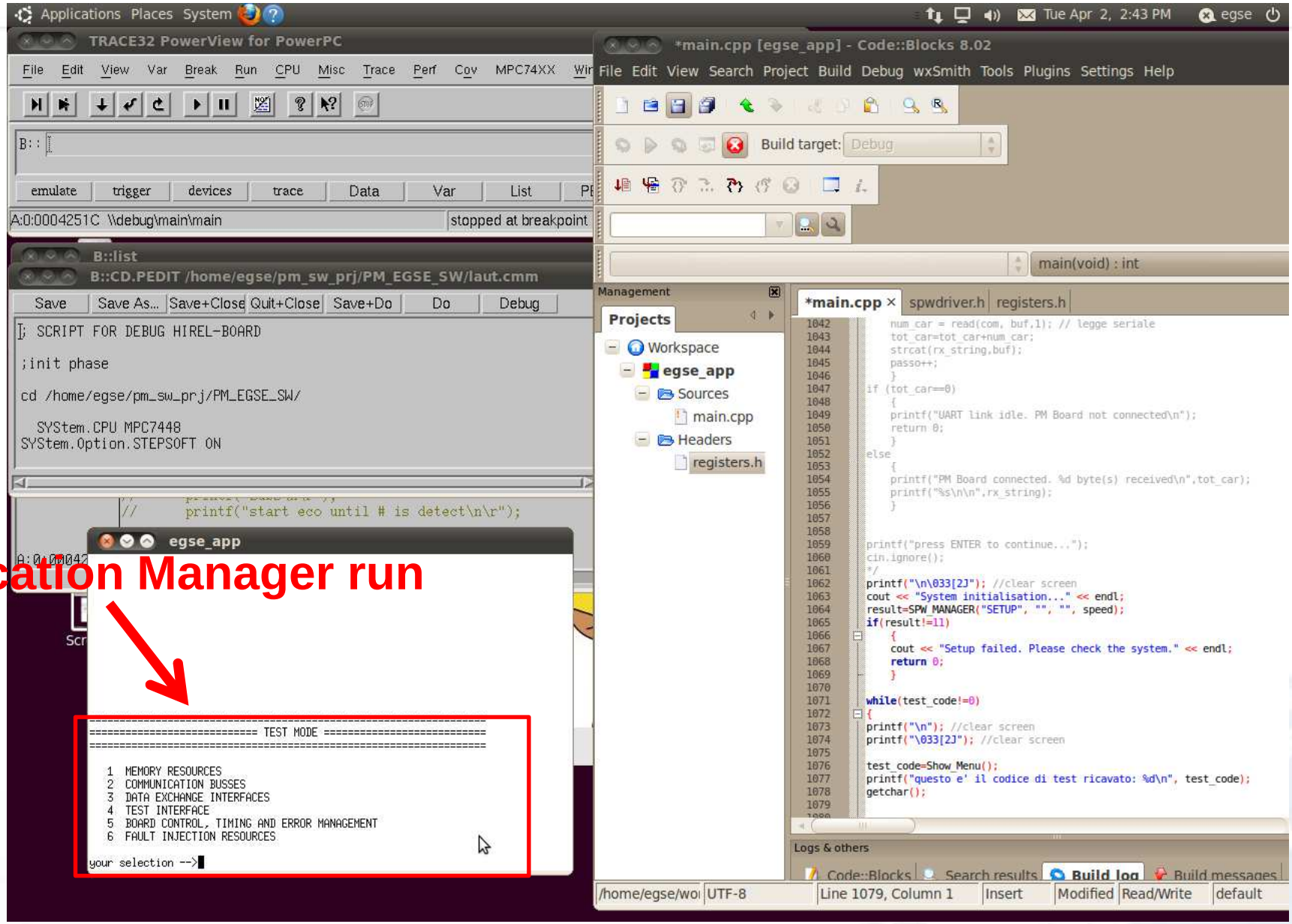
# EGSE Operation (cont'd)





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# 4- Hi-Rel cots SIHFT test

# Polito's involvment in the Hi-Rel CoCS programme

- Develop a Software implemented hardware fault-tolerance technique
- Develop a fault injection strategy
- Evaluate system reliability through fault injection



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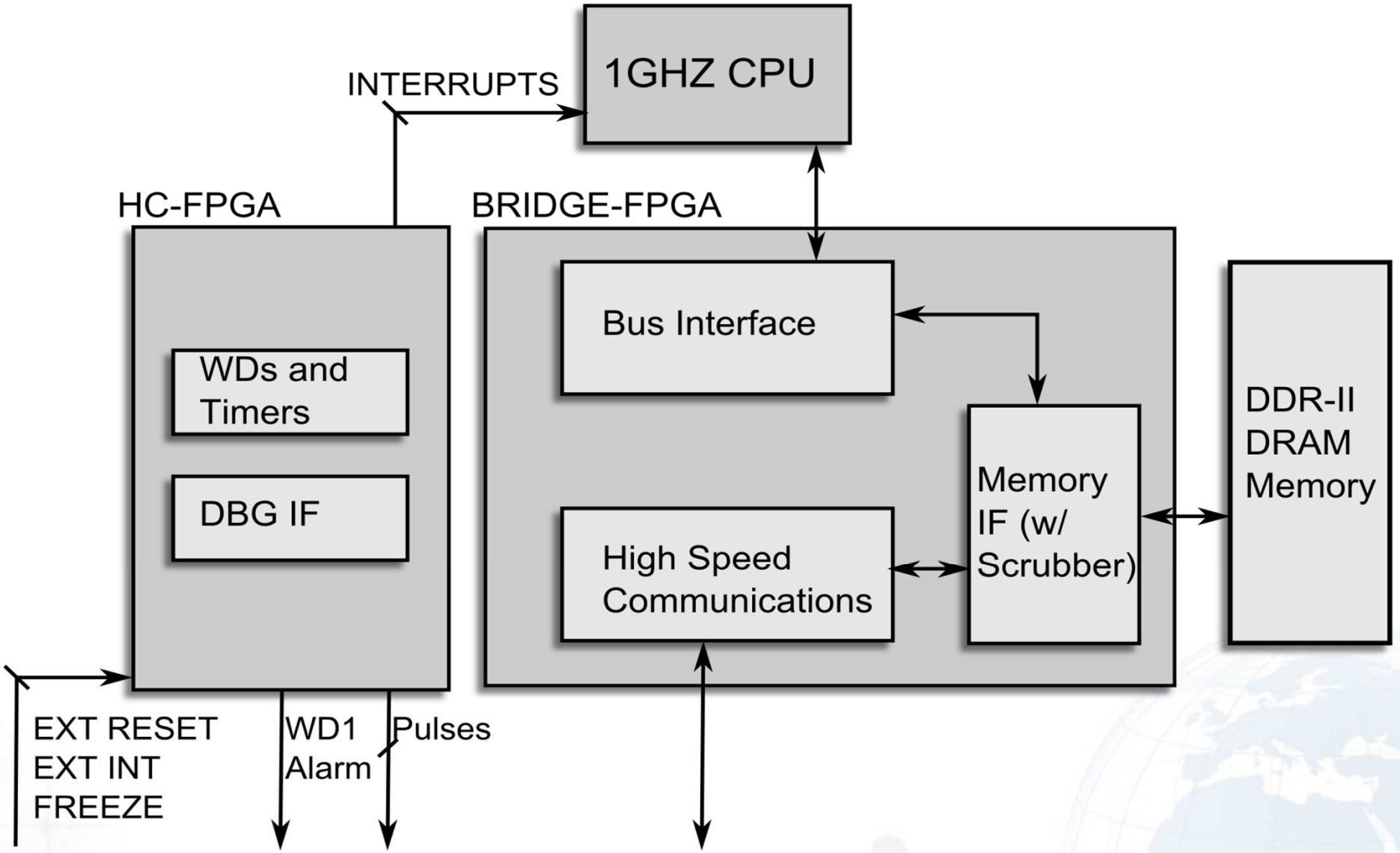
# The target system (simplified diagram)

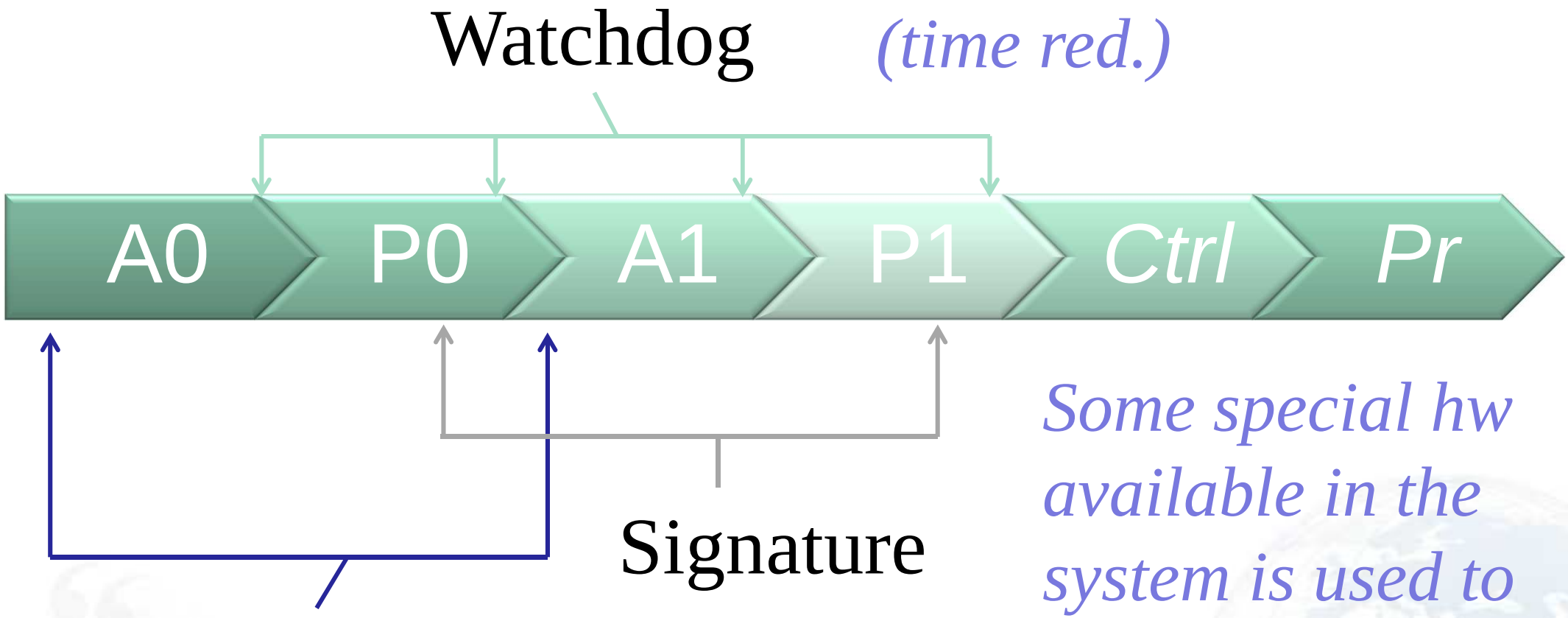


# The benchmark

- Composed of RICE, FFT, Dhrystone
- An SIHFT strategy was implemented on this benchmark

# SHIFT

*Acquisition and processing are repeated (time red.)*




*Some special hw available in the system is used to detect CFEs*



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# Recovery Mechanisms

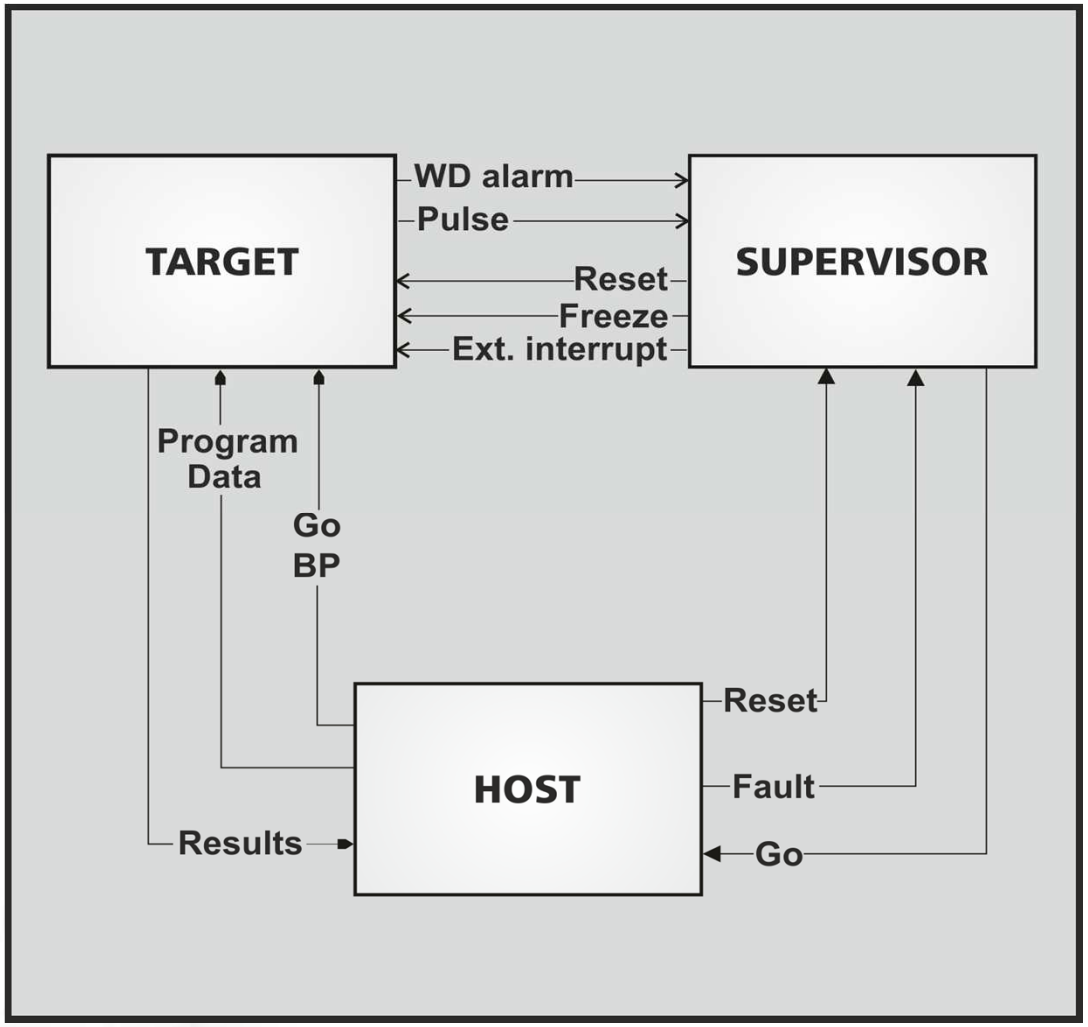
- Backward Recovery:
  - If a fault is detected at checkpoint, repeat both executions

- Forward Recovery:
  - If a fault is detected at checkpoint, execute a third time and select output through a majority vote

# Performance Evaluation

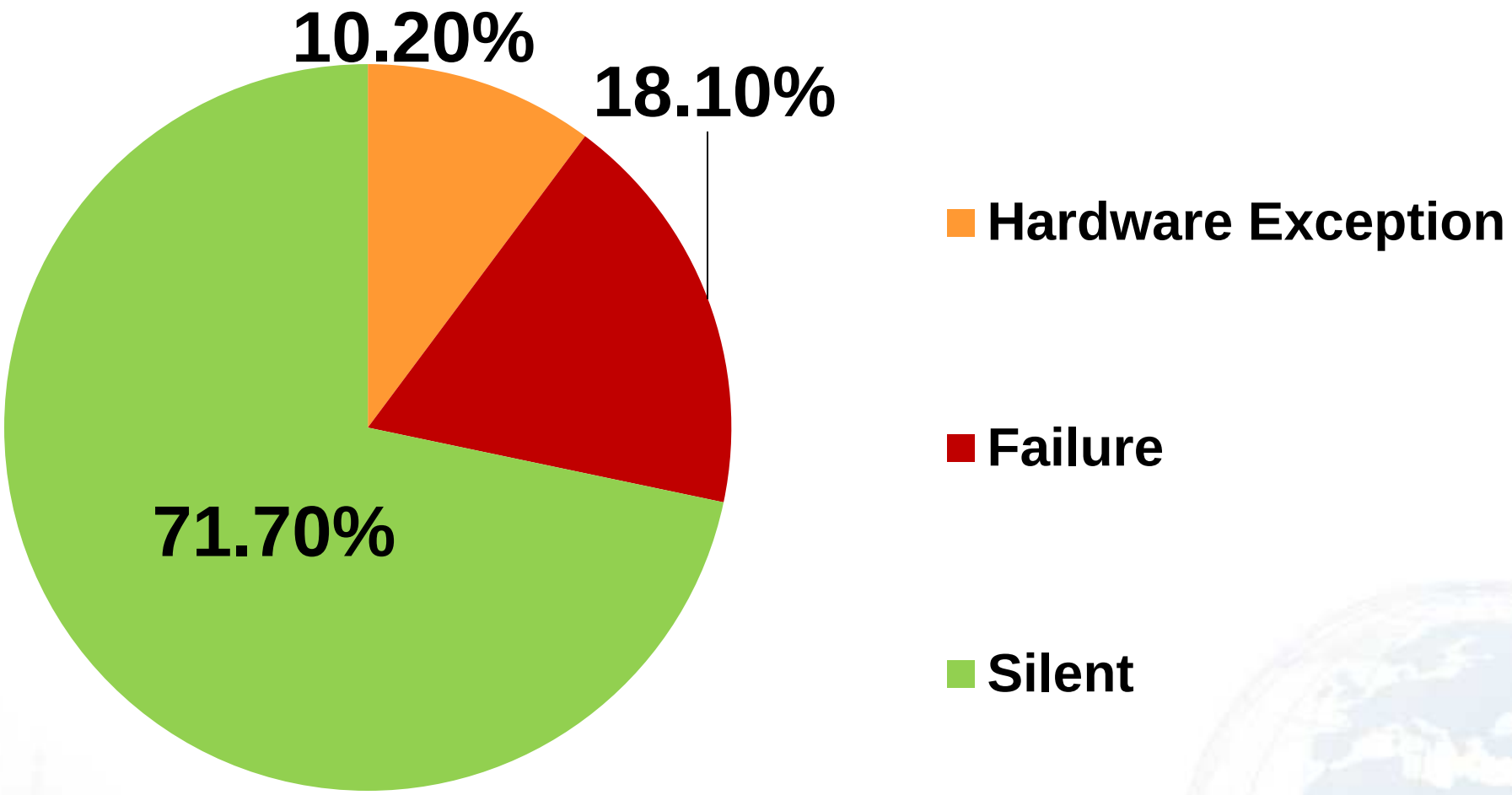
| | Exe. Time (us) | .text+ .init | .data | .sbss | .bss | Total |
|---|---|---|---|---|---|---|
| **w/o SIHFT** | 9,670 | 23,808 | 29,312 | 40 | 39,584 | 92,744 |
| **w/ SIHFT** | 19,833 | 25,292 | 29,440 | 20 | 68,880 | 123,632 |
| **Diff.** | **+105%** | **+6%** | **+0.4%** | **+100%** | **+74%** | **+33.3%** |

# Fault Injection Experiments

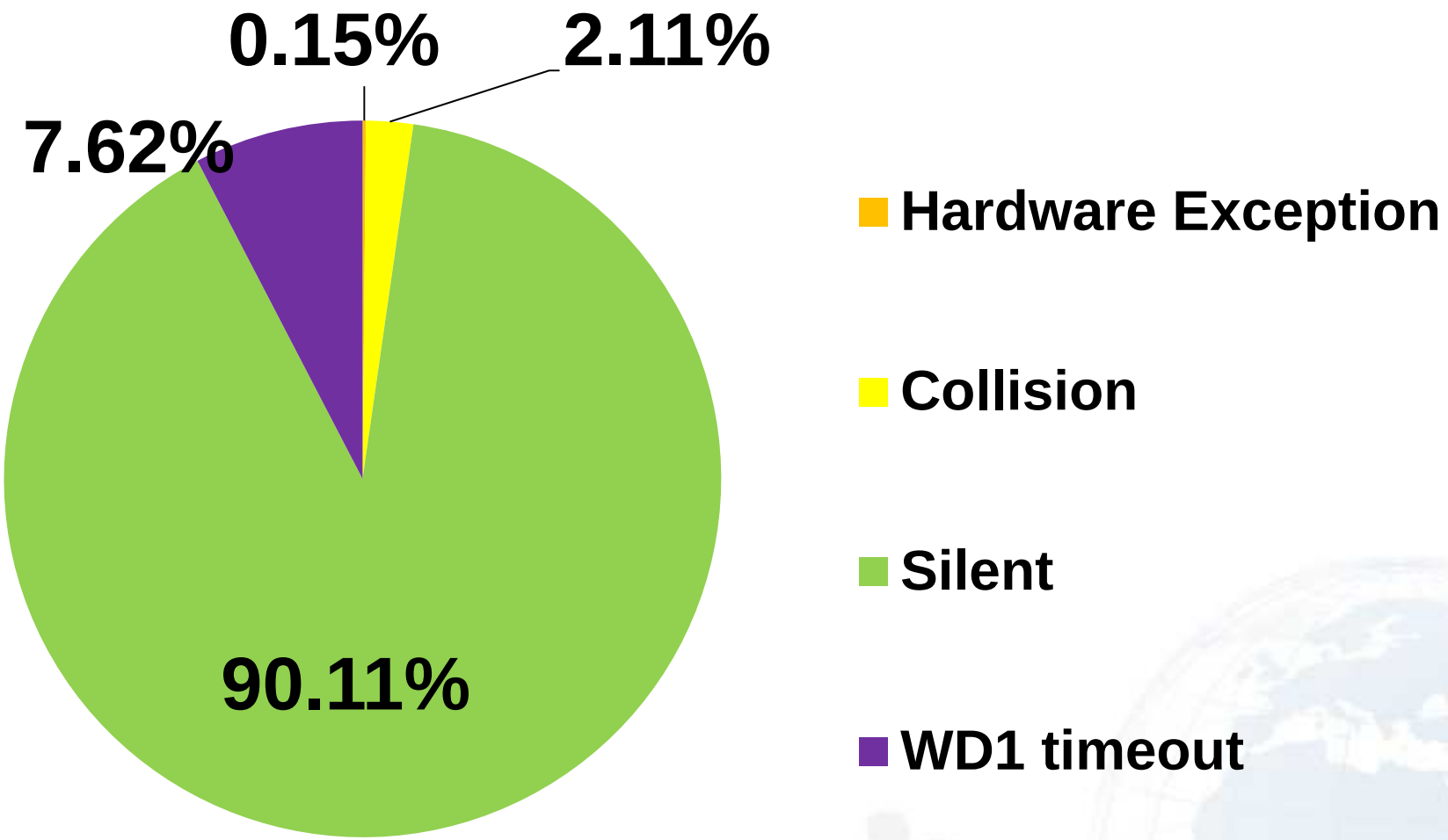



- Software (SW)
- Watchdog (TO)
- Exception (EXC)
- FAILURE
- SILENT

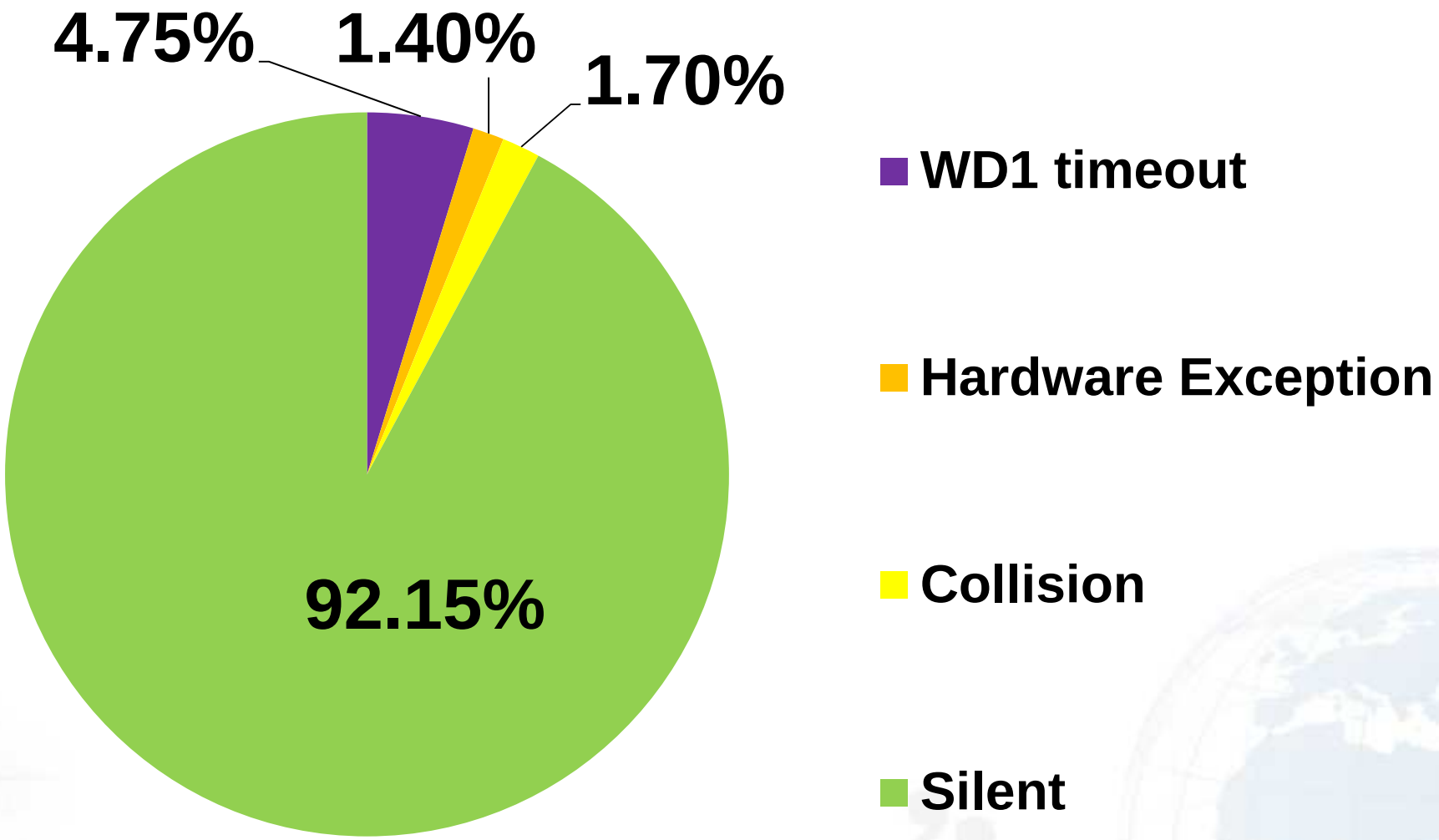
# Results: Without SIHFT



# Results: with SIHFT and Backward Recovery



# Results: with SIHFT and Forward Recovery



# Results: dissemination

- Results from this work were presented at the NSREC'15 conference held in Boston in July 2015.

- A paper describing the approach, the experimental methodology and the results was published on the December 2016 issue of IEEE Transactions on Nuclear Science.
  - S. Esposito, C. Albanese, M. Alderighi, F. Casini, L. Giganti, M. L. Esposti, C. Monteleone, and M. Violante, "COTS-Based High-Performance Computing for Space Applications," *IEEE Trans. Nucl. Sci.*, vol. 62, no. 6, 2015.

# SW test: conclusions and future *developments*

- The implemented SIHFT solution is a viable way to implement space applications using COTS, meeting the dependability requirements of the domain.

- Future solutions will leverage multicore architectures for fault tolerance implementation.

# 5- Hi-Rel cots project conclusion and possible developments

Main lesson learned for future developments:

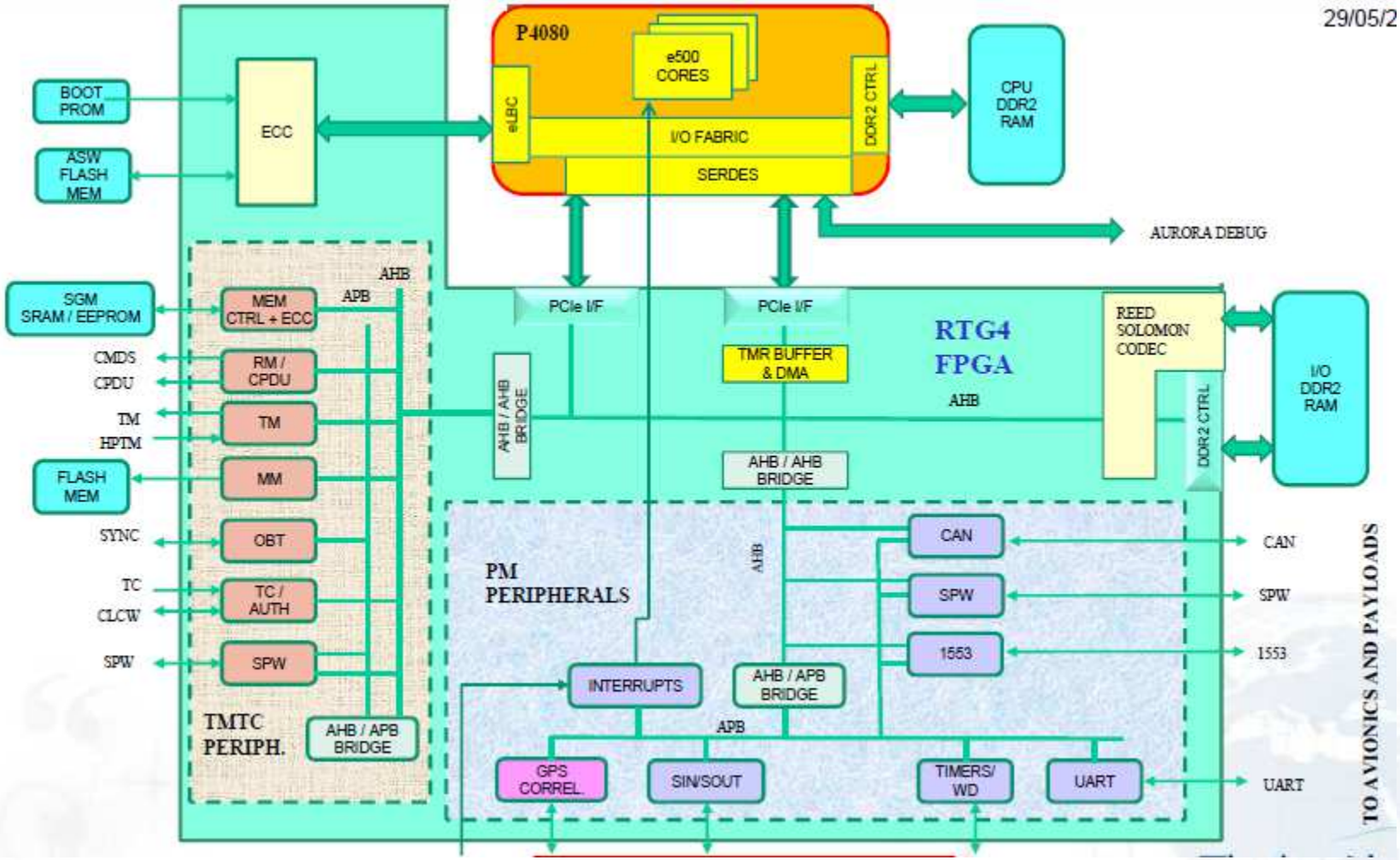
1. Resources (memories) shall be interfaced directly with the CPU to use the full potentiality of power PC processing

2. I/O shall be managed by Hi rel FPGA and not by CPU

3. Future solutions will leverage multicore power PC architectures for fault tolerance implementation (i.e. majority voting) with Hypervisor in order to mitigate SW errors

# Platform Computer based on Fault Tolerant Hypervisor






# High performance platform computer architecture