Emulator of Future NGMP Multicore

HAIR

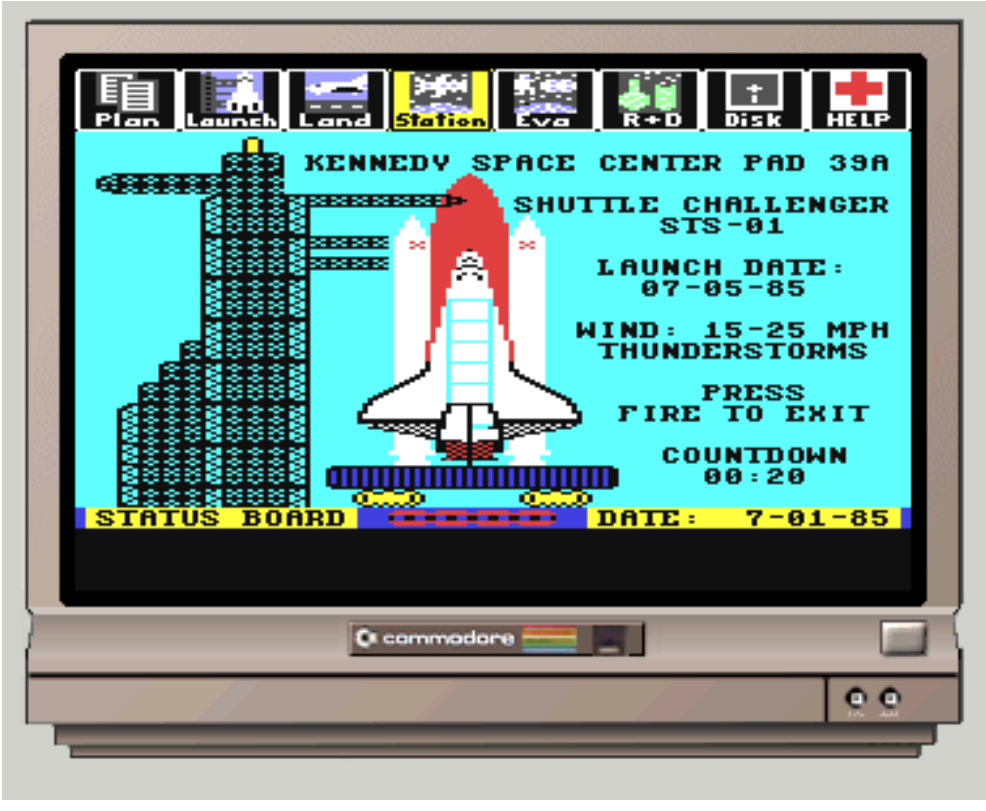
RAPITA SYSTEMS LTD

BSC Barcelona Supercomputing Center Centro Nacional de Supercomputación

gmv INNOVATING SOLUTIONS

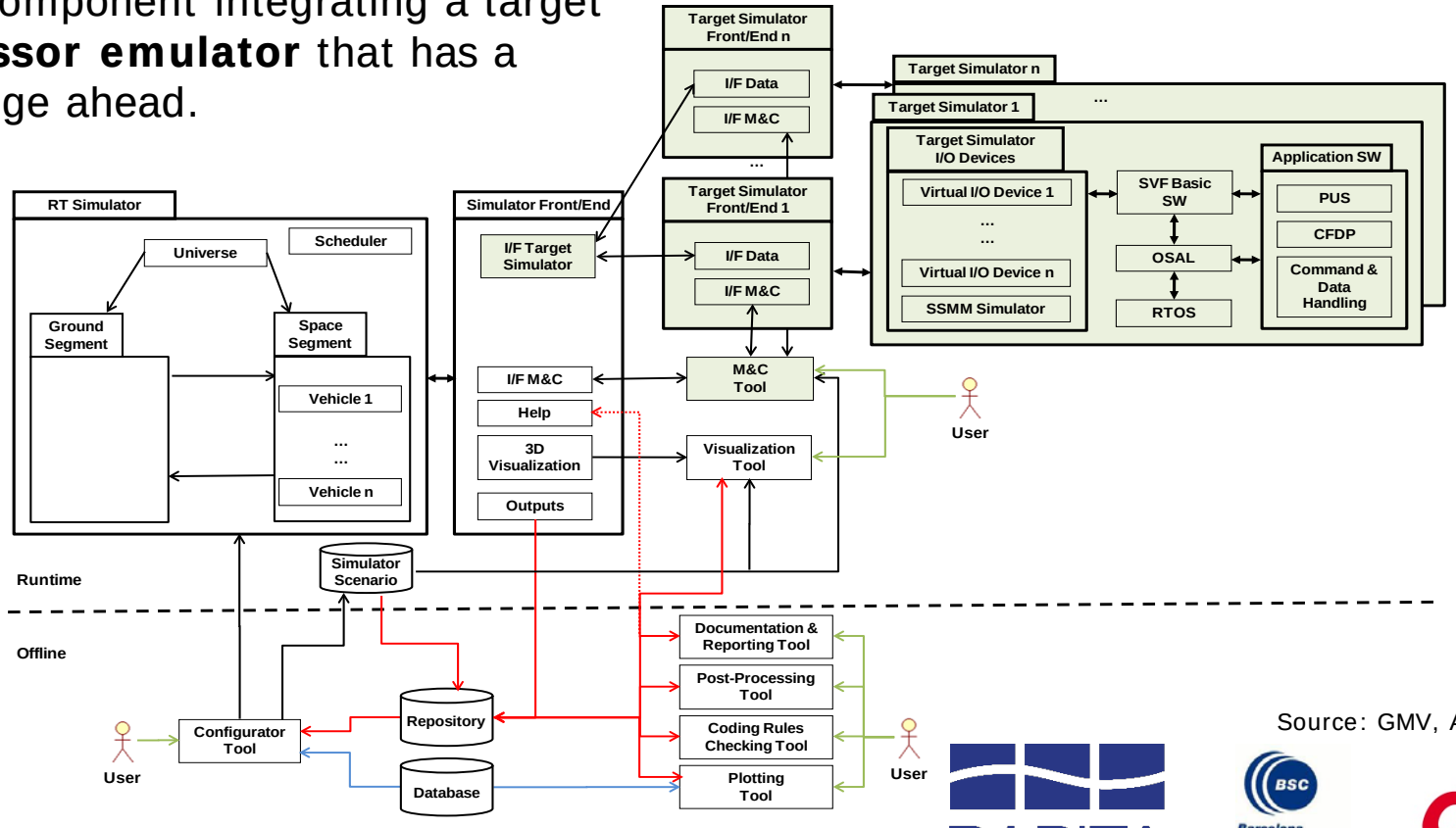
SOFTWARE VALIDATION FACILITY

SVF provides a fully functional and performance representative simulation model of the S/C HW and its dynamic behaviour in space.



PROCESSOR EMULATOR

The Target Simulator is the SVF main component integrating a target **processor emulator** that has a challenge ahead.



Source: GMV, ATB-RAC, D8,

NGMP Multicore Processor

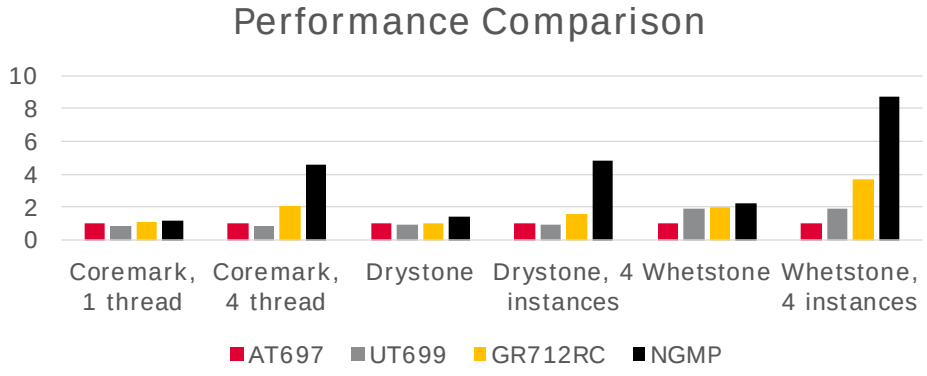
Prototype

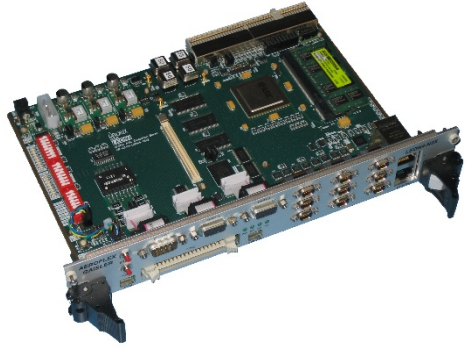
(LEON4-N2X)

- 4 x LEON4
- 2 x GRFPU
- 150 Mhz Clock

NGMP:

- 4 x LEON4
- 4 x GRFPU
- Up to 400 Mhz Clock



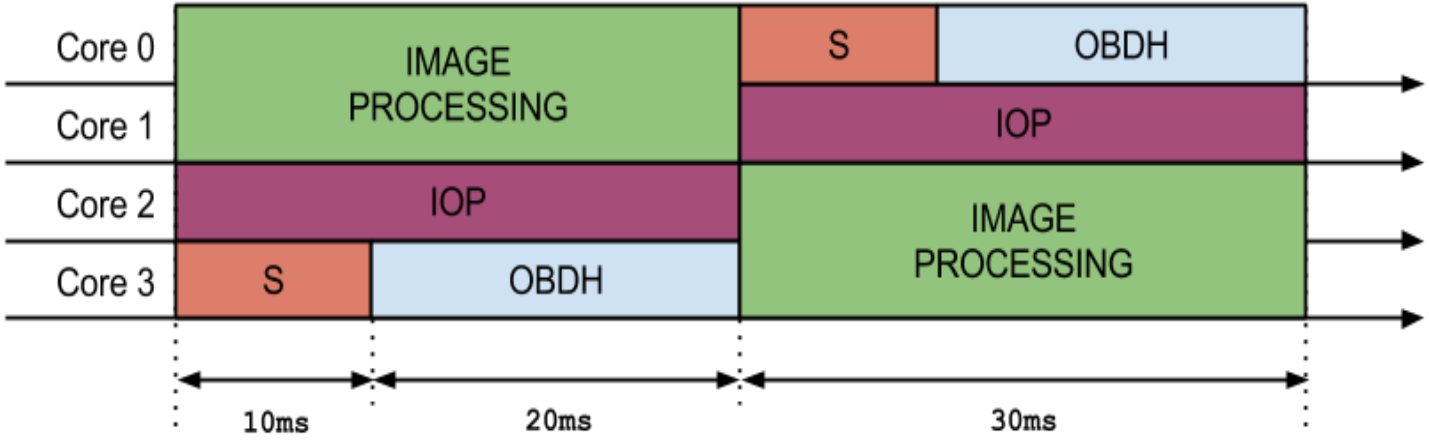


Source: Aeroflex Gaisler AB, TN on NGMP Verification

IMA & TIME AND SPACE-PARTITIONING

The NGMP will be able to host on a single computer, functions traditionally allocated on separate computers.

IMA and TSP are enablers of this use case



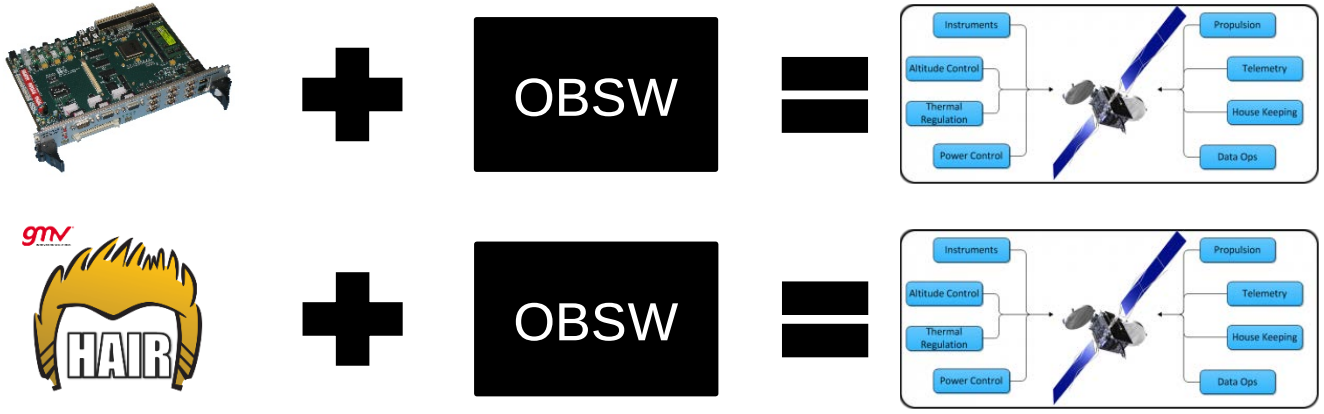
EMULATE NGMP

Same Functional behaviour of the OBSW

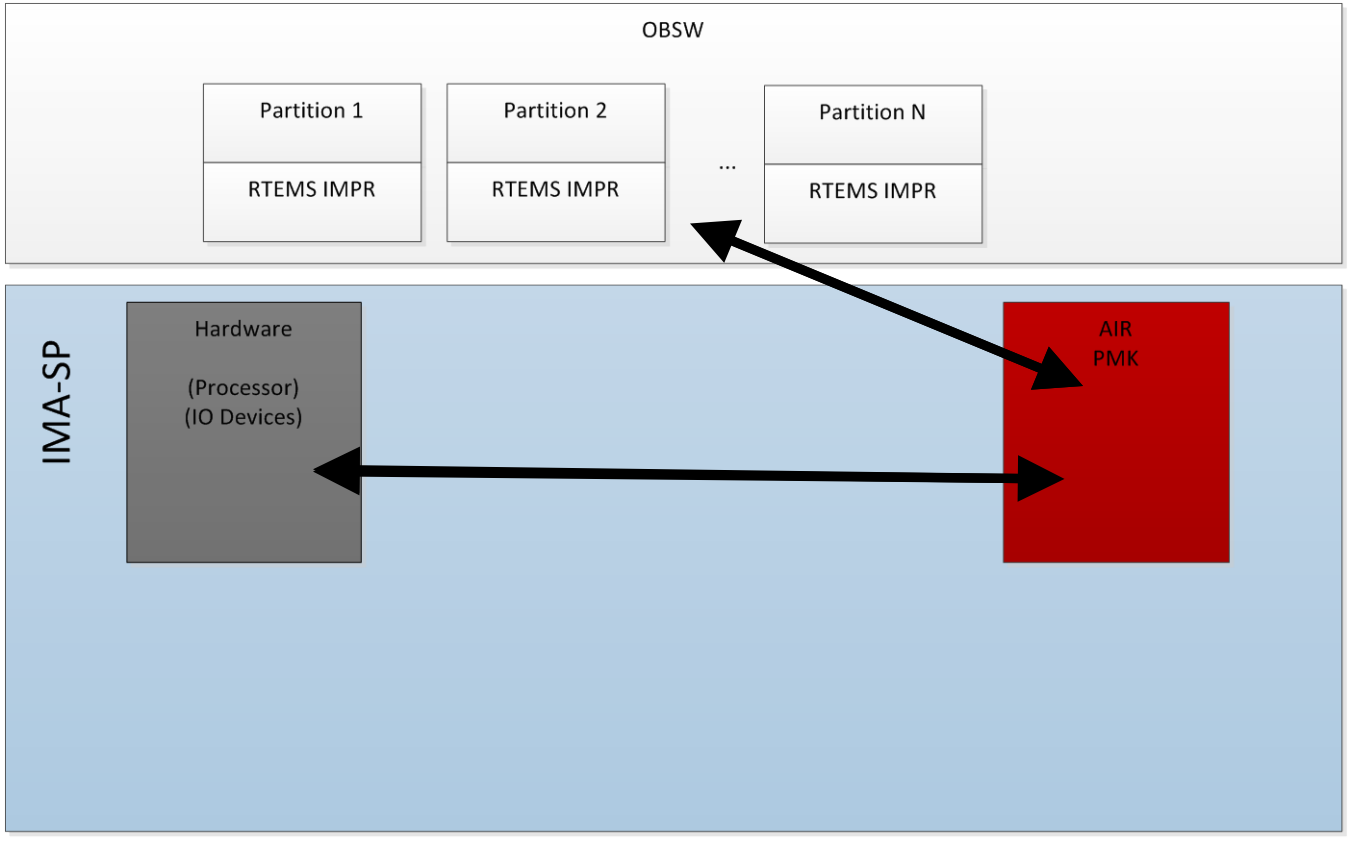
Same time profile of execution OBSW

Same SW/SW interface to the Guest OS

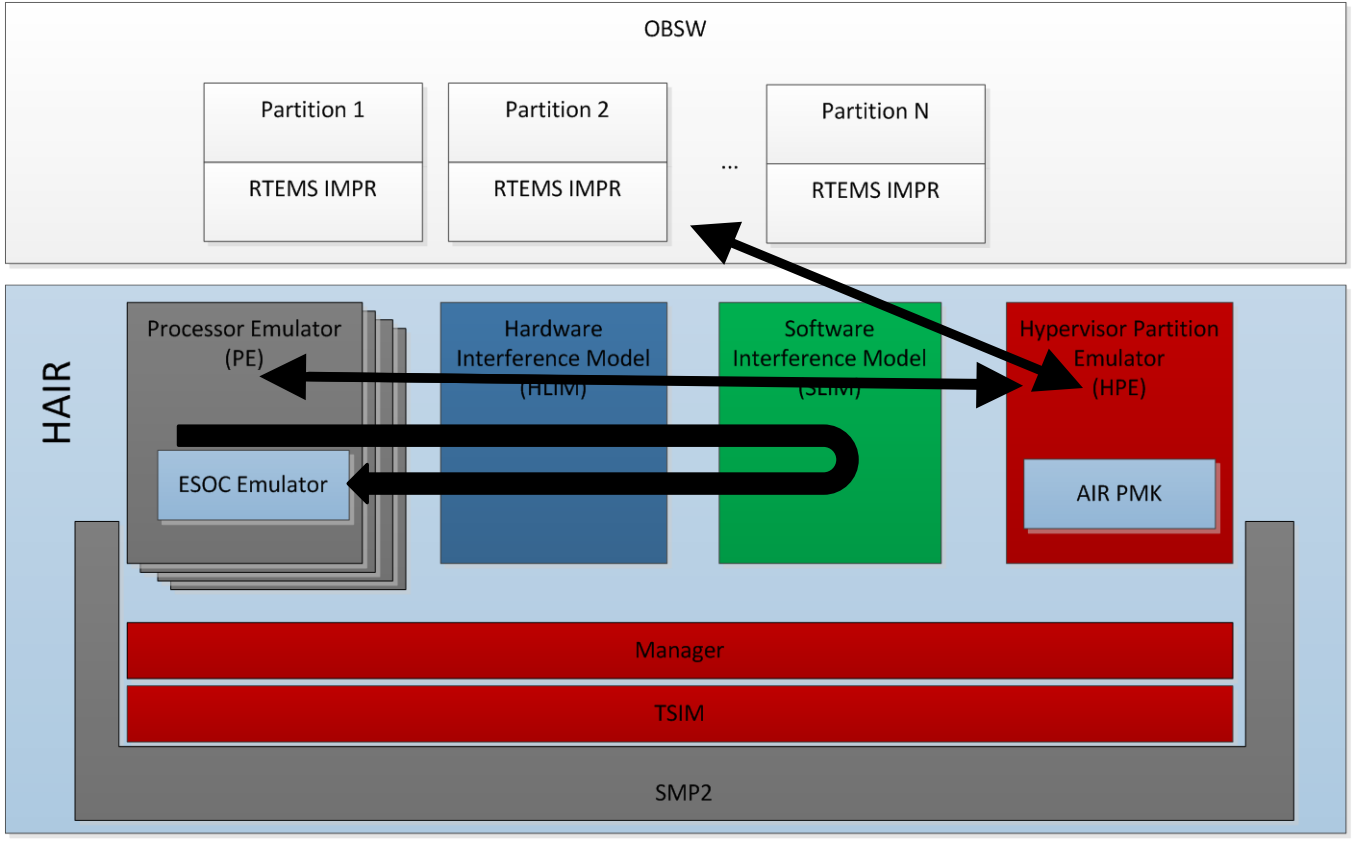
Same impact of SW running on other cores/partitions



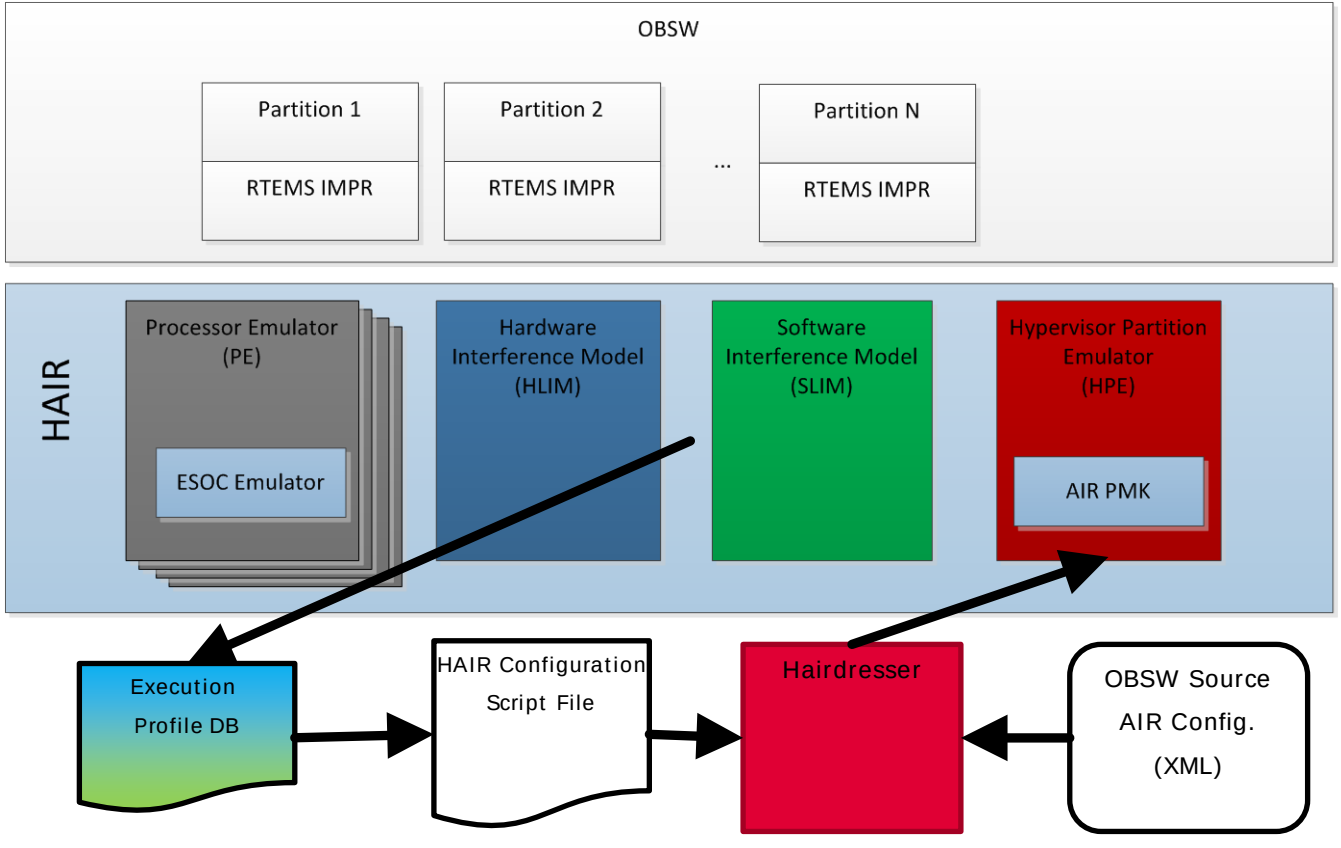
AIR on NGMP


OBSW
Partition 1
RTEMS IMPR
Partition 2
RTEMS IMPR
...
Partition N
RTEMS IMPR
IMA-SP
Hardware
(Processor)
(IO Devices)
AIR
PMK

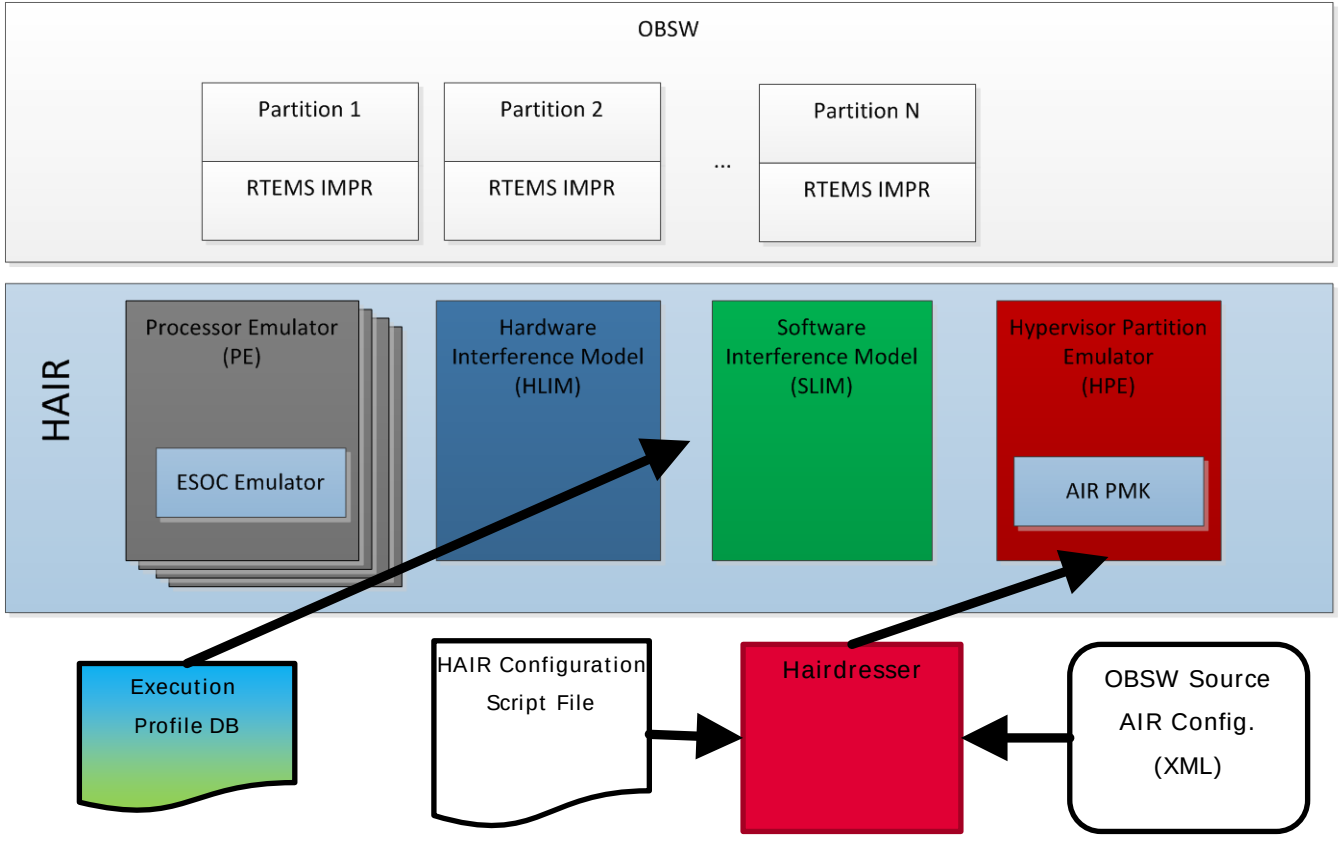
HAIR


OBSW
Partition 1
RTEMS IMPR
Partition 2
RTEMS IMPR
...
Partition N
RTEMS IMPR
HAIR
Processor Emulator (PE)
ESOC Emulator
Hardware Interference Model (HLIM)
Software Interference Model (SLIM)
Hypervisor Partition Emulator (HPE)
AIR PMK
Manager
TSIM
SMP2

HAIR Execution Profile – 1st Step

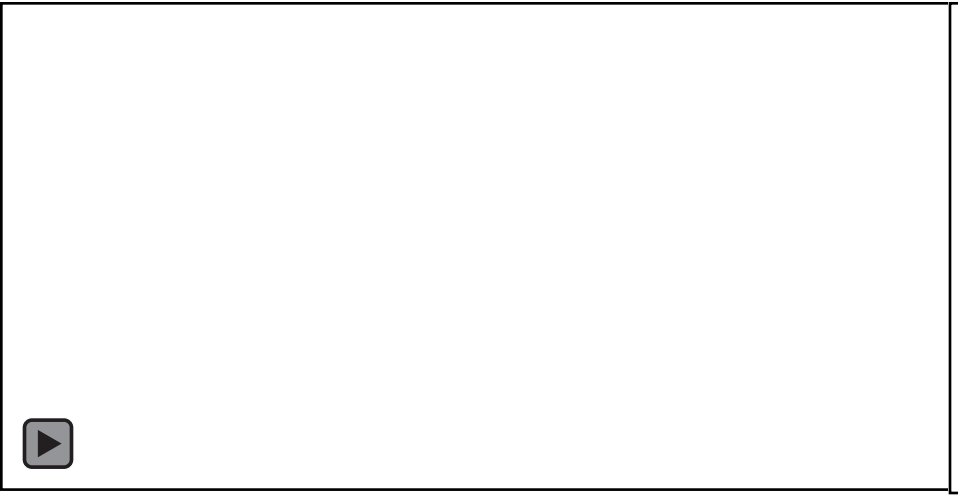


HAIR Emulation – Binary Timing Mode

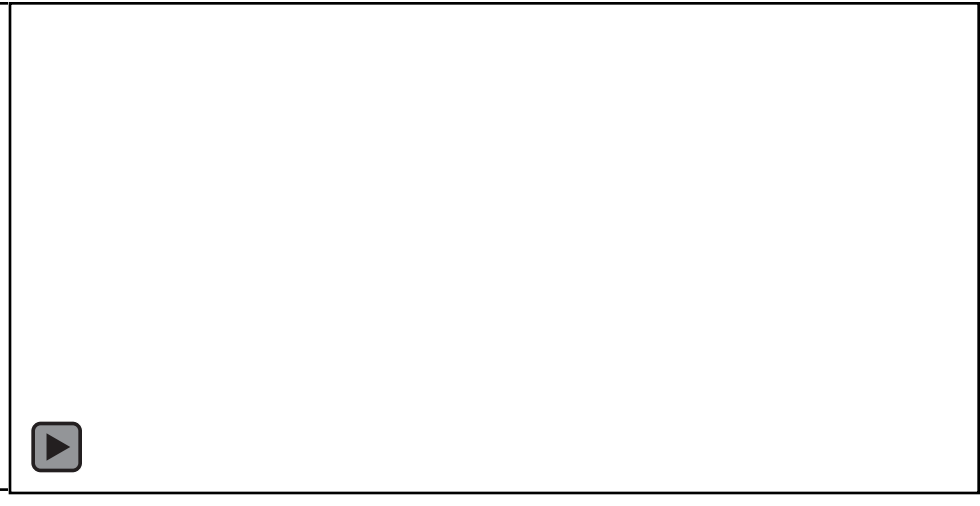


Binary Timing Demonstration

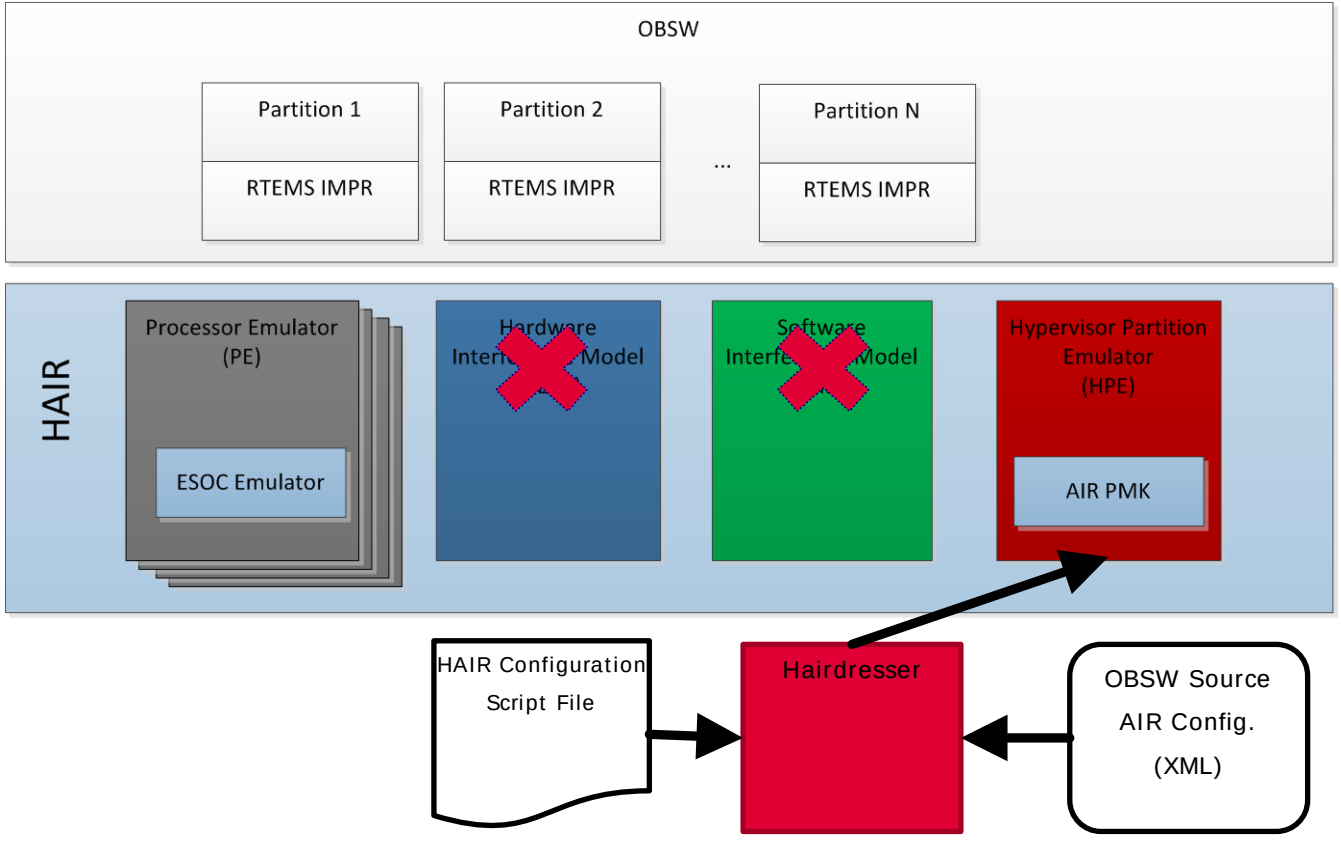
NGMP



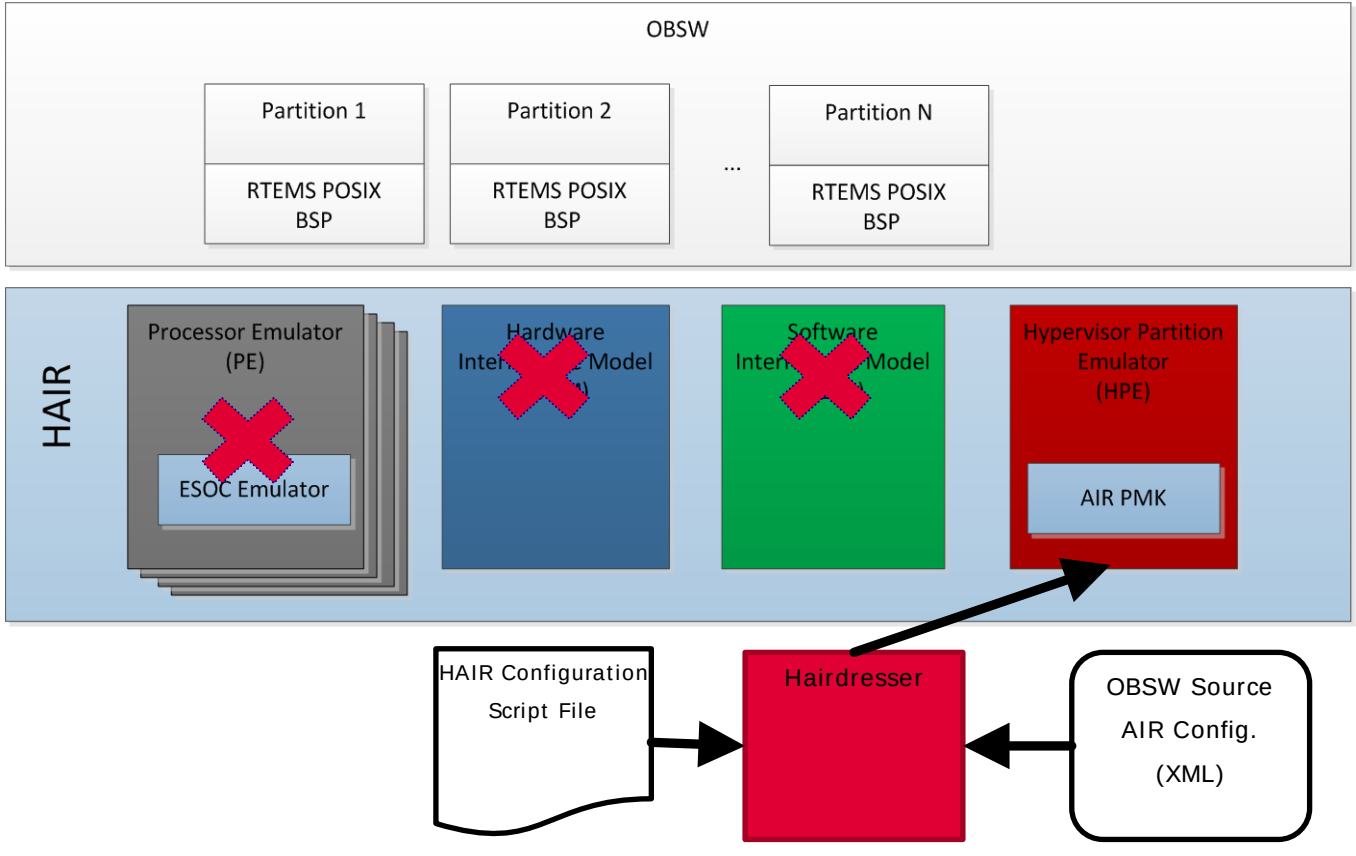
HAIR



HAIR Emulation – Binary Functional Mode



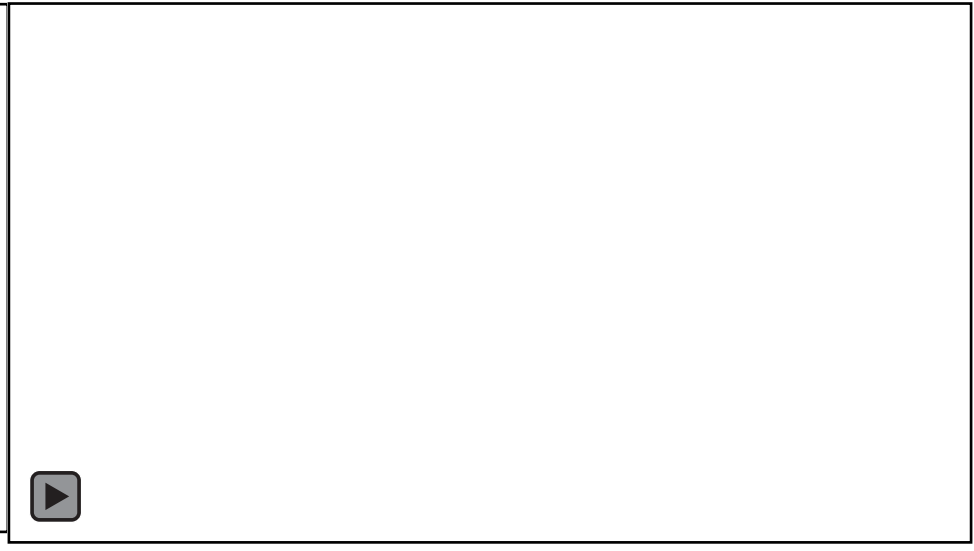
HAIR Emulation – Source Mode



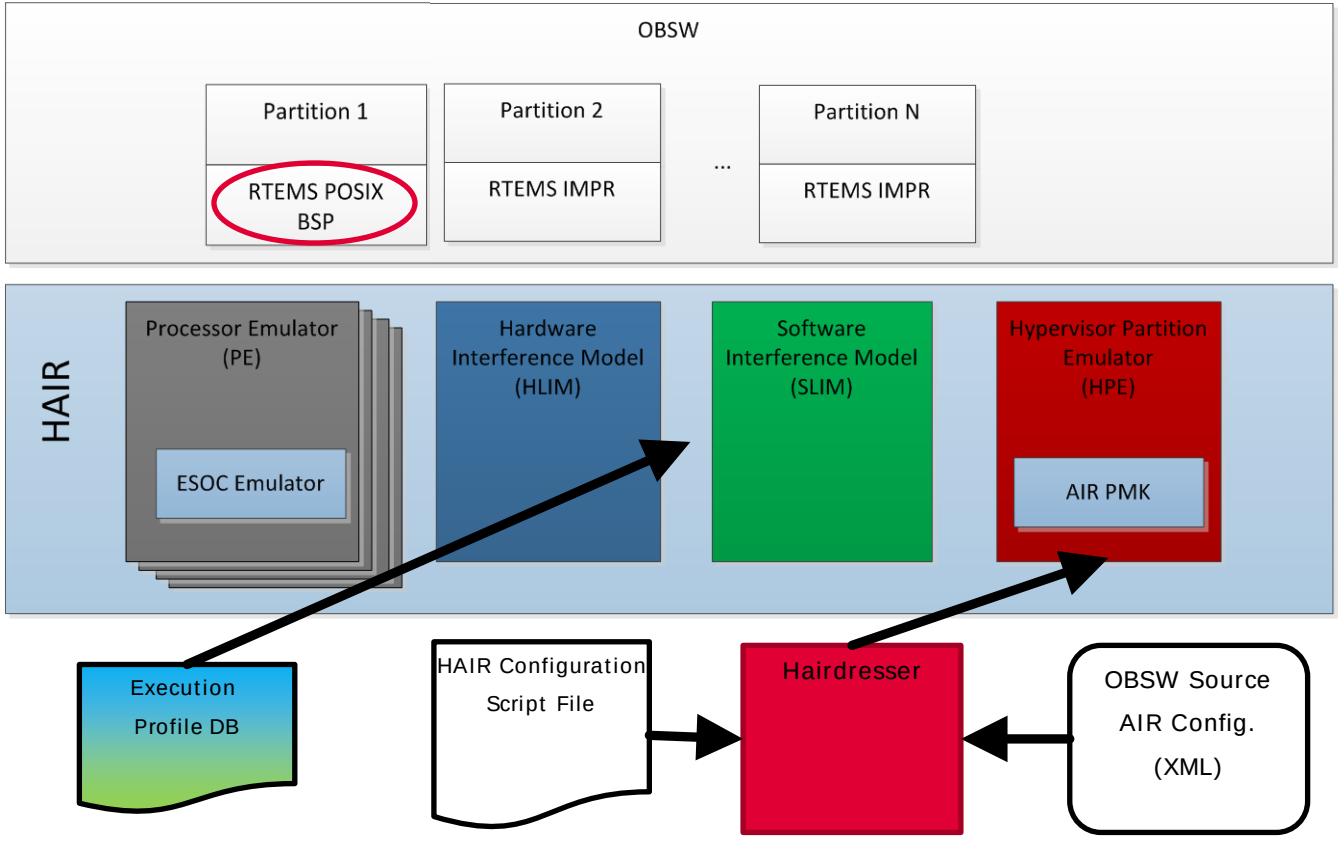
Source Mode with scheduling improved

NGMP

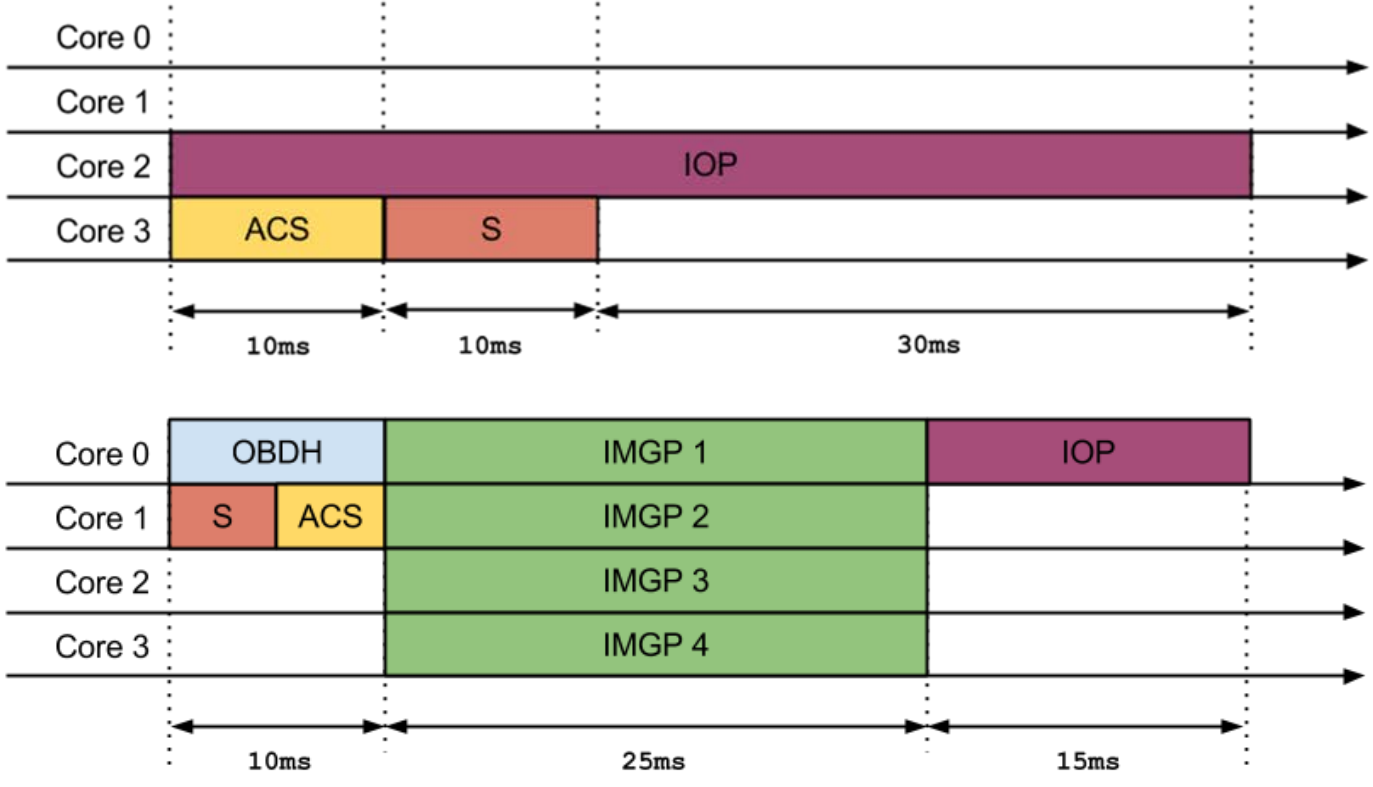
HAIR



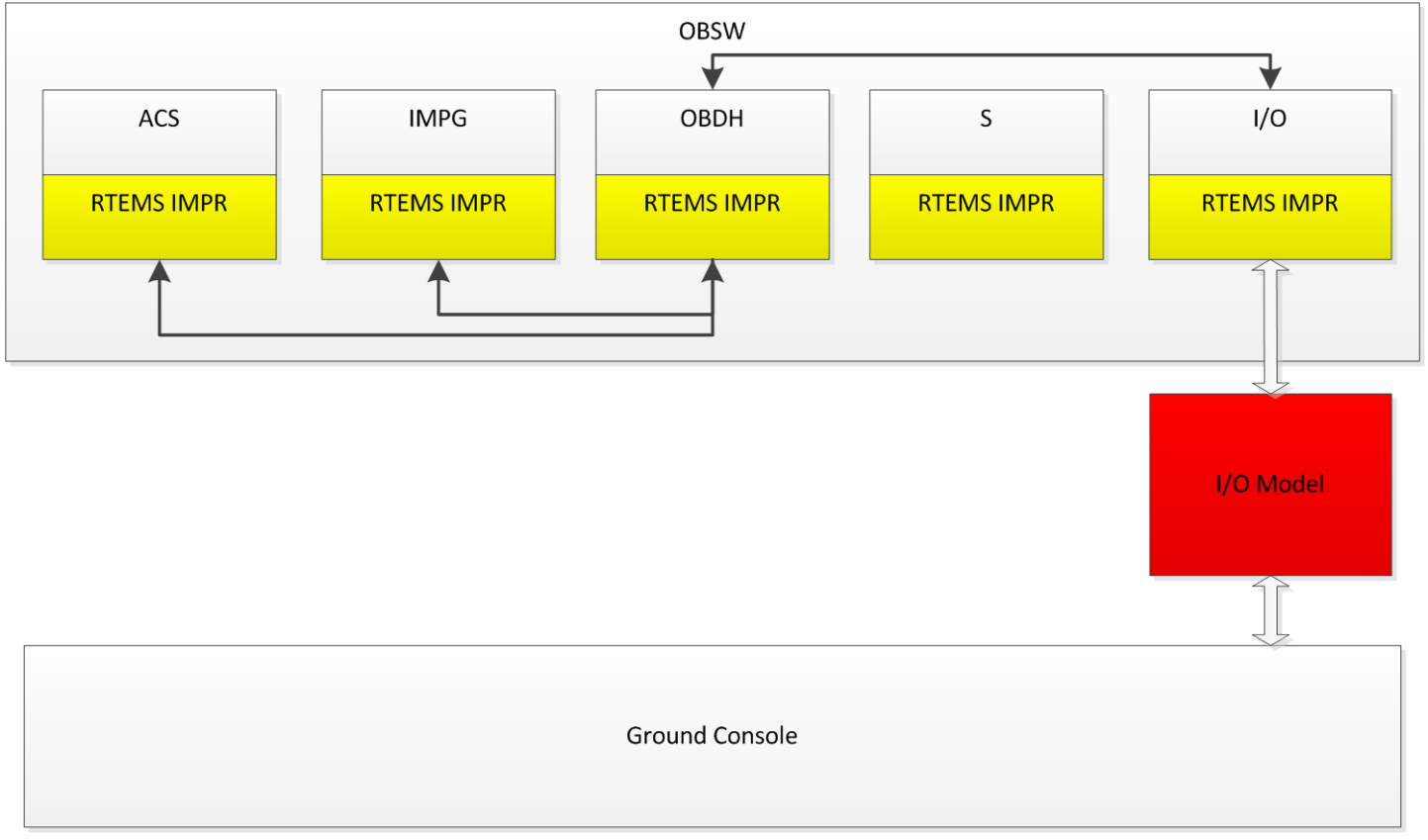
HAIR Hybrid Config (Source and Binary)



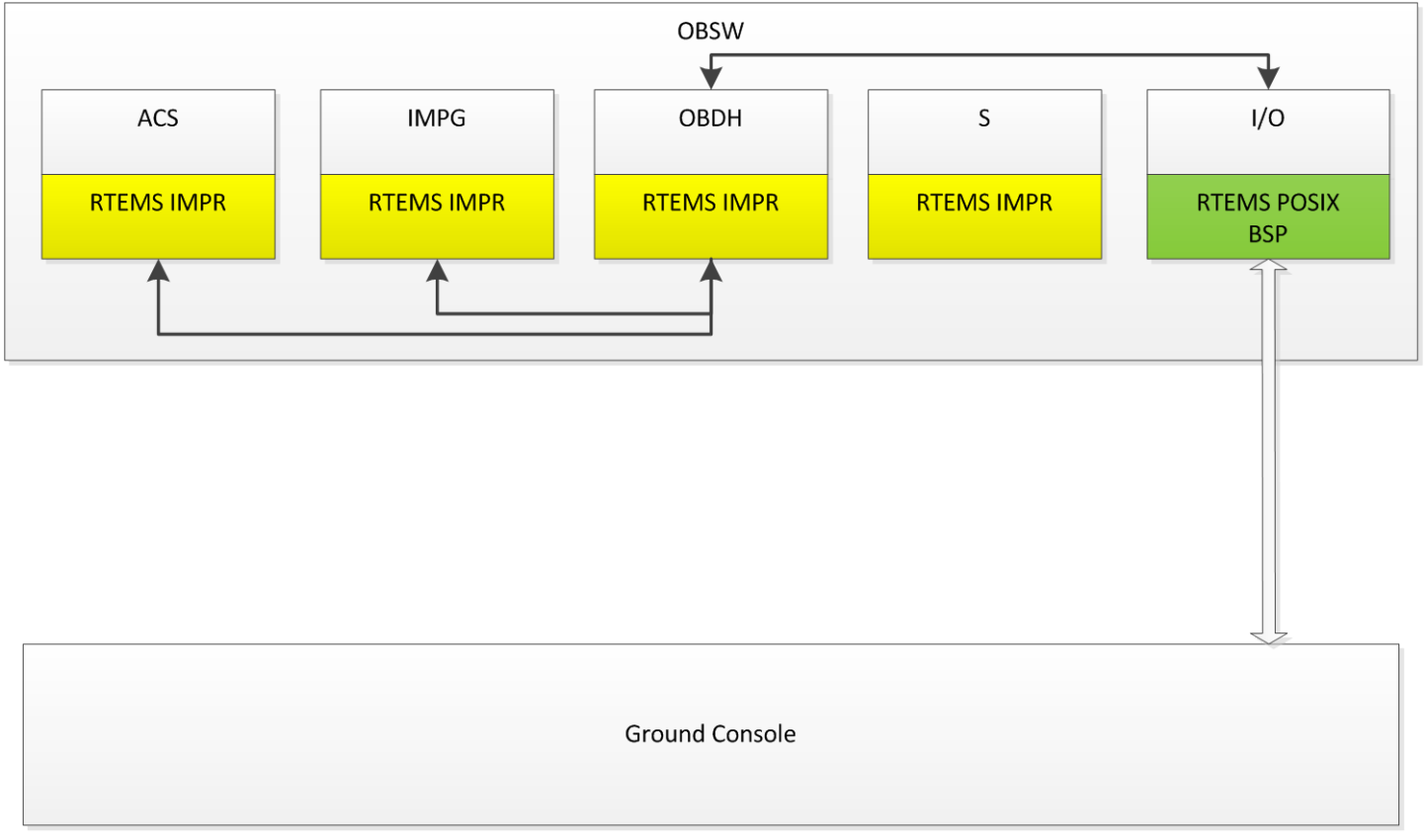
Use Case


Core 0
Core 1
Core 2
Core 3
IOP
ACS
S
10ms
10ms
30ms
Core 0
Core 1
Core 2
Core 3
OBDH
S
ACS
IMGP 1
IMGP 2
IMGP 3
IMGP 4
IOP
10ms
25ms
15ms

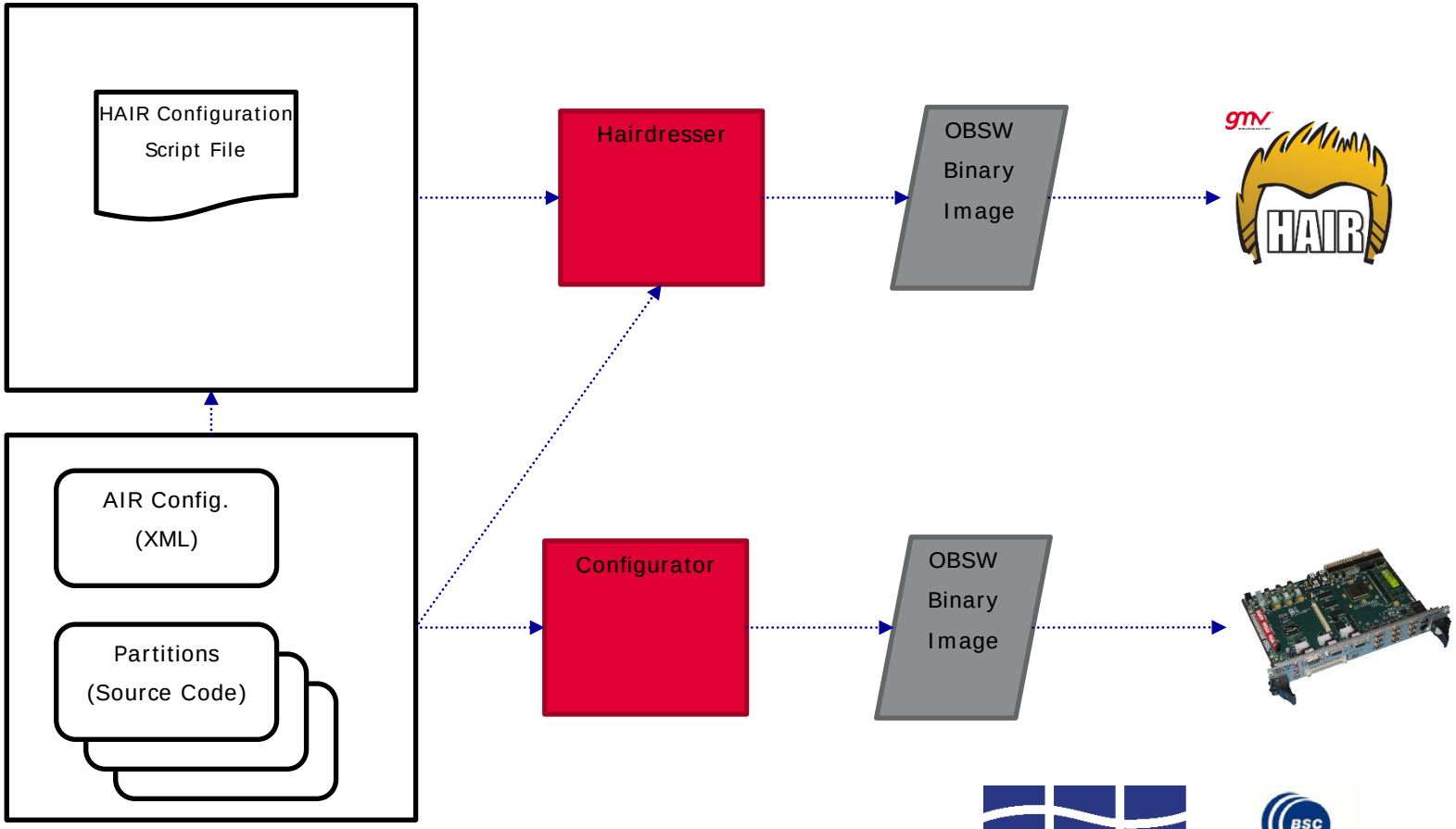
IO Model Support…



IO Model Support…



HAIR Transparency to AIR



Debugging in binary mode (breakpoint)

```
hair>partitions
CMD_INFO: partitions partitions

 List of Partitions:

   ID  -  Name
    1  -  OBDH          (binary code mode) use-case_air/obdh/p0.exe [0x41000000 - 0x421fffff]
    2  -  S             (binary code mode) use-case_air/s/p1.exe [0x41000000 - 0x413fffff]
    3  -  IOP           (source code mode) use-case_air/iop/p2.exe
    4  -  ImgP          (binary code mode) use-case_air/imgp/p3.exe [0x41000000 - 0x413fffff]
    6  -  ImgP2         (binary code mode) use-case_air/imgp2/p4.exe [0x41000000 - 0x413fffff]
    5  -  ACS           (binary code mode) use-case_air/acs/p5.exe [0x41000000 - 0x413fffff]

hair>break 2 41000af0
CMD_INFO: break 2 41000af0
```

Debugging in binary mode (breakpoint)

```
hair>go :: HPE : starting HPE
 :: HPE : hair>scheduler running (1000 us/tick)
 :: HPE : core 0 is context switching
 :: HPE : initializing schedule 1 - Waiting
 :: HPE : core 0 executing partition 5 - ACS (binary mode)
 :: HPE : core 1 is context switching
 :: HPE : core 1 executing partition 3 - IOP (source mode)
 :: HPE : core 2 is context switching
 :: HPE : core 2 is idle
 :: HPE : core 3 is context switching
 :: HPE : core 3 is idle
 :: HPE : core 0 is context switching
 :: HPE : core 0 executing partition 2 - S (binary mode)
Break at 0x41000af0 in partition 2

hair>step - Stepped 3000 cycles
hair>>>>S: Starting S_entry

hair>wmem 2 41014b33 7
CMD_INFO: wmem 2 41014b33 7

hair>mem 2 41014b30 4
CMD_INFO: mem 2 41014b30 4
0x00 0x00 0x00 0x07
```

Debugging with gdb in source mode

```
26278 pts/8    00:00:01 hair
26290 pts/8    00:00:02 p5.exe
26291 pts/8    00:00:00 p2.exe
26292 pts/8    00:00:00 p1.exe
```

```
gdb –p 26292
```

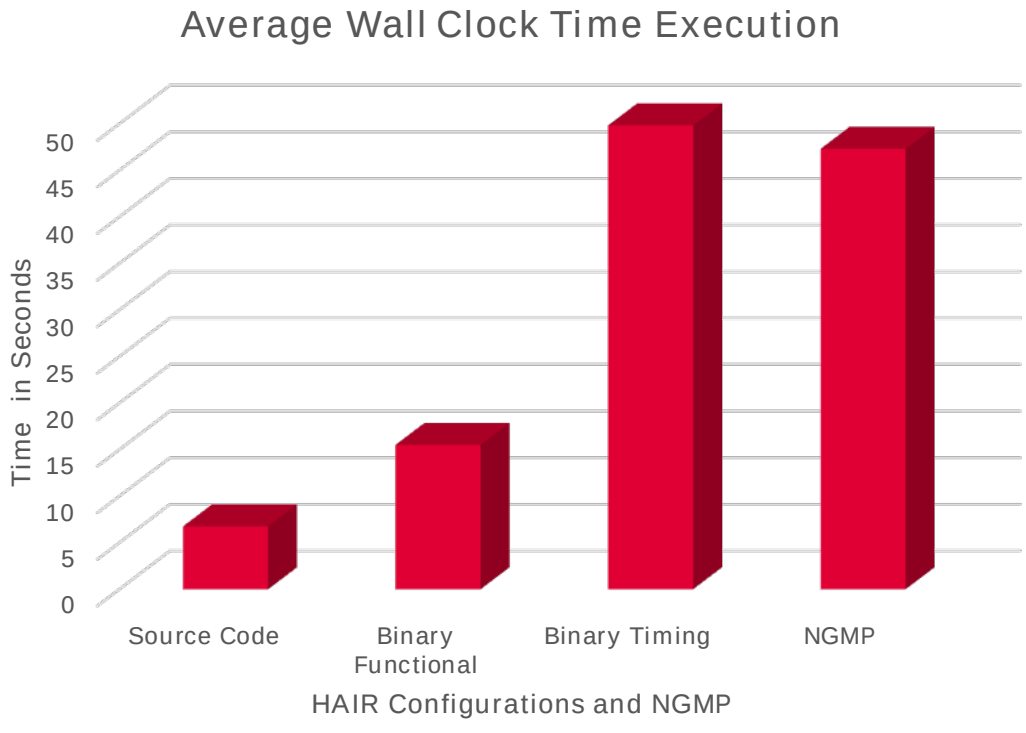
```
GNU gdb (GDB) Fedora 7.8.2-38.fc21
Copyright (C) 2014 Free Software Foundation, Inc.
License GPLv3+: GNU GPL version 3 or later <http://gnu.org/licenses/gpl.html>
...
Loaded symbols for /lib/ld-linux.so.2
0xf7727c10 in __kernel_vsyscall ()
```

```
(gdb) br supervisor_start_image_processing
Breakpoint 1 at 0x8048d8d: file s_main.c, line 126.
(gdb) cont
```

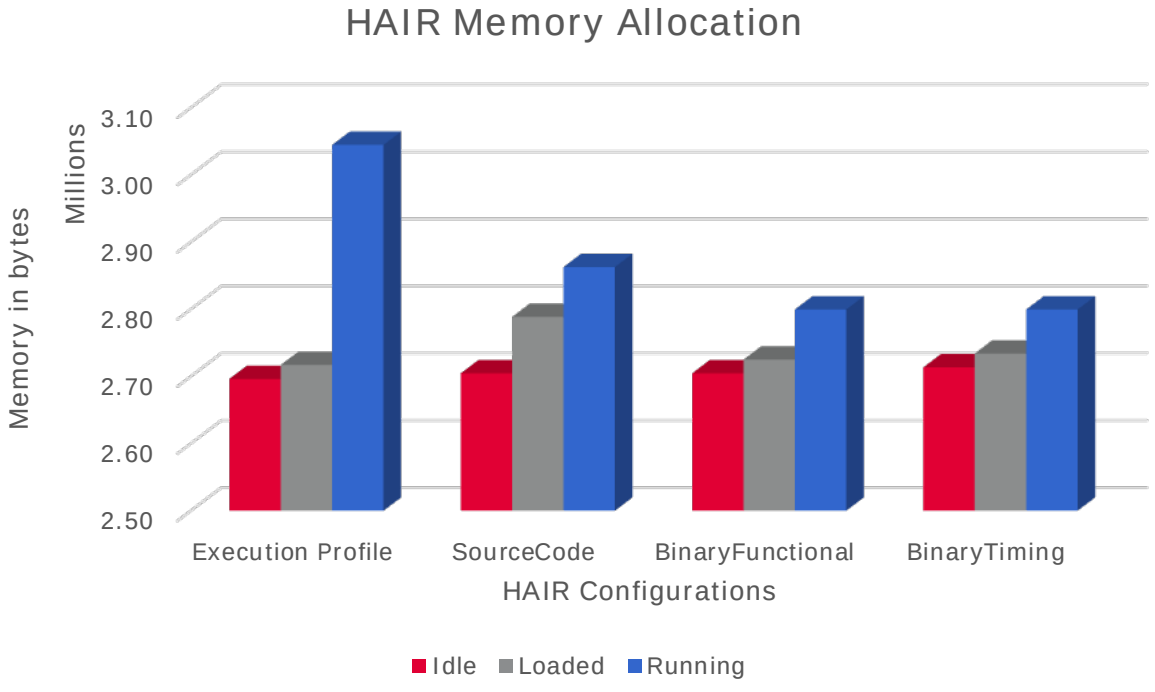
Other features

- All functionality is doable in a command line or scripted
- Interference models are configurable
- SMP2 2.0 Simulation integration
- It comes a with a set of sample templates
- It runs mono core OBSW

WALL CLOCK TIME MEASUREMENTS



MEMORY BUDGET

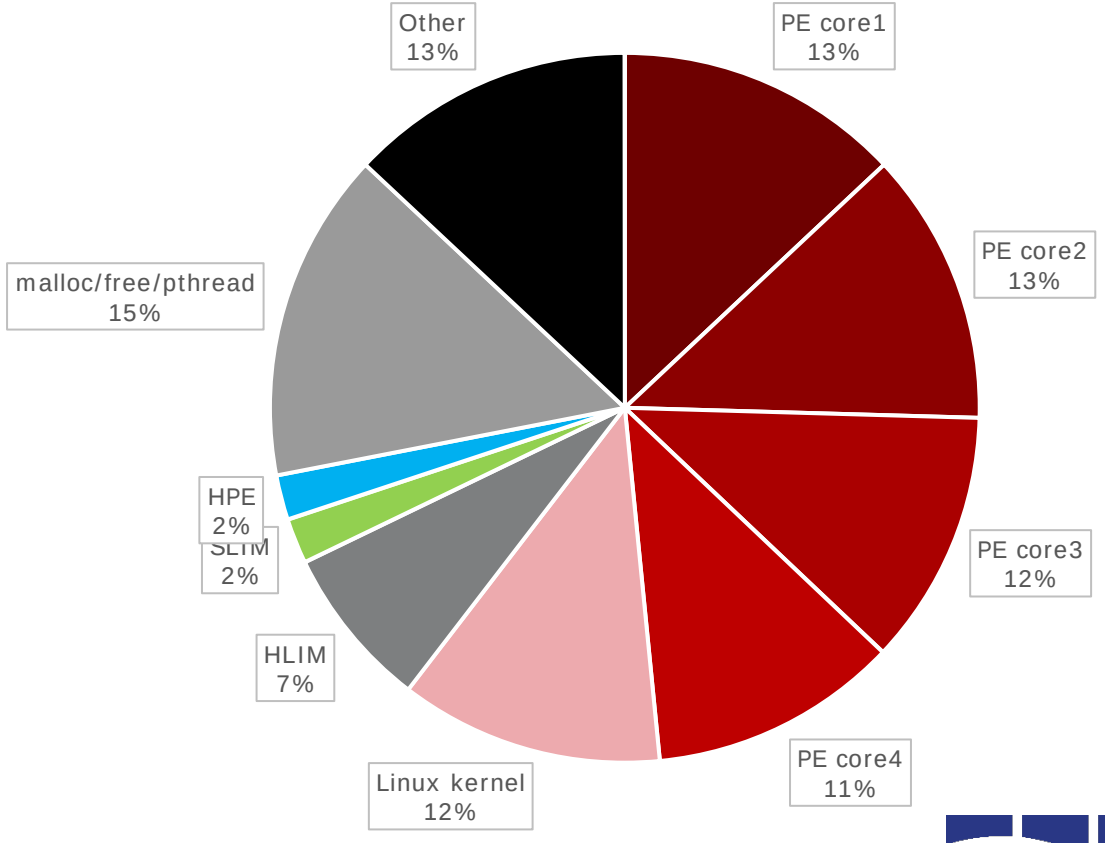


MEMORY ALLOCATION CAN BE IMPROVED

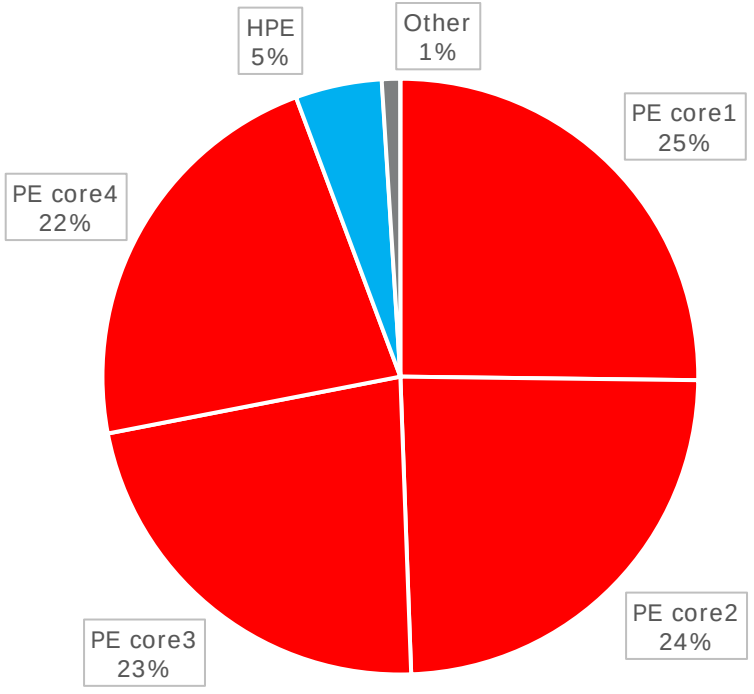
- There are 4 instances of ESOC Emu
- 11 libraries are clearly identified as quadrupled with “pmap”
- Source mode does need ESOC emu, but it is loading it anyway

sd	**/usr/lib64/librt-2.20.so**	7fab51cb5000 ---p 00007000	fd:00 1187203	2044	0	0	0		
sd	**/usr/lib64/librt-2.20.so**	7fab51eb4000 r--p 00006000	fd:00 1187203	4	4	4	0	0	
sd	**/usr/lib64/librt-2.20.so**	7fab51eb5000 rw-p 00007000	fd:00 1187203	4	4	4	0		
sd	**/usr/lib64/librt-2.20.so**	7fab51eb6000 r-xp 00000000	fd:00 1187027	88	64	6	64		

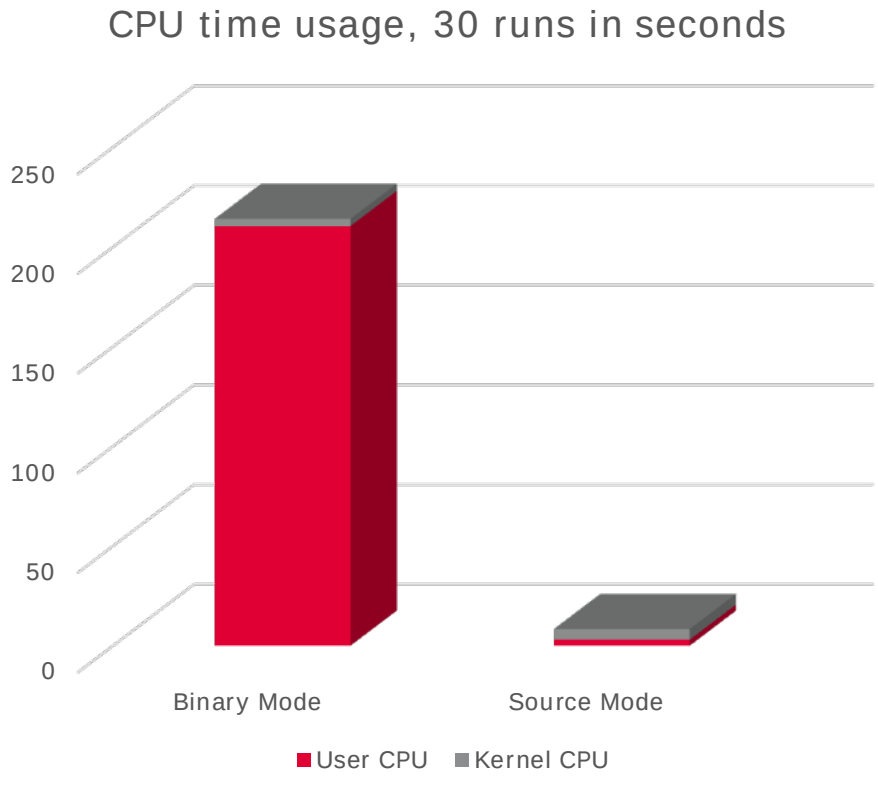
CPU BUDGET – Binary Timing Mode



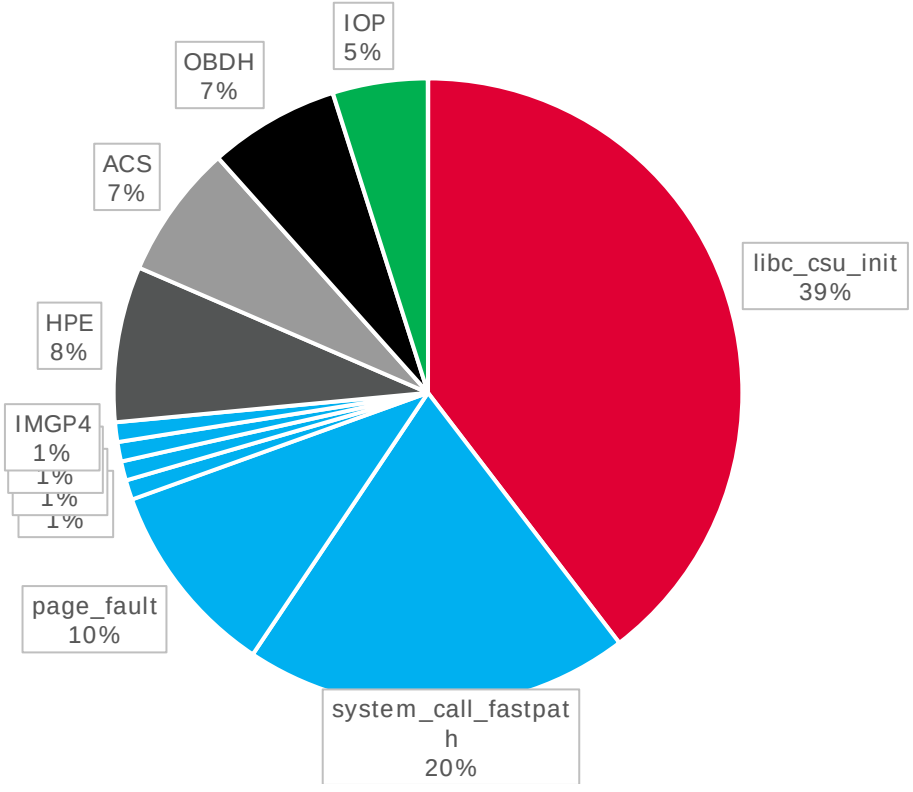
CPU BUDGET – Binary Functional Mode



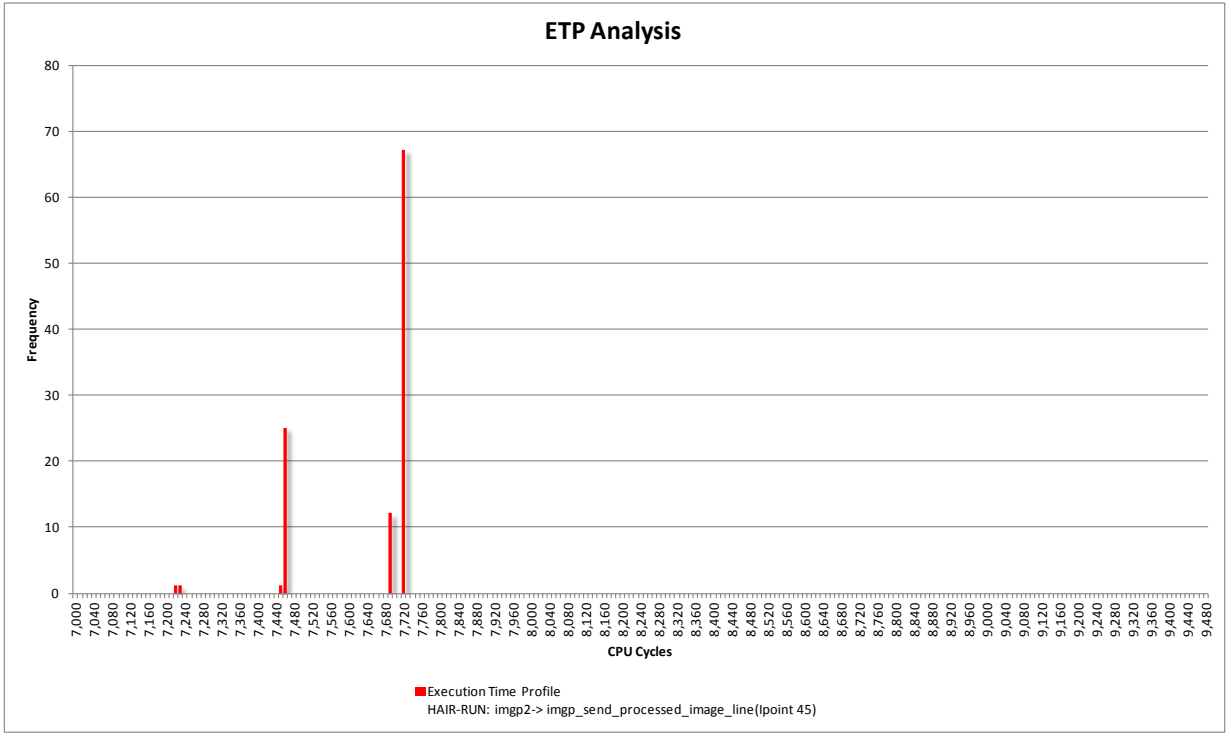
CPU Time – Source Mode vs Binary



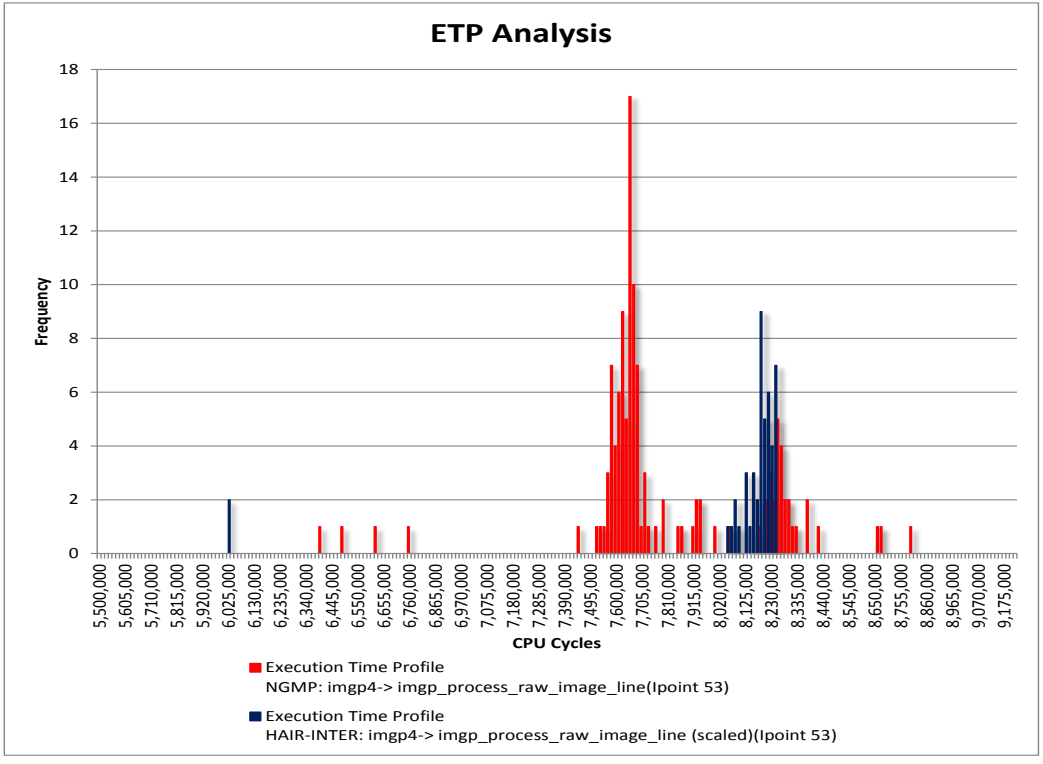
CPU BUDGET – Source Mode



Behavior Analysis without Interference



Behavior Analysis with Interference



Limitations

- Not all multi-core schedules are possibles
- Memory is an issue, high end workstation is needed.
- Running in VM timing precision is not achieved
- Running on Fedora 21, older linux distributions may not comply due to lack of some libraries e.g SLES

Room Improvement

There is room for improvement as identified in measurements

- HLIM can be less CPU heavy, with no I/O, malloc, free operations, it will increase behaviour precision and performance
- Cycle count discrepancy
- ESOC emulator is also improvable but taken as a black box, (out of scope)
- TSIM like user interface but yet unfriendly.

Ending remarks

- Now we can develop a space TSP OBSW without a NGMP board
- Likewise V&V activities
- AIR non space software also runs in HAIR
- Interference models are the way to go for emulating the behavior of multi-core
- Hybrid configuration allows develops one single partition without need of others
- Hybrid also allow to access data/items not yet available in SPARC.
- It is accelerating the development of new GMV TSP tools, because any linux machine can now be development machine for AIR.