Emulators of Future NGMP Multicore Processors

The processor emulator is a core component of the SVF and in many cases it drives the requirements and design of the rest of it. With next generation European multicore space processors it will no more be possible to simulate the on-board SW execution in real-time with the current type of emulators causing the need to improve further the processor emulator performance, leading to the need to investigate and adopt other technology solutions.
The HAIR project enables this possibility by presenting an hypervisor emulator capable of emulating future multicore processors, NGMP in concrete a SPARC V8 quad-core processor, based on the LEON4 and using Time and Space partitioning (TSP) technology based AIR hypervisor. HAIR therefore obtains the best benefits of multicore and TSP, being representative/accurate by emulating the behaviour of the NGMP in terms of timing and functionality running on ESOC EMU 2.0 processor emulator; and also being performant by compiling the embedded application, along with AIR hypervisor and RTEMS BSP natively on the host workstation.