taste
The Assert Set of Tools for Engineering

TASTE Tool-Chain improvements

Ellidiss Technologies

POLITECNICO DI MILANO

ISAE
Institut Supérieur de l'Aéronautique et de l'Espace

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- TASTE Model Verification (ISAE)

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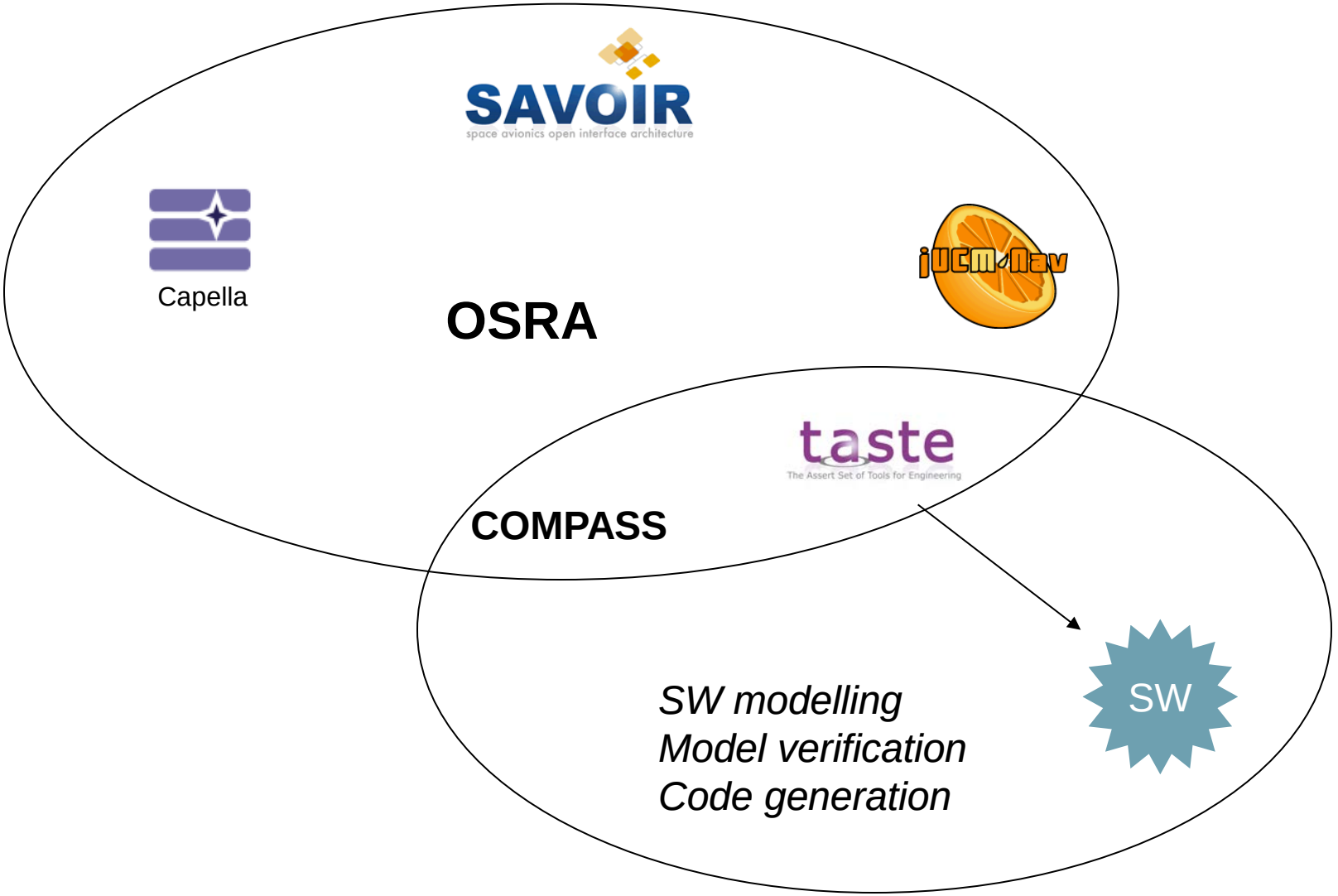
Overview

- Outcome of the ASSERT project (2004-2007)
- A complete development tool-chain for embedded applications
- Modelling:
  - Data modelling (ASN.1)
  - Software Architecture: TASTE Interface View (AADL)
  - Hardware Architecture: TASTE Deployment View (AADL)
  - Functional Behavior: OpenGEODE (SDL), Simulink, VHDL, Ada, C
- Real-Time code generation (Ada or C)
- Testing tools (MSC, Python)
- Supported by ESA and technology providers
- More information on: http://taste.tuxfamily.org

Eco-system


SAVOIR
space avionics open interface architecture
Capella
OSRA
jUCM-Nav
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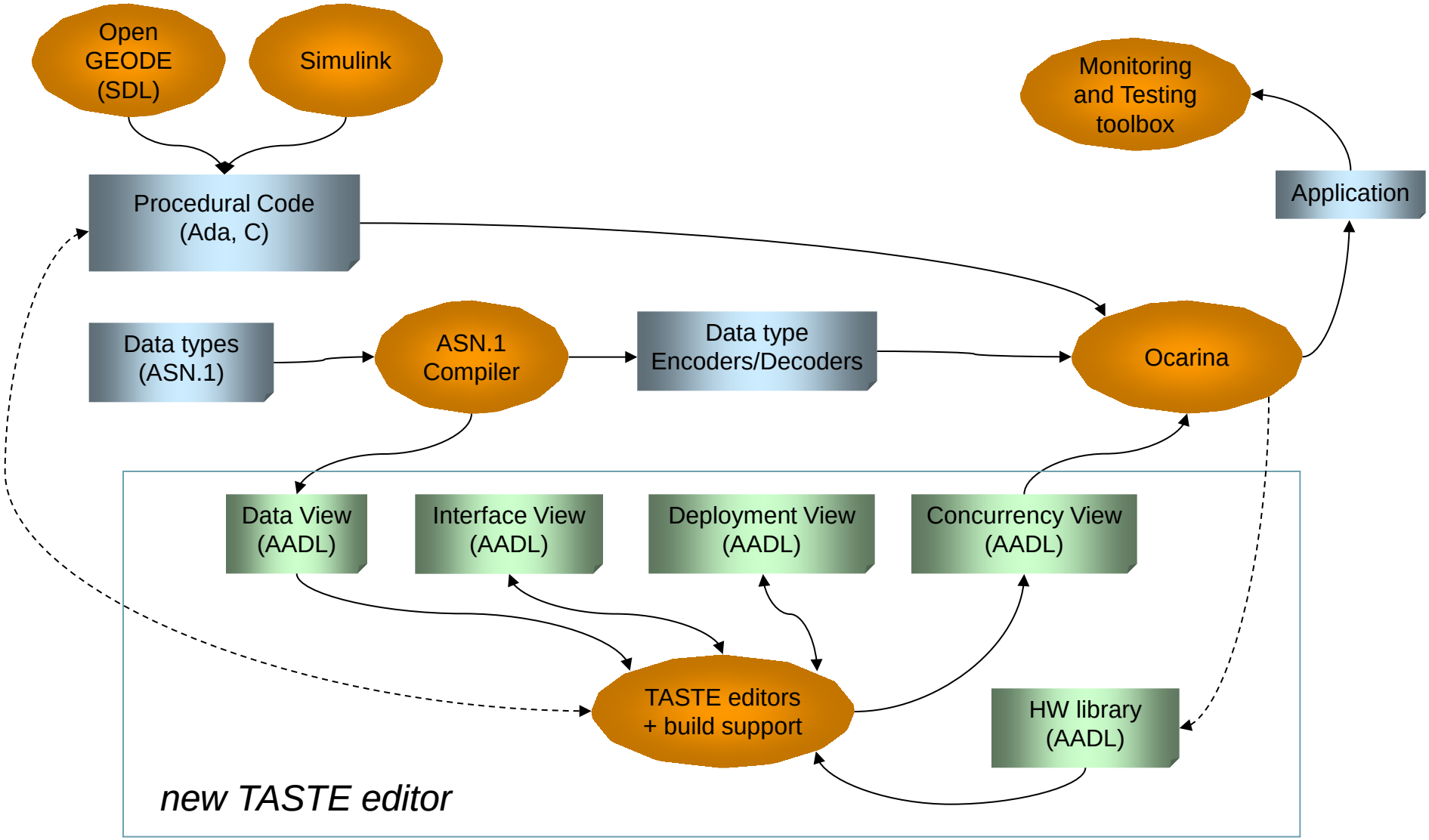
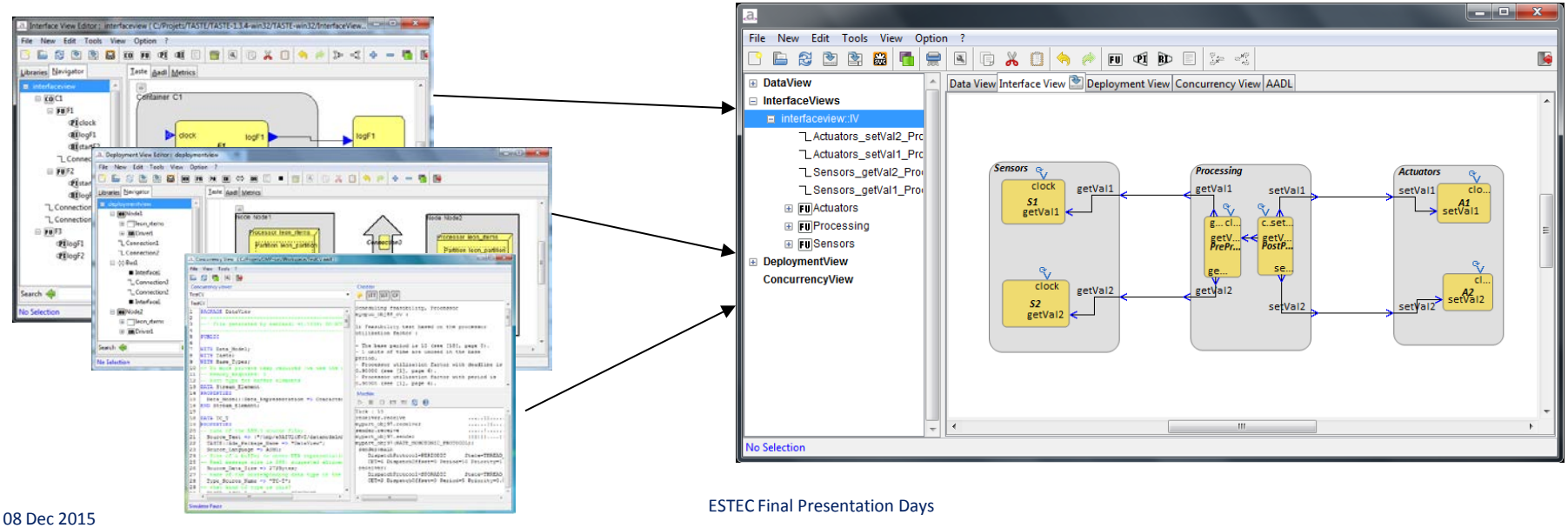
COMPASS
SW
SW modelling
Model verification
Code generation

Workflow


Open GEODE (SDL)
Simulink
Monitoring and Testing toolbox
Application
Procedural Code (Ada, C)
Data types (ASN.1)
ASN.1 Compiler
Data type Encoders/Decoders
Ocarina
Data View (AADL)
Interface View (AADL)
Deployment View (AADL)
Concurrency View (AADL)
TASTE editors + build support
HW library (AADL)
new TASTE editor

New IV-DV-CV editors

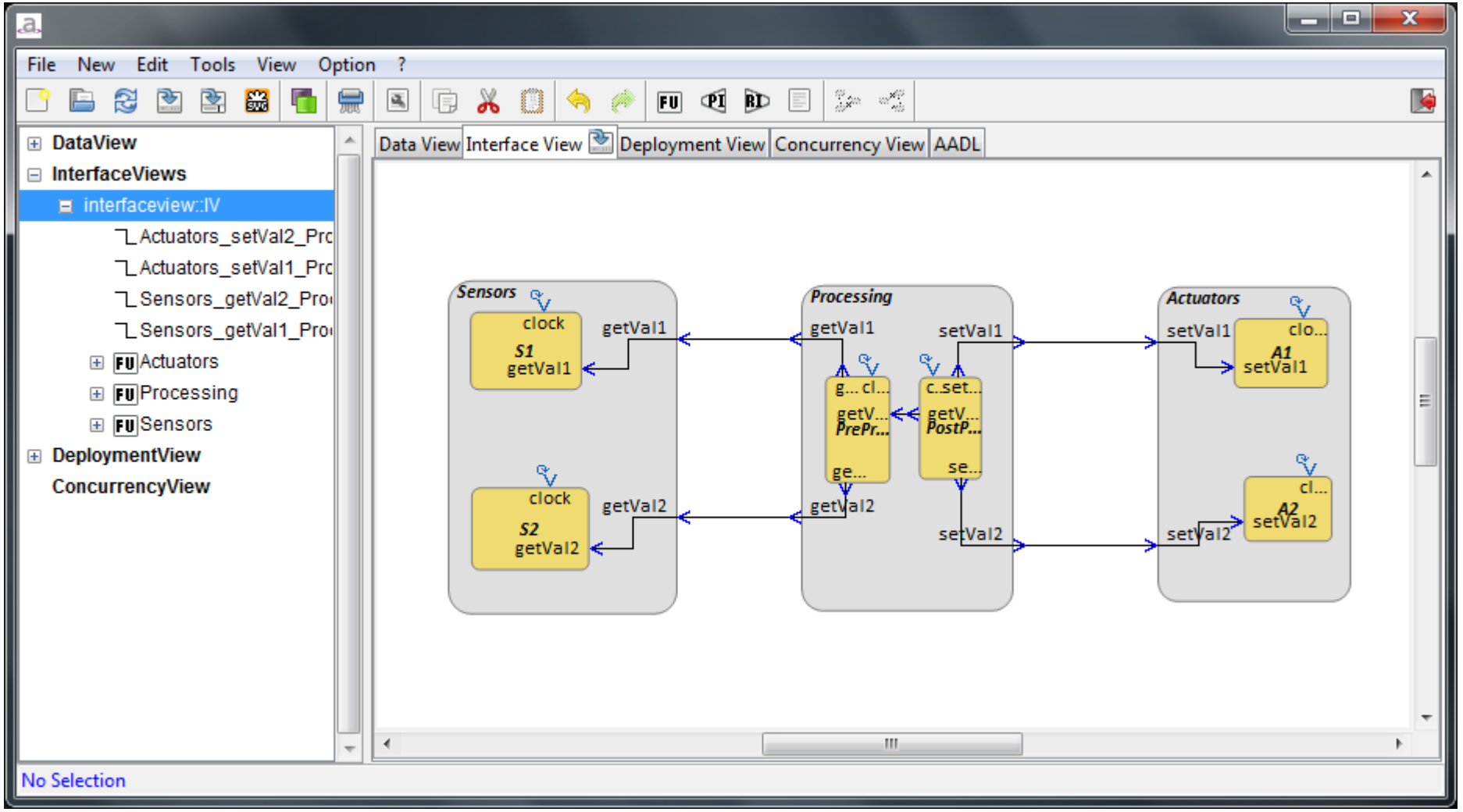
- Merging the IV, DV and CV editors into a single tool.
- Introducing hierarchical Functions in IV models
- Upgrading the CV editor with new versions of Cheddar (scheduling) and Marzhin (simulation)
- Factorizing the AADL toolbox (parsers, unparsers, checkers)



Interface View

- Software Architecture
- Main constructs of the IV model:
  - Functions, may be organized hierarchically
  - Interfaces (Provided and Required)
    - Give access to Operations (source code)
    - Cyclic, Sporadic, Protected or Unprotected
  - Parameters
    - Attached to Interfaces or shared within a Function
    - Typed by ASN.1 types defined in the DataView
  - Connections
    - Client-Server paradigm

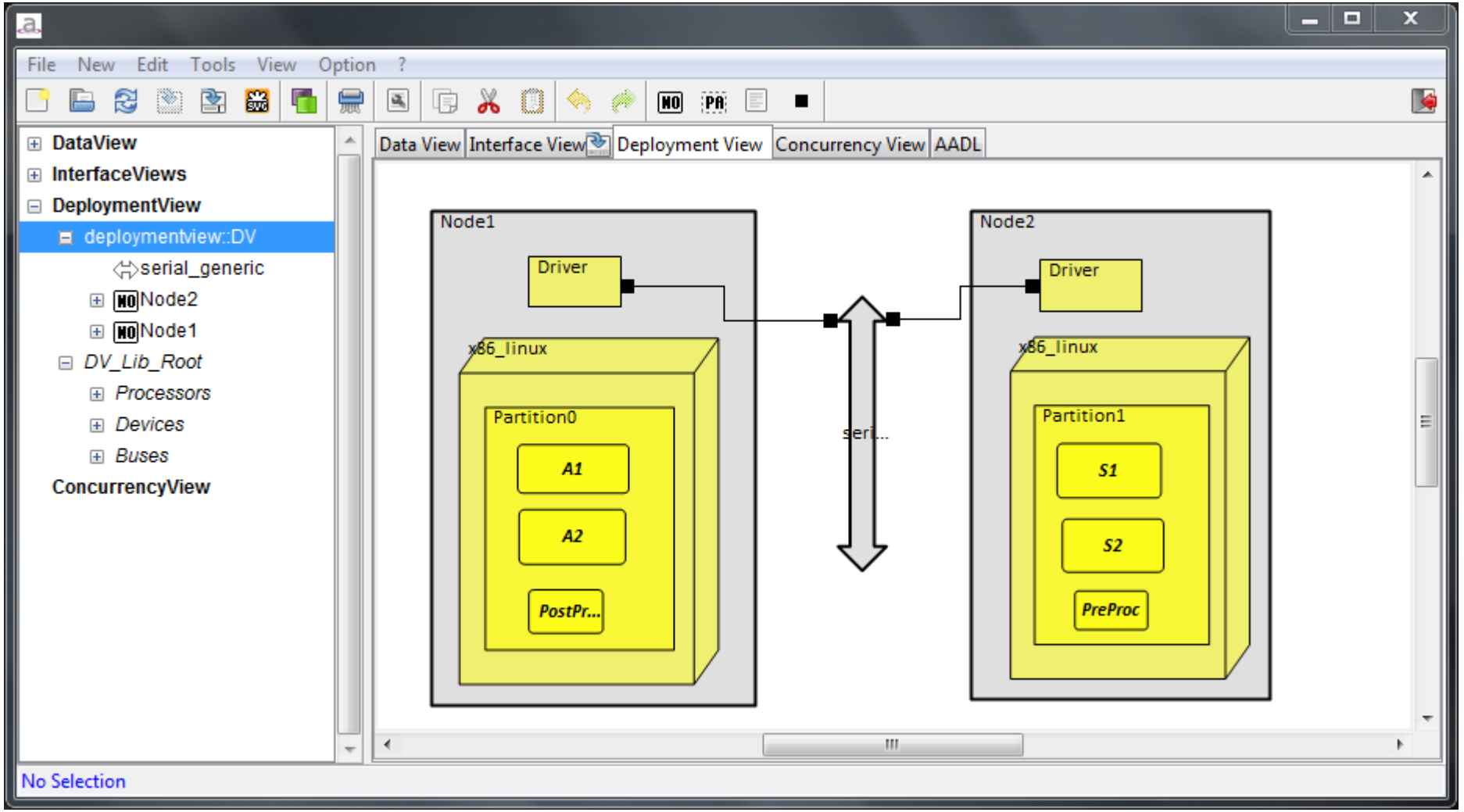
IV editor


File New Edit Tools View Option ?
DataView
InterfaceViews
interfaceview::IV
Actuators_setVal2_Prc
Actuators_setVal1_Prc
Sensors_getVal2_Pro
Sensors_getVal1_Pro
Actuators
Processing
Sensors
DeploymentView
ConcurrencyView
Data View
Interface View
Deployment View
Concurrency View
AADL
Sensors
clock
S1
getVal1
getVal1
clock
S2
getVal2
getVal2
Processing
getVal1
setVal1
getVal2
setVal2
Actuators
setVal1
A1
setVal1
setVal2
A2
setVal2
No Selection

Deployment View

- Hardware Architecture and SW-HW binding
- Main constructs of the DV model:
  - Nodes
    - Processor containing Partitions
    - Bus Drivers
  - Buses
  - Connections
    - Bus access for Drivers and Devices
    - Allocation of IV Function onto DV Partitions
    - Allocation of IV Connections onto DV Buses

DV editor


File New Edit Tools View Option ?
DataView
InterfaceViews
DeploymentView
deploymentview::DV
serial_generic
Node2
Node1
DV_Lib_Root
Processors
Devices
Buses
ConcurrencyView
Data View
Interface View
Deployment View
Concurrency View
AADL
Node1
Driver
x86_linux
Partition0
A1
A2
PostPr...
seri...
Node2
Driver
x86_linux
Partition1
S1
S2
PreProc
No Selection

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Concurrency View

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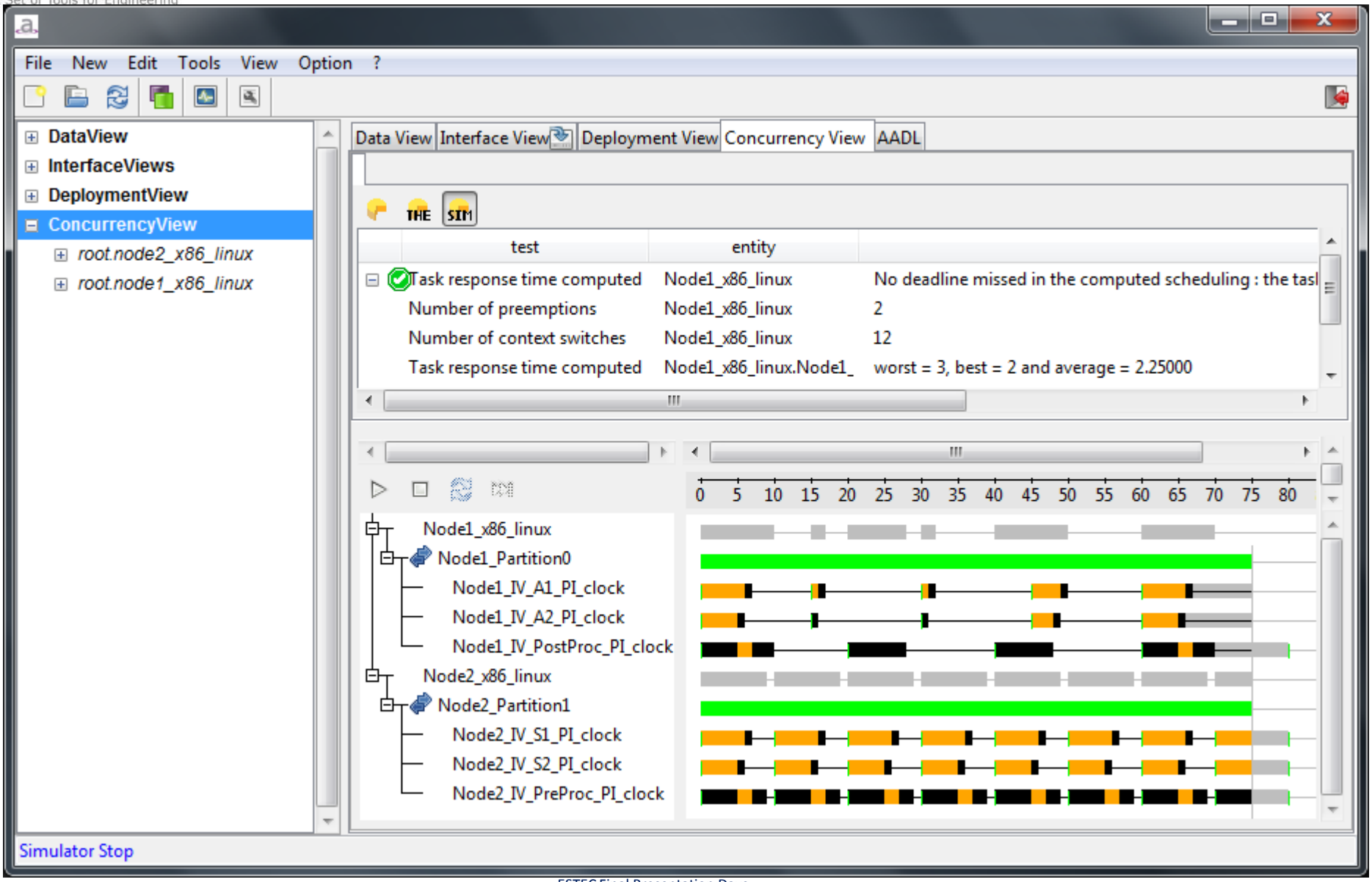
- Result of an AADL to AADL model transformation
- Real-time architecture:
  - Processes, Threads, Subprograms, Shared Data
  - Ready for timing analysis and code generation
- Timing Analysis
  - Scheduling analysis with Cheddar (University of Brest)
  - Model simulation with Marzhin (Ellidiss & Virtualys)
- Code Generation with Ocarina (ISAE)
  - Merged AADL model (DataView+IV+DV+HwLibraries+CV)
  - Ada or C RTOS compliant code generation with PolyORB-HI

CV editor


File New Edit Tools View Option ?
DataView
InterfaceViews
DeploymentView
ConcurrencyView
root.node2_x86_linux
root.node1_x86_linux
Data View
Interface View
Deployment View
Concurrency View
AADL
THE
SIM
test
entity
Task response time computed
Node1_x86_linux
No deadline missed in the computed scheduling : the tasl
Number of preemptions
Node1_x86_linux
2
Number of context switches
Node1_x86_linux
12
Task response time computed
Node1_x86_linux.Node1_
worst = 3, best = 2 and average = 2.25000
0 5 10 15 20 25 30 35 40 45 50 55 60 65 70 75 80
Node1_x86_linux
Node1_Partition0
Node1_IV_A1_PI_clock
Node1_IV_A2_PI_clock
Node1_IV_PostProc_PI_clock
Node2_x86_linux
Node2_Partition1
Node2_IV_S1_PI_clock
Node2_IV_S2_PI_clock
Node2_IV_PreProc_PI_clock
Simulator Stop

Demonstration

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TASTE usage

- Robotics Applications Development (SARGON)
- Payload Flight Software
- Tooling for the PUS-C standard
- Educational and technology demonstration
- Onboard SW fast prototyping and validation
- …

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Future work

- Simulation at model level
- More verification
- Improved user experience
- Integration of other formal methods (VDM)
- Tool pre-qualification
- Better integration with OSRA and CAPELLA
- Safety/Security analysis (link with COMPASS)