TASTE evolution and Integration of High Level Synthesis Flow

TASTE toolchain partially supported the integration of hardware accelerators by automatically generating the hardware interface and the corresponding driver of the functions that have been mapped to hardware. On the contrary, the accelerator implementations (i.e., the HDL code to be synthesized) had to be provided by the designer. Since the generation of such type of implementations is typically a hard task for software developers, High Level Synthesis has been introduced. It consists of a set of methodologies aimed at automatically generating the HDL implementation of a function starting from its high level description (i.e., C source code implementation).

In this project, bambu, an open source High Level Synthesis tool developed at Politecnico di Milano has been modified to generate hardware architectures targeting the TASTE infrastructure. The tool starts from the formal specification of the application (interface and data views) and identifies which are the functions to be implemented on the FPGA. The source code of these functions (C or SDL) is then automatically synthesized in a set of custom hardware accelerators compatible with the TASTE FPGA driver interface. Finally, the whole FPGA architecture including this components is also generated.

In parallel to this work on hardware-software co-design, the latest evolutions of the TASTE editors will be presented by Ellidiss ; in particular the support for hierarchical systems, library of components, scheduling analysis with the latest version of Cheddar and Marzhin, and better integration of the TASTE front-ends in a single tool.