SEFUW: SpacE FPGA Users Workshop, 3rd Edition

Tuesday 15 March 2016 - Thursday 17 March 2016

European Space Research and Technology Centre (ESTEC)

SEFUW 2016 is organised with the support from CNES CTT and ESA's Data System Division

Tuesday 15 March 2016

Registration and Early Morning Networking Break sponsored by CNES CCT and ESA's Data System Division (09:30 – 10:00)

Welcome to SEFUW 2016 (10:00 - 10:25)
Presenter: Mr. DANGLA, David (CNES); Mr. MERODIO CODINACHS, David (ESA)

Session: Design Experiences (10:25 – 12:10)
Chair: *Mr. MERODIO CODINACHS, David (ESA)*

	10:25	**Implementation of Space-Industry IP : A Comparison of Space-Grade FPGAs** *Presenter: Dr. BEDI, Rajan (Spacechips Ltd.)* The number and diversity of space-grade FPGAs offer many options when architecting satellite sub-systems. One-time programmable anti-fuse, flash and SRAM-based technologies, each with unique fabrics, present many interesting trade-offs when selecting the most appropriate device for your next mission. Today, space-grade FPGAs are formally available from 350 µm to 28 nm nodes with advertised speeds ranging from 50 to 800 MHz. On-board storage varies from 55 kB to 50 MB with the latest devices offering high-speed serial links with data rates of 8.5 Gbps. For some spacecraft sub-systems, *e.g.* high throughput payloads or localised control of a power supply, the system requirements quickly dictate the choice of FPGA. For some satellites, OEMs have re-used devices from previous programs which in some cases has proven to be cost effective, however, for others, this decision has resulted in expensive re-design, late delivery of hardware and over-budget projects. To avoid unnecessary over-design, some manufacturers of satellite sub-systems have started to compare space-grade FPGAs during the system architecture phase to allow them to make an informed decision and select the most appropriate device given their mission constraints, *e.g.* power consumption, cost, performance, reliability etc ... FPGA vendors offer unique device fabrics with each supplier promoting differently the capability and the number of logic resources offered by their parts. Which FPGA is the most appropriate for your next mission? This paper compares the FPGA implementation of IP used by the space industry and offers an independent view of selecting the right device for your next spacecraft sub-system.
	10:55	**FPGA development flow for future large space FPGA** *Presenter: Mr. MANNI, Florent (CNES DC/TV/IN)* The FPGA available for Rad-tolerant or Rad-Hard applications are quite small (with regard to their commercial brothers). Some are SRAM based, many are antifusible based. The development flow described inside the ECSS-Q-60-02 standard is well fitted for this kind of targets. The next generation of FPGA for space application will include bigger FPGA matrix most of them SRAM or flash based. The mix between biggest and reprogrammable matrix will lead to longer FPGA development and new strategies to handle it. This kind of development will match less easily with the ECSS standard. During this presentation two different FPGA development examples will be described: one using FPGA Proasic3 and the other using the SOC Zynq.
	11:20	**Prototyping a SOC on RTAX4000D for Solar Orbiter's Low Frequency Receiver.** *Presenter: Mr. JEANDET, Alexis (Plasma Physics Laboratory)* Many space instruments using FPGA rely on the RTAX family, from the RTAX-250 to the RTAX-2000D but none of them embed a **RTAX-4000D**. For the first a RTAX-4000D will be onboard the **Solar Orbiter** (http://sci.esa.int/solar-orbiter/) spacecraft in the Low Frequency Receiver instrument (**LFR**) developed at the Laboratory of Plasma Physics (LPP) (http://www.lpp.fr/). The LFR is in charge of digitizing the E and B fields below 10kHz and processing them to extract basic parameters from the solar wind. In fact this need more RAM and logical resources than the RTAX2000D can provide, the reason for which the LPP decided to choose the RTAX4000D. In this workshop the LFR's FPGA prototyping will be presented from custom solderless socket solution to high level SOC debug and verification.
	11:45	**LEON3/GRLIB for Space-Grade Programmable Devices Update and Roadmap** *Presenter: Mr. ANDERSSON, Jan (Cobham Gaisler AB)* Cobham Gaisler develops the LEON3FT SPARC V8 fault-tolerant microprocessor that is

		available both as IP cores part of an IP library (GRLIB) that allows users to design their own custom system-on-chip (SoC) designs, and also as part of ready-made designs and devices. The GRLIB library currently provides template designs that allow users to target Xilinx Virtex-5QV, Microsemi RTAX, RT ProASIC3 and RTG4. The presentation will provide an update on the latest features supported and give a roadmap for future updates.

Session: Industrial Experiences (12:10 – 12:35)
Chair: *Mr. MERODIO CODINACHS, David (ESA)*

	12:10	**Feedback on Xilinx Virtex-5QV FPGA** *Presenter: Mr. SEYCHAL, Florian (THALES ALENIA SPACE FRANCE)* A designer's approach is done on the last space-grade FPGA provided by Xilinx: Virtex-5QV. The presentation gives details of features, performances and power consumptions of real designs developed in Thales Alenia Space. The methodology used for Xilinx FPGAs is also presented. Finally, some recommendations are delivered for designers.

Session: FPGAs: High Performance (12:35 – 13:00)
Chair: *Mr. MERODIO CODINACHS, David (ESA)*

	12:35	**SpaceWire and SpaceFibre on the Microsemi RTG4 FPGA** *Presenter: Mr. MCCLEMENTS, Chris (STAR-Dundee)* To explore the implementation of SpaceFibre and SpaceWire in the new Microsemi RTG4 FPGA, a demonstration system has been developed which implements the STAR-Dundee SpaceWire and SpaceFibre IP cores on the RTG4 development kit. In addition to the RTG4 development kit, the demonstration system uses the STAR-Dundee SpaceFibre and SpaceWire FMC interface card, STAR Fire SpaceFibre interface and diagnostics unit, and a SpaceWire Brick Mk3 USB. The system interconnects between RTG4 development boards using the SpaceFibre and SpaceWire interfaces of the FMC interface boards. Each FMC board features two SpaceFibre interfaces and four SpaceWire interfaces. The RTG4 FPGA design has two SpaceFibre interfaces running at a bit rate of 2.5 Gbit/s and four SpaceWire interfaces running at 200 Mbit/s. The SpaceFibre interfaces are configured with eight virtual channels, with virtual channels 0 to 3 connected to the SpaceWire interfaces on one interface and virtual channels 4 to 7 interconnected between the SpaceFibre interfaces. The design makes use of the new features of the RTG4 including the SpaceWire clock recovery circuit and the high speed SERDES interfaces. The demonstrator system uses a STAR Fire as a high speed SpaceFibre data generator sending and receiving data through the RTG4 boards to saturate the SpaceFibre link. Another STAR Fire unit can be used in analyser mode to capture data travelling over SpaceFibre. In parallel, one Brick Mk3 is used as a lower speed SpaceWire data source, sending data in one direction to a remote computer. At the same time, this remote computer is sending a webcam video feed through SpaceWire back to the SpaceWire source PC. The low speed SpaceWire traffic generated by the Brick MK3 is sent and received over the same SpaceFibre link as the high speed data traffic. Thanks to the inbuilt QoS for every virtual channel, the low speed traffic is not affected by the high speed traffic used to saturate the link, as they travel over different virtual channels. The use of the RTG4 with the SpaceFibre and SpaceWire IP cores provides a powerful platform for future spacecraft on-board instrument control, data handling and data processing. Furthermore, due to the inbuilt Quality of Service (QoS) and Fault Detection and Isolation (FDIR) capabilities, SpaceFibre allows the reduction of system complexity, deterministic data delivery and the substantial reduction of cable harness mass.

Networking Luncheon (13:00 – 14:20)

Session: Fault Tolerance Methodologies and Tools (14:20 – 15:35)
Chair: *Mr. DANGLA, David (CNES)*

	14:20	**Configuration Scrubbing and Mitigation Approaches for the Zynq System-on-Chip** *Presenter: WIRTHLIN, Mike (Brigham Young University)* The Xilinx Zynq programmable system-on-chip offers new capabilities for spacecraft systems by integrating two ARM A9 processors along with programmable logic on the same silicon die. Tightly coupling embedded processors with a programmable logic fabric facilitates hybrid computing systems that use the processors for higher-level sequential processing and the programmable logic for parallel computing, low-level I/O, and stream processing's. A number of

		CubeSat satellite systems are planning on exploiting this novel architecture. Like all SRAM programmable logic, the FPGA resources on the Zynq processor are susceptible to single-event upsets (SEU). Conventional SEU mitigation techniques such as configuration scrubbing and TMR are necessary for protecting the programmable logic within the Zynq. This presentation will summarize a number of novel techniques for configuration scrubbing using the new PCAP configuration interface. In addition, a hybrid scrubbing system that exploits both the internal scan feature of the 7 series FPGA as well as the PCAP interface will be described.
	14:45	**SET effects analysis and mitigation on Flash-based FPGAs** *Presenter: Prof. STERPONE, Luca (Politecnico di Torino)* Flash-based Field Programmable Gate Arrays (Flash-based FPGAs) are becoming more and more interesting for safety critical applications due to their re-programmability features while being non-volatile. However, Single Event Transients (SETs) in combinational logic represent their primary source of critical errors since they can propagate and change their shape traversing combinational paths and being broadened and amplified before sampled by sequential Flip-Flops. In this paper the SET sensitivity of circuits implemented in Flash-based FPGAs is mitigated with respect to the working frequency and different FPGA routing architecture. We outline a parametric routing scheme and placement and routing tools based on an iterative partitioning algorithm able to generate high performance circuits by reducing the wires delay and reducing the SET sensitivity. The efficiency of the proposed tools has been evaluated on a Microsemi Flash-based FPGA implementing different benchmark circuits including a RISC microprocessor. Experimental results demonstrated the reduction of SET sensitivity of more than 30% on the average versus state-of-the-art mitigation solutions and a performance improvement of about 10% of the nominal working frequency.
	15:10	**FT-UNSHADES2: the User Friendly Framework as an interface for designer support** *Presenter: Dr. HIPÓLITO, Guzmán-Miranda (Universidad de Sevilla)* FT-UNSHADES2 is a framework dedicated to fault injection in both ASIC netlists and FPGA devices. This system has been conceived to perform, in the same environment, large injection campaigns and detailed analysis without additional user efforts. The team at Universidad de Sevilla has created a system that is remotely accessible, avoiding the necessity of having the hardware device present. Its remote access via web can be installed, for example, in the intranet of a company. The system allows with the same framework, both large fault injection campaigns and detailed analysis to study the effects of single faults. The design preparation procedure, and few examples of use, ASIC campaign mode, ASIC detailed analysis and FPGA campaign mode are three ways of using FTU2, integrated in the same framework. In this presentation we describe the new framework for making fault injection in different cases and procedures. The system in Sevilla is now accessible by all users because is offered as online access.

Session: Reconfigurability (15:35 – 16:00)
Chair: *Mr. DANGLA, David (CNES)*

	15:35	**Dyplo: software driven threaded FPGA development using partial reconfiguration techniques** *Presenters: Ms. RUTTEN, Inge (Topic Embedded Systems), Mr. VAN DEN HEUVEL, Dirk (Topic Embedded Products)* Dyplo is a DYnamic Process LOader, enabling software-like programming capabilities on an FPGA such as threading, dynamic process switching and on-the-fly context switching. This allows seamless integration of FPGA logic in a typical software application without the need of deep FPGA design knowledge. A software API gives you full control over functionality run on the FPGA as well as the data transaction of processes running on the FPGA and CPU. The concept behind Dyplo makes use of partial reconfiguration technology, supporting currently only Xilinx FPGA technology. Using an infrastructure that spans both the FPGA and operating system of the processor is a unique solution. This creates all kinds of special capabilities such as functional redundancy, self-repairing systems and time-division-multiplexing of FPGA fabric. This presentation will give you more insight in the concept, a description of the demonstration we will show and a glance of the road ahead where Topic goes with this concept. Topic Embedded Products delivers embedded solutions to accelerate our customers development, forming a complete ecosystem of hardware and software building blocks which are all combinable and compatible. Topic is also one of 10 premier partners world-wide of Xilinx.

Networking Coffee Break sponsored by CNES CCT and ESA's Data System Division (16:00 – 16:30)

Demo Session and Cocktail Reception sponsored by CNES CCT and ESA's Data System Division (16:30 – 18:30)
Chair: *Mr. DANGLA, David (CNES)*

Wednesday 16 March 2016

SEFUW Intro – Opening Remarks (08:50 - 09:00)
Presenter: Mr. DANGLA, David (CNES); Mr. MERODIO CODINACHS, David (ESA)

Session: FPGA Vendors (09:00 – 10:30)
Chair: *Mr. FERNANDEZ-LEON, Agustin (ESA)*

09:00	**Microsemi RTG4 FPGAs – Product Overview, Update on Radiation and Reliability Testing** *Presenter: Mr. O'NEILL, Ken (Microsemi)* Dramatic increases in sensor resolution in remote-sensing space payloads are causing a processing bottleneck, as downlink bandwidth is not keeping pace. Operators require on-board processing so that satellites send processed information, not just raw data. It is a growing challenge for the designers of the hundreds of remote sensing satellite payloads launched each year. Microsemi's RTG4 Flash-based radiation tolerant FPGAs are now being applied to the problem, combining high-speed signal processing with special built-in radiation mitigation techniques to keep systems operational in harsh radiation environments. In addition, these Flash FPGAs maintain low static power, and contribute significant dynamic power savings. With more than 150,000 logic elements and up to 300 MHz system performance, this new class of radiation tolerant FPGA incorporates significantly more registers, combinatorial logic, DSP Mathblocks, and transceivers than were previously available with any radiation-tolerant FPGA technologies. This presentation will provide an overview of the architecture and technology of the RTG4 FPGAs, and will then cover the latest information on reliability testing and radiation effects analysis. Product qualification schedules and availability of flight units will also be discussed.
10:00	**ATMEL AT40K RHBD FPGA last news** *Presenter: Mr. BANCELIN, Bernard (ATMEL Nantes S.A.S.)* ATMEL keep up on enhancing its AT40K radiation-hardened FPGA family composed of the AT40K, ATF280, AFee560 and ATF697 devices. SpaceFpgaDesigner, the family design software suite, has been significantly enhanced, including Mentor Precision and Figaro latest releases. The new Hardware Macro flow now offers an optimally placed and routed, ready to use, 1553 IP. Analysis are on-going for SpaceWire, PCI and CAN. Using ATMEL space packaging expertise, the ATF697 device efficiently combine in a SiP (system in package) the ATF280 and the AT697 LEON2FT processor, allowing a significant footprint reduction for a frequently used combination of devices. The European AT40K radiation-hardened FPGA family offers proven US export regulations free solutions and is mainly used for Scientific and Earth Observation missions.

Networking Coffee Break sponsored by CNES CCT and ESA's Data System Division (10:30 – 11:00)

Session: FPGA Vendors (11:00 – 12:00)
Chair: *Mr FERNANDEZ-LEON, Agustin (ESA)*

11:00	**Common Subsystems Design Requirements for Performance and Reliability in an FPGA** *Presenter: Mr. HU, Ching (Intel Corporation)* The commercialization of LEO in the recent year has inspired many creative ways to reduce cost while increasing performance of the satellite systems. Traditional satellite system designs have more focus on reliability. The new approach is to focus more on short term performance and compensate reliability with cluster of redundant satellites. Through an overview of various common subsystems, this discussion will explore topics to combine the most practical aspect of reliability with high performance. Subsystems to be discussed may include (as time permits): communication links, multi-spectral remote sensing, traffic management, and fundamental building block DSP capabilities.

Session: Fault Tolerance Methodologies and Tools (12:00 – 12:35)
Chair: *Mr. FERNANDEZ-LEON, Agustin (ESA)*

12:00	**The Benefits of Feedback TMR for SEU Tolerance of SRAM FPGA Designs** *Presenter: WIRTHLIN, Mike (Brigham Young University)* Modern SRAM Field Programmable Gate Arrays (FPGAs) provide a large amount of logic,

		computing, and I/O resources that can be programmed in the field through device configuration. FPGAs are also increasingly including a variety of fixed circuits such as programmable processors and high-speed I/O interfaces to facilitate the development of complex, single-chip programmable systems. Like all semiconductor devices, FPGAs are susceptible to ionizing radiation and experience single-event upsets (SEUs) within the logic configuration memory, user block memory, and user flip-flops. To use SRAM FPGAs reliably in space environments, the negative effects of these SEU must be mitigated. Fortunately, the programmable nature of FPGAs can be exploited to provide SEU mitigation. Programmable resources can be reserved for replication of user circuits to mask circuit failures. Triple Modular Redundancy (TMR) is a popular technique for addressing such SEUs by triplicating circuit resources and adding majority voters. Feedback TMR, a form of TMR that involves insertion of voters in all feedback paths, can be used to provide self-synchronization when circuit resources are repaired. To maximize the benefits of TMR, configuration memory scrubbing is used to repair upsets in the configuration memory during system execution. Configuration scrubbing uses the partial reconfiguration to continuously repair unwanted upsets in the configuration memory before the effects of these upsets overwhelm the TMR mitigation approach. The use of both techniques together has been shown to provide significant improvements in circuit reliability over the use of either technique on its own. Feedback TMR and configuration scrubbing have been applied to a variety of circuits on the Xilinx 7 series FPGA and tested for SEU tolerance using both fault injection and radiation testing. This presentation will summarize the improvements in reliability of a soft LEON3 processor and a B13 ITC'99 benchmark. The fault injection results suggest improvements in mean time to failure of 51x for the LEON3 and 105× for the B13 benchmark. The same designs were tested at the Los Alamos Neutron Science Center (LANCE) and demonstrated improvements in mean-fluence to failure of 47x for the LEON3 and 52x for the B13 benchmark.

Session: Design Experiences (12:35 – 13:00)
Chair: *Mr. FERNANDEZ-LEON, Agustin (ESA)*

	12:35	**Resource-Efficient Debugging Core to Evaluate FPGA Designs in On-Board Processors** *Presenter: Mr. RITTNER, Florian (Friedrich-Alexander-Universität Erlangen-Nürnberg)* Modern SRAM-based FPGAs improve on-board processing (OBP) in space applications through dynamic reconfiguration of the firmware. This provides flexibility and adaptability for new communication experiments. An example for such a novel signal processing platform is the *Fraunhofer On-Board Processor* (FOBP), located in the scientific payload part of the *Heinrich Hertz* satellite mission, with two space-grade *Virtex-5QV*. Nevertheless, in-orbit verification (IOV) of new firmware experiments comes with the price of reduced debugging possibilities. While on-ground debugging enables to use different tools and methods to access the FPGA, in-space debugging (ISD) restricts this direct access. To solve this problem, we present an ISD core which acts as an interface inside the FPGA to debug firmware signals by an user on earth. The result is a wireless remote access of the FPGA with the possibility of tracing signals and controlling the firmware. We use a virutal telemetrie/telecommand (vTM/TC) link within the user-band to transmit or receive debugging data. We focus a resource-efficient approach based on a VHDL concept and consider flexibility for adaptions and improvements. The concept contains a trigger unit, a read-in module for user data sampling, a memory block for the data storage and a read-out module to connect the ISD core with the vTM/TC. For the first proof of concept, the implementation is reduced to the TX part (capture debug data of a user logic module). We use a typical setup (8 bit data width, 4096 sampling depth) to verify the functionality of the ISD core. The resource consumption results in less than a half percent flip-flops (FFs), look-up tables (LUTs) and BRAM compared to all usable *Virtex-5QV* resources. If we choose a setup with higher data width or sampling depth, the BRAM consumptions appropriately increases while the increase of FFs and LUTs are negligible. We analyze the essential bits of the ISD core and the mentioned setup uses only 0.1 % essential bits. The presented resource-efficient ISD core is able to improve the IOV of new firmware-experiments in FPGA-based OBPs. A debug-unit on the ground is necessary to depacketize, visualize and analyze the debug data. Furthermore, a combination with an BRAM radiation sensor provides additional information about the space whether and allows a categorization of the debug data.

Networking Luncheon (13:00 – 14:00)

Session: Industrial Experiences (14:00 – 15:15)
Chair: *Mr. POUPAERT, Jelle (ESA)*

	14:00	**Experience gained in Flash-based FPGA for InSight** *Presenter: Mr. HUMBERT, Stephane (Syderal SA)* This presentation will address the advantages and disadvantages of flash-based FPGAs versus antifuse FPGAs, in particular regarding radiation resistance. Using reprogrammable FPGAs provides the ability to perform design update late in the equipment development process, but it also brings several constraints that do not have to be taken into account when using the well-known Microsemi RTAX-S FPGAs. RTAX-S FPGA (anti-fuse) has to be configured (programmed) before being soldered on the board which is the main drawback in case of late bug discovery. Microsemi RT ProASIC3 (reprogrammable flash cells) allows late FPGA functionality modifications without hardware impact since the device can be re-programmed on board. But using reprogrammable FPGAs also brings several constraints related to radiation effects mitigation (no native TMR as for RTAX FPGA) and mitigation structure implementation verification. From FPGA selection trade-off to flight design implementation, the presentation will explain how Syderal managed the mitigation technique selection and implementation for two FPGAs designs.
	14:25	**Spartan 6 Evaluation for Space Application** *Presenter: PIKE, Tim (Airbus DS)* The Spartan 6 from Xilinx is an SRAM based military grade FPGA product offering attractive performance for a low power consumption. This presentation covers an investigation by Airbus DS to evaluate this part for space application. Initial radiation results have shown that the Spartan 6 is latch-up free. These results are presented and complementary tests to complete the radiation analysis discussed. Technology investigations and reliability analysis indicate that the Spartan 6 could satisfy the environmental requirements of more demanding space missions. Finally PCB mounting of this part is less challenging than other high pin count FPGA's: it comes in a moderately sized 676 ball PBGA package and first mounting trials at Airbus DS have proved encouraging. An outlook to perform a formal qualification of this component to ECSS-Q-ST-60-13C concludes this presentation.
	14:50	**High Performance COTS based Computer with FPGA's implementation** *Presenter: Mr. NOTEBAERT, Olivier (Airbus Defence and Space)* Architectural solutions for improving robustness of space computers w.r.t. radiations effects enables the development of high performance computers based on commercial grade digital processing devices such as microprocessors or FPGA's. This can bring a new range of space data processing performance at a reasonable cost. Indeed, several range of space applications require increasing bandwidth in data processing together with the flexibility or reprogrammable devices. However, conventional Rad-hard FPGA's provide limited performance and can only be configured once. Few rad-tolerant devices are now available but the capability to use commercial based FPGA's in space is a strong enabler. The ESA study HiP-CBC (High Performance COTS Based Computer) has validated the radiation mitigation concept with a TRL6 demonstrator. This concept is now applied to several applications, for instance with the Spartan 6 and should be extended in the future to other reprogrammable devices.

Session: FPGAs: High Performance (15:15 – 15:40)
Chair: *Mr. MANNI, Florent (CNES DC/TV/IN)*

	15:15	**High-Performance Scientific Computing on FPGA aboard the Solar Orbiter PHI Instrument** *Presenter: Dr. COBOS CARRASCOSA, Juan Pedro (Institute of Astrophysics of Andalusia)* SO/PHI (Solar Orbiter Polarimetric and Helioseismic Imager) is a filtergraph-based, solar magnetograph aimed at mapping the vector magnetic field and the line-of-sight (LOS) velocity of the solar photospheric plasma. It belongs to the scientific payload of the European Space Agency's Solar Orbiter mission which will orbit the Sun at 0.28 astronomical units. The limited telemetry rate combined with the large amount of scientific information retrieved by the SO/PHI instrument demand a sophisticated on-board data reduction and scientific analysis through the study of the polarization state of a specific spectral line. The main aim is to perform the complicated algorithm needed to translate the polarization state of the light spectrum in terms of some specific solar parameters like the magnetic field vector and velocity. Technically speaking, the inference of the solar physical quantities through a spectropolarimetric study is based on the inversion of the Radiative Transfer Equation (RTE) and these tasks require the

		processing of a huge quantity of data in parallel. The RTE inverter is the core of the on-board scientific data analysis and, probably, one of the most innovative parts of the instrument. Due to the unavailability of qualified for space processors, DSPs, or GPGPUs that fulfil the stringent computational requirements with the limited room and power consumption allocated to the instrument, a specifically designed hardware device has been implemented in SO/PHI. This device is in charge of inverting the RTE aboard Solar Orbiter under narrow time and power constraints. The main aim of this work is to design, build, and test such a hardware device for SO/PHI. With that goal in mind, we propose a high-performance computing architecture for carrying out the RTE inversion using FPGA devices embedded in the SO/PHI instrument. The computing proposal consists of a SIMD multiprocessor architecture to reach high performance in floating point operations. This architecture on a Virtex-4 FPGA squeezes the FPGA resources in order to reach the time constraints. It is focused in exploiting the data parallelism using several processors working together and using different data streams. One of the most important contributions of this architecture is the ability of saving resources allocating operation cores in a shared operation block, which is accessed by every processor. Some details for extending the architecture to other problems are pointed out. Using the SIMD architecture, the challenge of carrying out the RTE inversion in less than 15 minutes has been reached. The architecture has not only demonstrated that is able to do it but it is also improves the computing capabilities of ground systems by more than ten times using a relatively slow (and 10 year-old) Virtex-4 FPGA device. The RTE inverter prototype has been tested using real images taken by another instrument. It is able of working as accurately as usual computers regarding the scientific precision. In addition, it has satisfied the stringent requirements of power consumption and processing time.

Networking Coffee Break sponsored by CNES CCT and ESA's Data System Division (15:40 – 16:10)

Session: FPGAs: High Performance (16:10 – 16:35)
Chair: *Mr. MANNI, Florent (CNES DC/TV/IN)*

	16:10	**High Performance CCSDS Image Compression Implementations on Space-Grade SRAM FPGAs** *Presenter: Dr. KRANITIS, Nektarios (Dept. of Informatics & Telecommunications, National and Kapodistrian University of Athens)* The huge volume of remote sensing data generated from today's and future high resolution, high-speed, imagers and the limited spacecraft data storage resources and downlink bandwidth make on-board image compression one of the most challenging on-board payload data processing tasks. Over the last few years, the Consultative Committee for Space Data Systems (CCSDS) issued two image compression standards: a) the CCSDS-122.0-B-1 Image Data Compression (IDC) standard for lossless and lossy (rate-limited and quality-limited) compression of monoband images and b) the CCSDS 123.0-B-1 Lossless Multispectral & Hyperspectral Image Compression standard for lossless compression of Multispectral and Hyperspectral images. These two CCSDS algorithms were developed specifically for use on-board a space platform, addressing challenges related to memory and computational resources requirements achieving an excellent trade-off between compression effectiveness and computational complexity. Currently, CCSDS is working towards the definition of lossy multispectral and hyperspectral compression algorithms either by defining a spectral transform preprocessing stage followed by application of the image compressor defined in CCSDS-122.0-B-1 or extending CCSDS 123.0-B-1 by defining a quantization feedback loop and associated output data structures to provide low-complexity near-lossless compression. The current state-of-the-art SRAM-based FGPA technology offers radiation hardening by design (RHBD), high density and dynamic partial reconfiguration for in-flight adaptability and Time-Space Partitioning (TSP) of on-board data processing. Such FPGA technology offers unique advantages over both OTP FPGAs and ASICs and can be considered as an excellent platform for implementation of on-board payload data processing due to its ability to support upgrades after launch, greatly enhancing mission profile and extending valuable system life time. In this presentation, we will present two state-of-the-art throughput performance implementations of both CCSDS image compression standards targeting the Xilinx Virtex-5QV space-grade SRAM FPGA. The CCSDS-IDC implementation as an IP core is a highly integrated, single FPGA solution providing state-of-the-art throughput performance (128 MSamples/s) and has the following features: a) it does not require any external memory for data buffering; b) it provides high rate-distortion performance for lossy mode supporting large values of segment size (S=128); c) it

		supports selective image compression by leveraging segmentation features of CCSDS-IDC in order to enable a non-uniform distribution of the available bit budget (i.e. image quality) between a selected region-of-interest (ROI) and the rest of the image, without any modifications on the standard and without any computational performance overhead. The presented CCSDS 122.0-B-1 implementation as an IP core achieves significant throughput performance improvement (128MSamples/s) with respect to the current state-of-the-art (78MSamples/s) and requires about 60% of slices and 67% of BRAMs of the Virtex-5QV FPGA resources. The CCSDS 123.0-B-1 implementation as an IP core over doubles the throughput performance (100MSamples/s) with respect to the current state-of-the-art (40MSamples/s) and has the following features: a) it supports Band-Interleaved Pixels (BIP) ordering, b) it interfaces with an external DRAM memory controller for data buffering; c) it requires less than 22% of slices and 10% of BRAM of the Virtex-5QV FPGA resources. To the best of our knowledge, both implementations are the fastest space-grade SRAM FPGA implementations of CCSDS image compression algorithms to date.

Session: Fault Tolerance Methodologies and Tools (16:35 – 17:25)
Chair: *Mr. MANNI, Florent (CNES DC/TV/IN)*

	16:35	**OLT(RE)^2: A Tool Flow for Mitigation of Permanent Faults in Reconfigurable Systems** *Presenters: Mr. COZZI, Dario (Univesity of Bielefeld), Mr. KORF, Sebastian (Bielefeld University)* Reconfigurable systems are more and more employed in many application fields, including aerospace. SRAM-based FPGAs represent an extremely interesting hardware platform for this kind of systems, because they offer flexibility as well as processing power. Furthermore, the ability of run time reconfiguration of SRAM-based FPGAs can provide advantages for many applications. The scope of this project is to develop a software flow, named **OLT(RE)²** (**O**n-**L**ine **T**esting and Healing Permanent **R**adiation **Effects** in **Re**configurable Systems), for testing and diagnosing permanent faults in SRAM-based FPGAs during the life-time of a space mission. Once faults in the FPGA-fabric have been detected and located, the flow should enable patching the discovered faulty resources, allowing faulty regions of the FPGA to be available for further use during the space mission. The OLT(RE)^2 flow enables to prove that the routing resources of an FPGA are free of stuck-at-1 and stuck-at-0 permanent faults (e.g., caused by TID). It is important to verify that the routing resources of the FPGA fabric are free of permanent faults, since they may cause stuck-at-0, stuck-at-1, bridge, conflicts or antenna effects in a specific design. OLT(RE)^2 relies on dedicated testing circuits handled by an integrated, custom place and route tool. Currently, these testing circuits allow testing slice associated routing resources. Results regarding the fault coverage of the created testing circuits are presented for different FPGA families (Xilinx Virtex-4, Virtex-5, Virtex-6 and Spartan-6). The effectiveness of OLT(RE)^2 is proved on the DRPM (Dynamically Reconfigurable Processing Module) demonstrator, which allows validating the concept in a space application scenario. Stuck-at-1 and stuck-at-0 permanent faults are emulated on the DRPM in order to prove the fault detection capability of the tool. The hardware tests are performed on a Xilinx Virtex-4 FX100 FPGA of the DRPM, e.g., one clock region with 111,179 testable wires is diagnosed for permanent faults in around 26 seconds.
	17:00	**Using Dynamic Circuit Specialisation to Enable Microreconfigurations for Space Applications** *Presenter: Mr. KULKARNI, Amit (Ghent University)* Dynamic Circuit Specialisation (DCS) allows an FPGA design to be dynamically specialized for a subset of its infrequently changing inputs (parameters). Instead of implementing these parameter inputs as regular inputs, in the DCS approach these inputs are implemented as constants and the design is optimized for these constants. When the parameter values change, the design is re-optimized for the new constant values by reconfiguring the FPGA. This is done via micro-reconfiguration where we replace stale bits with specialized bits. The configuration for the parameterized design is generated off-line through an adapted FPGA tool flow. In the adapted tool flow, the bitstreams (entries of the truth tables) are expressed as the Boolean functions of the parameter inputs. At the run-time, for every infrequent change in parameter value, these Boolean functions are evaluated for a specific parameter value to generate specialized bitstreams. In this demo we will show, how we can use DCS to reconfigure FPGAs in space applications. With DCS we create an intermediate generic bitstream that can be later evaluated to its specialized version, for the given parameters. However, this generic bitstream results to functionally equivalent specialized configuration resulting from the evaluation of a boolean

		function. Thus, there is no need of qualifications of the new design. Moreover, we can therefore transmit when needed only the trigger for the evaluation of the Boolean function and not the entire bitstream, making the reconfiguration faster and the transmission safer.

Wrap up and Open discussion (17:25 - 17:55)
Presenter: Mr. DANGLA, David (CNES); Mr. MERODIO CODINACHS, David (ESA)

SEFUW Dinner (20:00 – 22:30)
3 Course Menu and drink arrangement at “Iets Anders in Bistro Bardot"
(Pickeplein 4 - 2202 CK Noordwijk)

Thursday 17 March 2016

SEFUW Intro – Opening Remarks (08:50 - 09:00)
Presenter: Mr. DANGLA, David (CNES); Mr. MERODIO CODINACHS, David (ESA)

Session: FPGA Vendors (09:00 – 11:30)
Chair: *Mr. DANGLA, David (CNES)*

09:00	**NanoXplore NXT-32000 FPGA** *Presenter: Mr. LEPAPE, Olivier (NanoXplore)* NanoXplore will introduce the first member of its Radiation Tolerant NXT FPGA family. This device is the first SRAM based FPGA based on NanoXplore scalable patented architecture and entirely hardened by design in order to mitigate SEL, SEU and SEFI in the user application as well as in the configuration initialization and integrity. The combination of advanced hardening by design techniques with architectural features implemented in the configuration management lead to outstanding radiation robustness in line with space missions requirements. The first part of the presentation will cover the FPGA hardware in term of user functionalities and characteristics (combinatorial logic, registers, memories, DSP functions, clock generation, clock distribution, I/O capabilities), radiation mitigation features (hard protections, soft protections), and configuration integrity mechanisms (bit stream download, bit stream integrity check, configuration check). Then the second part will focus on the mapping software providing a full chain from RTL description to bit stream generation. By adopting dedicated algorithms developed specifically for NXT FPGA architecture, this software provides best in class mapping performances as well as very short execution times.
10:00	**Xilinx Virtex-5QV Update and Space Roadmap** *Presenter: Mr. HUEY, Kangsen (Xilinx, Inc.)* Xilinx Space grade Field Programmable Gate Array (FPGA) has been utilized by the space community for over 15 years for payload applications requiring extensive amount of FPGA resources. The most current generation space grade FPGA is Virtex-5QV, which was introduced in 2011 which is well received by customers globally and has started to accumulate space flight heritage. This presentation will provide a quick status update on Virtex-5QV, then move on to the main topic to introduce Xilinx Space Roadmap, which will outline the next generation space grade FPGA from Xilinx. Many current and future requirements for space payload applications are demanding vast amounts of processing resources like logic cells, DSPs, SRAMs, and SERDES for digital data processing and image compressions, etc.; plus the in-orbit reconfigure-ability has now become essential to enable multi-use hardware for true reduction of SWaP (size, weight and power). These new requirements far exceeds the capability of Virtex-5QV and similar level devices, and can only be achieved with Xilinx next generation space grade FPGA. This presentation will provide an overview of the features and performance of Xilinx next generation space grade FPGA, initial radiation data, packaging plan, schedule for software, prototyping and space flight parts.

Networking Coffee Break sponsored by CNES CCT and ESA's Data System Division (11:30 – 11:45)

Session: Radiation (11:45 – 12:10)
Chair: *Mr. POIVEY, Christian (ESA)*

11:45	**Heavy-Ion Micro Beam Study of Flash-Based FPGA Microcontroller Implementation** *Presenter: Mr. EVANS, Adrian (IROC Technologies)* Flash-based FPGAs such as the ProASCI3L family are frequently used in space applications because the flash storage is highly resistant to single-event effects (SEEs). In this presentation we show the results of a study of an ARM® Cortex-M0+® processor core running a benchmark application (Dhrystone) and tested under a heavy-ion micro-beam. Over a million individual ions were fired both at a plain and a sequential TMR version of the processor. Using special control circuitry, the physical location and exact time of each ion strike was localized and the effect on the test application was studied. We show the reduction in silent data corruption (SDC) and detected-uncorrected errors (DUE) that was achieved in the SEU mitigated (sTMR) processor. It is also shown, using both test-results and fault injection simulations, that single event transients (SETs) are responsible for a significant fraction of the failing cases. The use of the mirco-beam

		allows designers to identify the specific weak, sensitive areas in their designs with fine granularity.

Session: FPGAs: High Performance (12:10 – 13:00)
Chair: *Mr. MERODIO CODINACHS, David (ESA)*

	12:10	**FPGA acceleration in GMV projects for Space Vision-based GNC systems** *Presenter: Mr. GONZALEZ-ARJONA, David (GMV Aerospace and Defence)* Vision Based GNC is becoming the focus of interest for future missions since it will allow mission objectives which cannot be performed by ground because of delays or because the dynamic is too fast for being controlled remotely. On the other hand, the use of information extracted from image in the GNC loop is a challenging issue because images are composed by large amount of data, and, extracting information to be used in the GNC requires complex algorithms that have to be executed at determined frequencies. GMV is applying FPGA acceleration to autonomous GNC system for solving this problem in descent and landing (DL) scenarios under several ESA contracts. The GNC systems are vision-based navigation relying on advanced algorithms and European navigation sensors. The image processing and navigation algorithms developed have been optimized for different scenarios: Itokawa asteroid (Marco Polo-R), Phobos (Phootprint), Dydimos (AIM), the Moon (Lunar Lander and related activities). The GNC systems, where GMV is involved, can use three different vision-based navigation strategies, pure relative navigation, enhanced relative navigation and absolute navigation. They have been implemented in flight representative hardware in a tight and optimal implementation with HW/SW co-design methodology onto a Xilinx XC4V FPGA plus processor device system. As example, within NEOGNC2 project, GR-RASTA-101 avionics has been used for the breadboard prototype, based on Leon2 processor ASIC and XC4VLX100 GR-IO reprogrammed FPGA. The system has been tested in real time testbench available at GMV with simulated images. In addition, HIL tests with a mock-up of Phobos surface and a real camera have validated the performances of the core of the system in a representative environment. In other activities, CPCI-CPU-750 is used as representative HW for hosting complex SW algorithms. Furthermore, within a project of an ECSEL call, GMV participates in the demonstration of in-flight reconfigurable FPGA which uses different vision-based navigation techniques during different mission phases. In this section, the different concepts are presented especially pointing out to the challenges of HW/SW co-design implementation, validation and verification techniques implied in these complex designs.
	12:35	**FPGA acceleration of computer vision and optimization for European space applications** *Presenter: Dr. LENTARIS, George (National Technical University of Athens, Greece)* Future space robots will rely heavily on computer vision to achieve a high degree of autonomy and efficiency during their mission. Specifically for the Mars rovers of 2020+, ESA plans on using highly accurate localization and mapping algorithms with significantly increased speed. The goal is to provide the rover with the capability to process a mid-resolution stereo image pair in only 1 second, as well as to export a high-definition wide field-of-view depth map in less than 20 seconds. Given the low processing power of the space-grade CPUs, the means to achieve this high-performance goal is to employ high-density space-grade FPGAs and accelerate the computationally demanding kernels of the algorithms by a factor of 10x-1000x. In the project COMPASS of ESA (Code Optimization and Modification for Partitioning of Algorithms developed in SPARTAN/SEXTANT), we perform HW/SW co-design, multi-FPGA partitioning and optimization/customization of various computer vision algorithms for the future Mars rovers. We consider the most prominent of the HW/SW pipelines developed in the past projects SPARTAN and SEXTANT and we re-implement them on space representative hardware focusing on available European devices. To this end, we make use of a LEON3 CPU and, additionally, we take into account the specifications of the new BRAVE NG-FPGA developed for ESA. More specifically, on SW, we use RTEMS on LEON3 and we project the timing results to 150 MIPS. On HW, we use the Synopsys HAPS-54 multi-FPGA board and we impose constraints on the resource utilization of each FPGA to emulate the BRAVE devices. During the optimization phase of COMPASS, we decreased the SW execution time of the algorithm by 90%, whereas for the HW parts, we decreased the FPGA resources by 25%-51% compared to SEXTANT. As a result, today, the complete system (the FPGA parts of both localization & mapping pipelines) will fit in a single space-grade Xilinx FPGA, i.e., the Virtex-5QV. The proposed system can perform 3D terrain mapping in only 17.4sec generating a limited error of 2cm at 4m depth (achieved system speedup 796x), as well as rover localization with less than 2% positional error while running at 1-2 frames per second (achieved system speedup 34-56x). Furthermore, in the multi-FPGA partitioning phase of COMPASS, we demonstrated that it is possible to fit the proposed algorithms in the European space-grade NG-FPGA by

		employing 1, 2, or 3 BRAVE devices of distinct size each; depending on the specifics of the hypothetical mission (device availability, reconfigurability, and algorithmic performance), we proposed and tested 3 fully-functional multi-FPGA designs, which proved the concept of using European FPGA technology to advance the space applications of the near future.

Networking Luncheon (13:00 – 14:00)

Session: Reconfigurability (14:00 – 14:25)
Chair: *Mr. MERODIO CODINACHS, David (ESA)*

	14:00	**Fast In-Orbit FPGA Reconfiguration via In-Band TM/TC** *Presenter: Mr. STENDER, Christopher (Fraunhofer Institute for Integrated Circuits IIS)* Flexible payloads often contain one or more reconfigurable FPGAs. In order to use them for various tasks or to quickly deploy new algorithms, a fast FPGA reconfiguration is essential. Unfortunately, satellite telemetry and telecommand (TM/TC) links usually provide only slow data rates for configuration uploads or might not even be available for the payload operator at any time. Thus the upload of a new design, with a size of several megabytes, makes up the largest part of the reconfiguration time. We present a robust in-band "virtual" TM/TC communication system that enables the upload and configuration of new FPGA designs within minutes or even seconds. Cutting dependencies to the satellite's flight computer or payload controller further simplifies the development and increases the flexibility of the payload. The two lower link layers and parts of the configuration logic are implemented in VHDL. The upper link layers and the management of multiple configurations are realized in software running on a *LEON3FT* soft IP microprocessor. Since the entire digital communication system is implemented in a *Xilinx Virtex-5QV* FPGA, no additional computing hardware is required. To increase the reliability, multiple instances of the virtual TM/TC can be instantiated in the same or other FPGAs. The virtual TM/TC communication system is going to be used for the *Fraunhofer* On-Board Processor (FOBP). Assuming a 1 Mbit/s uplink, a 6 Mbyte *Virtex-5QV* configuration file can be reliable uploaded and configured in less than a minute.

Session: Radiation (14:25 – 15:15)
Chair: *Mr. POIVEY, Christian (ESA)*

	14:25	**Single Event Effect Test on 28nm FPGA** *Presenter: Dr. GARCIA, Pierre (TRAD)* The focus of our study is to evaluate the impact of single event effect on Kintex-7 SRAM based FPGA. The 28nm Kintex-7 family is optimized for best price-performance with 2X improvement compared to previous generation. One of the few major disadvantages of SRAM-based FPGAs is their sensitivity to ionizing radiation. A change in configuration memory due to radiation can modify the implemented circuit, possibly leading to Single Event Functional Interruptions, SEFI for example. Moreover, the improvement of the technological node, such as in kintex-7, can lead to the increase of the sensitivity to ionizing particles. Two different approaches will be used in order to estimate the SEE sensitivity of the device, one design composed by shift register chain, and a second complex design dedicated to represent a typical space application. The aim of the first test vehicle being to characterize the different elements of the FPGA, it is proposed to test in the same time during irradiation under heavy ion beam, a group of chains and a block memory of 36 Kbits. The second design will be an actual space application. This test vehicle must present an interest for spacecraft payload or platform. However the diagnostic of the failures linked to soft errors must be easy to interpret. On the other hand it also must present a sufficient complexity to necessitate a Kintex-7 FPGA. During the presentation, this two vehicle designs and the test bench will be described and explained. Details of the kintex-7 implementation for SEE testing will also be discussed.
	14:50	**An overview of FPGA use in the LHC accelerator and the CERN experiments** *Presenter: Mr. DANZECA, Salvatore (CERN - European Laboratory for Nuclear Research)* The particle accelerators and high energy physics (HEP) experiments require advanced instruments using the latest technology. The complex and new applications require custom instrumentation and need constant research and development of new electronics. To address the need of customization and high processing capability the Field Programmable Gate Arrays (FPGA) are a very popular choice in both the Large Hadron Collider (LHC) accelerator and HEP experiments. The advantage of using FPGA is in their versatility,

		programmability, high bandwidth communication interfaces and signal processing capabilities. FPGAs are key elements for several equipment in the LHC accelerator with different degrees of criticality. In the accelerator the most exposed equipment, such as the cryogenic, power converter and beam instrumentation widely use FPGAs. For the HEP experiments, the FPGA starts to become attractive in environments with low/medium radiation and where power/integration issues are less critical. Being one of the showstoppers, the radiation levels in the LHC accelerator and in the experiments are presented. The custom application requirements for the accelerator and the experiments are discussed with a focus on the lifetime and tolerable error rates. Some typical applications will be presented in order to give an overview of the use of the FPGA in the HEP sector.

Session: Fault Tolerance Methodologies and Tools (15:15 – 16:05)
Chair: *Mr. MERODIO CODINACHS, David (ESA)*

	15:15	**Enhancing the Reliability of COTS SRAM-based FPGAs with Microreconfiguration for SEU Mitigation in Space Applications** *Presenter: Ms. KOURFALI, Alexandra (Ghent University / ESA)* SRAM-based logic devices such as FPGAs are susceptible to SEUs and functional interruptions in harsh radiation environments, such as space. Several mitigation techniques have been used in order to sustain the functionality of the design, after SEUs are detected and corrected. However, the majority of these mitigation techniques (e.g. TMR) introduce area overhead in the original design. We propose a methodology that adds an extra layer of reliability to Commercial off-the-shelf (COTS) FPGAs that will allow them to be used safely in space missions. This technique can add an integrated online testing infrastructure in the design, in order to provide extra protection. This infrastructure can detect and correct efficiently possible SEUs occurring in the FPGA's logic during operating time, by using microreconfiguration. With microreconfiguration the design is dynamically specialised for a subset of its current signals that are susceptible to a SEU. Microreconfigurations are normal FPGA-configurations where some of the bit-values are replaced by Boolean functions of certain signals. An actual FPGA configuration is generated from the microreconfiguration by evaluating these signals. During operating time, when a SEU occurs, the correct bit-values are found by evaluating the boolean functions of the microreconfiguration. These new bit-values can then be loaded into the FPGA configuration memory using partial run-time reconfiguration. This technique can reduce the area overhead after adding the extra functionality for the SEU mitigation technique, as a subset of the signals are replaced by boolean functions, resulting at a new specialised design that is smaller, and in some cases faster, than the original.
	15:40	**Highly Reliable System-on-Chip using Dynamically Reconfigurable FPGAs** *Presenter: Prof. STERPONE, Luca (Politecnico di Torino)* Radiation-induced Soft Errors are widely known since the advent of dynamic RAM chips. Reconfigurable FPGA devices based on SRAM configuration memories are extremely sensitive to these effects resulting in an unwelcome change of behavior in digital logic. Indeed, soft errors occur today as a result of radiation from space or even at sea level. Detection, protection and mitigation of soft errors beyond aerospace and defence applications have been widely debated over the last decades. In the present paper we provide a complete design flow illustrating the proper design rules ranging from the synthesis, mapping and physical place and route algorithm tailored to the implementation of high performance and reliable SoCs using dynamic-reconfiguration oriented SRAM-based FPGAs. Radiation experimental results obtained radiation test performed using proton particles demonstrated the goodness of our developed design flow resulting in an overall error cross-section reduction of more than 2 orders of magnitude.

Concluding remarks and closure (16:05 - 16:30)
Presenter: Mr. DANGLA, David (CNES); Mr. MERODIO CODINACHS, David (ESA)

SOCIAL DINNER – SEFUW 2016

A non-hosted dinner will take place on Wednesday night (March 16th) at
"Iets Anders in Bistro Bardot" at 8pm

Price: 43 EUR
The price includes a 3 course menu and drink arrangement.
The restaurant is situated in **Pickeplein 4 -2202 CK Noordwijk**.

MENU

Carpaccio with grated Parmesan, marinated tomatoes and rocket dressing
or
Goat cheese salad with sweet vinaigrette
or
Home-made creamy poultry soup

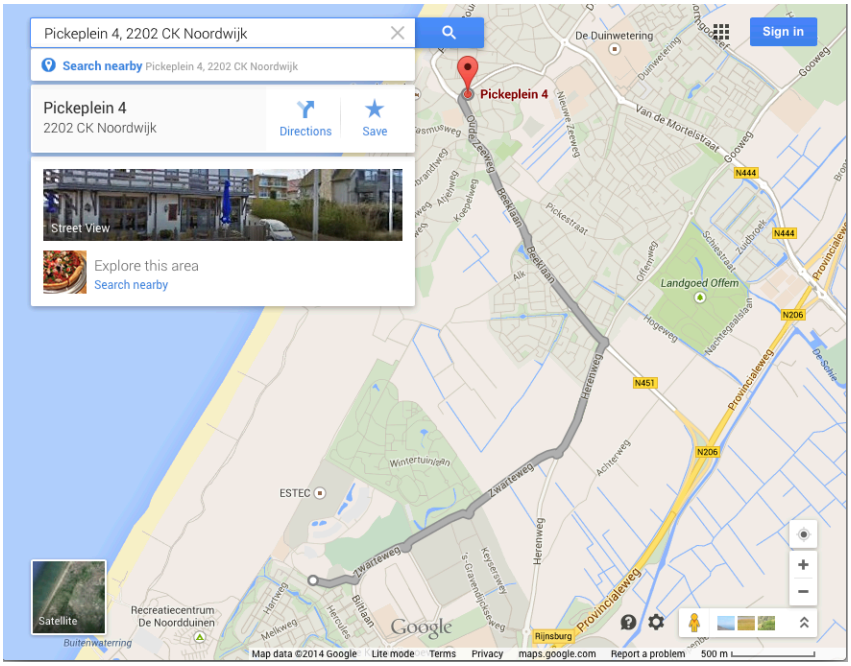
* *

Grilled salmon steak with remoulade sauce
or
Vegetarian lasagna filled with vegetables, tomatoes and crème fraîche
or
Beef entrecote with home-made BBQ sauce

All mains are presented with organic vegetables and pasta or potato garnish

* *

Crêpes Suzette, with orange sauce, Grand Marnier and vanilla ice cream
or
Selection of French cheeses



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