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High Performance COTS based computer FPGA implementation

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High Performance COTS based computer FPGA implementation

- High Performance Processing needs
- The High Performance COTS Based Computer Study (HiP-CBC)
- Hi-P CBC FPGA implementation

High Performance Processing Needs

High Performance Payload Processing Needs

- **Payload / Instruments data processing**
  - Data-flow architecture
  - High data rate front-end interface for raw data filtering and digitalization
  - Mission dependant on-board data processing
  - Data buffering in fast local memory
  - Control loops / latency requirements (in few cases)
  - Data storage in high capacity mass memory
  - Processing performance / power consumption
- **Industrial efficiency requires Lower cost, Modularity, Flexibility…**

Reprogrammable Devices
FPGAs and micro-processors
(DSP's, multi-cores, many cores,…)

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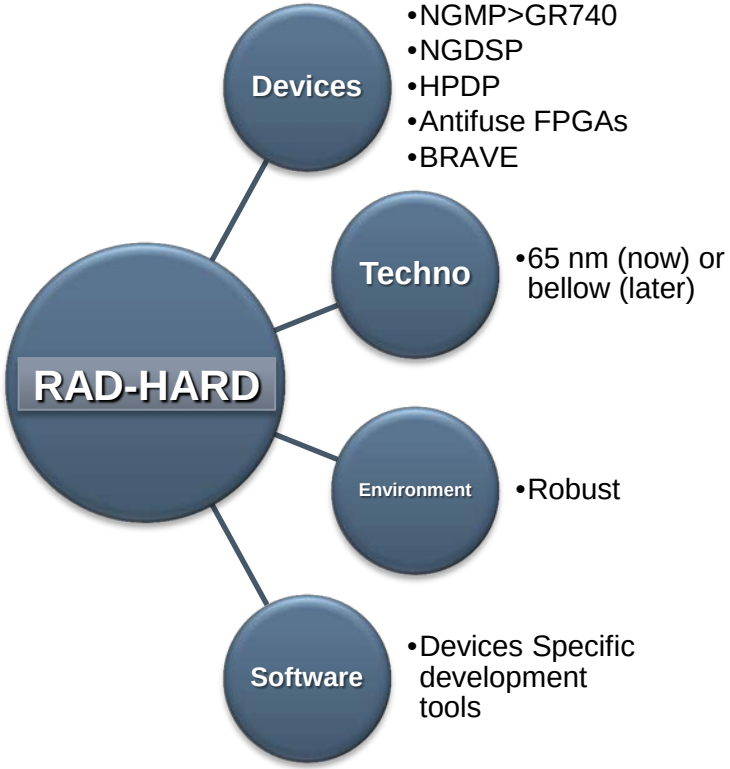
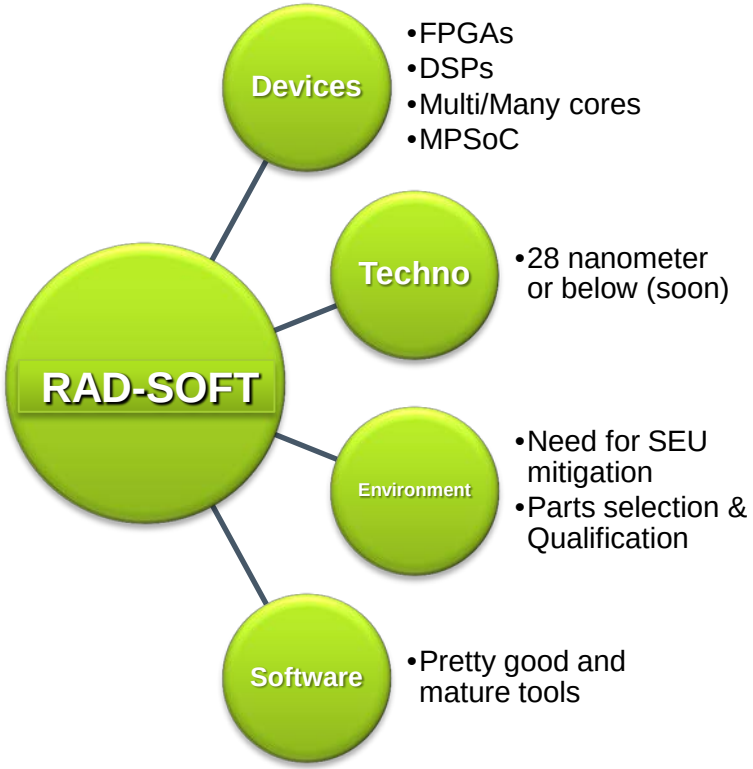
High Performance Reprogrammable devices

Multi and many cores µ-processors / reconfigurable FPGA's





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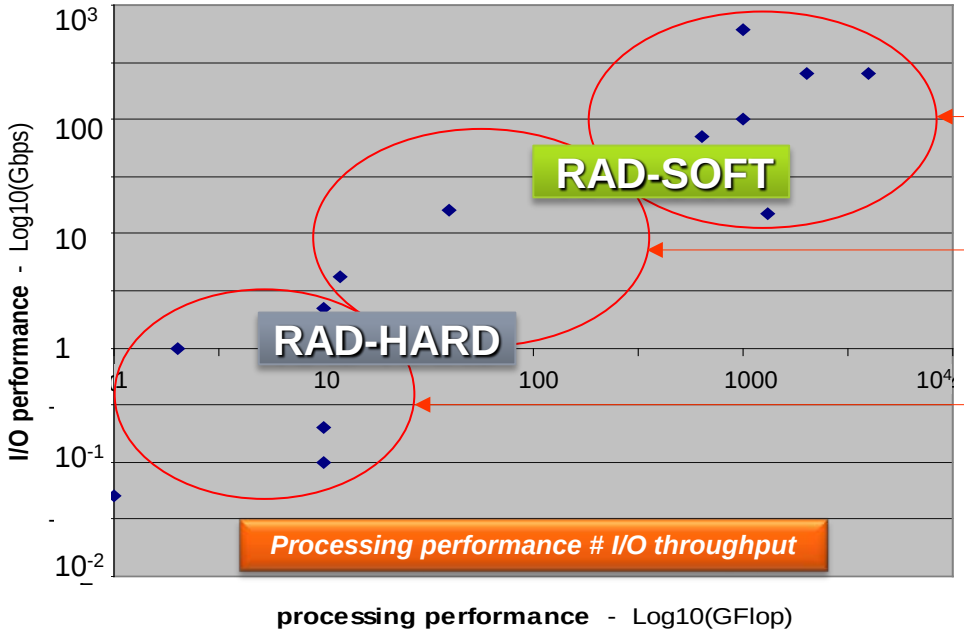
High Performance Processing classes



Processing Performance classes

High > 100 GFlop
High-end COTS FPGAs

Medium [10 – 100] GFlop
High end many core CPU's or FPGAs

Low 0.5 - 10 GFlop
multi – many cores µP/DSP's

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Commercial µProcessors and FPGA's

- **Dynamic roadmap with attractive products**
  - µProcessors: DSP6727, PPCs, ARM, ATOM…
  - FPGA's: Virtex, ProASIC
  - MPSoC: Zynq
- **Manageable radiations issues**
  - Destructive effects
    - Latch-up free – or can be mitigated
    - Total dose acceptable for many LEO missions
    - Some products with "rad-hard" characteristics
  - Non permanent effects require mitigation

RAD-SOFT components
May be used for a wide range of missions
(not for all)

The High Performance COTS Based Computer Study (HiP-CBC)

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High Performance COTS Based Computer (HiP-CBC)

- **Robust architecture for COTS based processing**
  - Use existing COTS devices (DSP, FPGA's)
  - Mitigate radiation effects from a robust and programmable external device (SmartIO)
  - Applications to payload data processing
- **Study priorities**
  - Mission scalability
  - Independence of the mitigation mechanism w.r.t. processing device
  - High data bandwidth standard interfaces
  - Suitable for different types of missions
  - TRL 5-6 demonstrator
    - Mature technology
    - DSP as COTS processor

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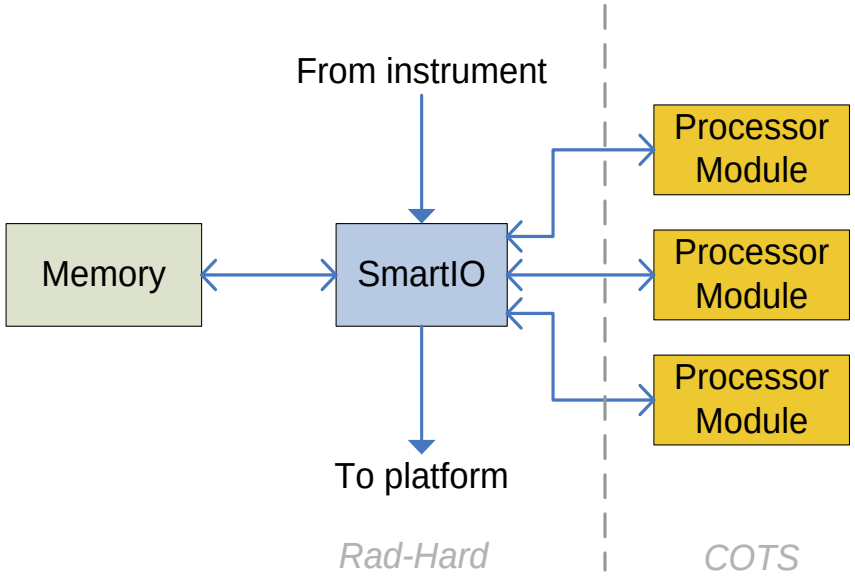
High Performance COTS Based Computer (HiP-CBC)

Concept

- **SmartIO**
  - Rad hard component
    - in charge of the isolation between the COTS world and the “rad hard” world.
  - Controls several COTS components
  - Provides scalable fault mitigation functions
  - Buffers instrument data in a fast local memory, and replays it in case of error
- **Several Processor Modules**
  - Implemented with µProcessor or FPGA



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Benefits

- SmartIO / PM link is a standard HSSL
  - LVDS, SpW, SpFi, SRIO, PCIe_serial, GbitEthernet
    → flexibility, technology independence
- PM’s are slaves of the SmartIO
  - simplicity of the fault model
- SmartIO in HW+SW to manage fault mitigation
  → versatility
- Batch processing and results checks with signature
  → performance
- Scalable Architecture
  → adaptable to mission requirements

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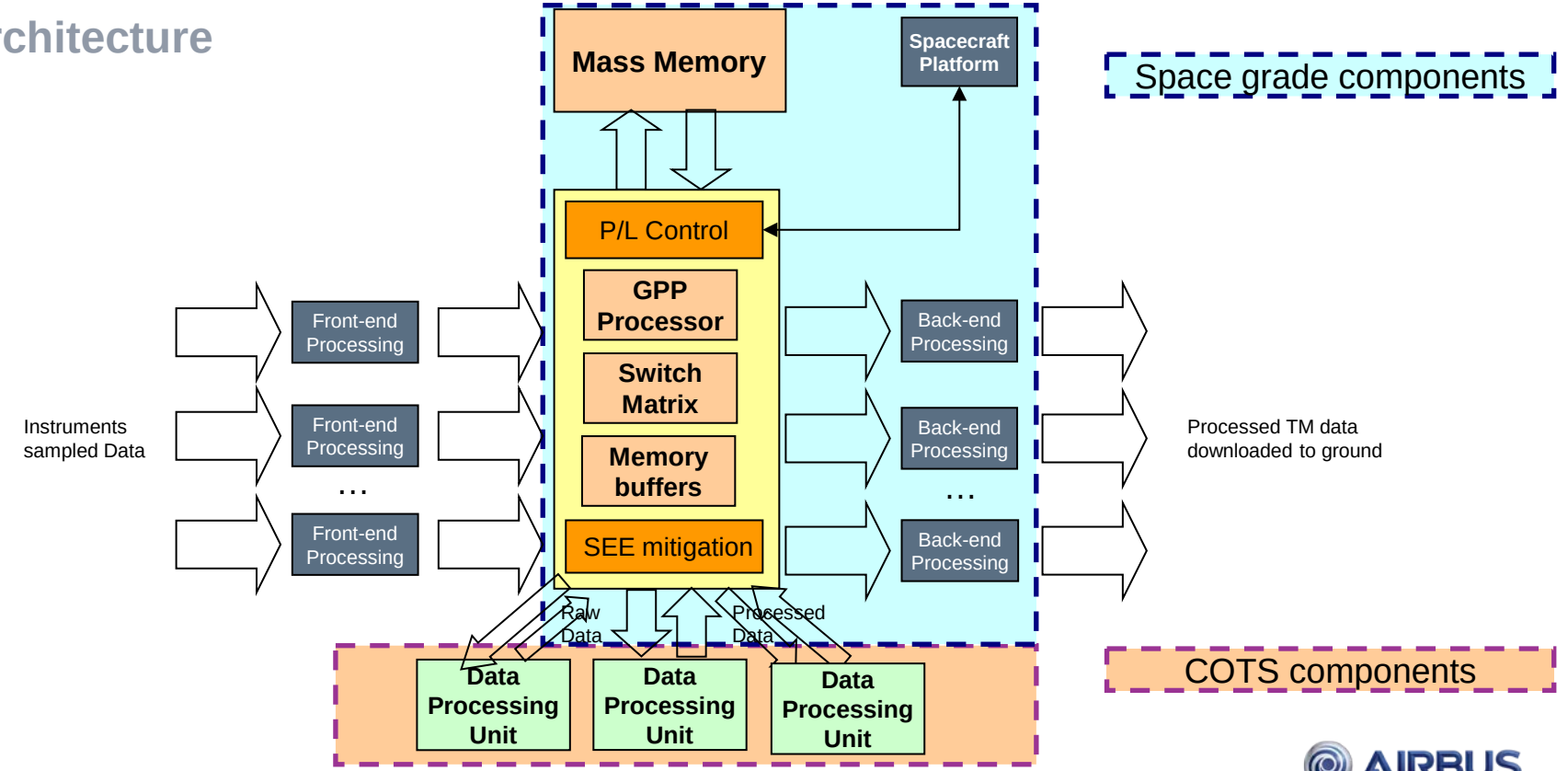
High Performance COTS Based Computer (HiP-CBC)

Architecture



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High Performance COTS Based Computer (HiP-CBC)

Demonstrator

- SmartIO with SCoC3 (Leon3) for control, monitoring and reconfiguration
- DSP board developed by OHB_{CGS} in Milano with a DSP 6727 from TI
- Demonstration Software on Smart I/O and Processing Module S/W
- Performance and availability model

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Hi-P CBC FPGA implementation

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FPGA Technologies

Feature	Antifuse	Flash	SRAM
Reprogrammable	No	Yes but limited (hundreds of times)	Yes
Volatile Configuration	No	No	Yes
Online reconfiguration	No	Not Recommended	Yes
Capacity	Low	Medium	Very High
DSP Performance	Low (125 MHz)	Medium (350 MHz)	Very High (700 MHz)
Soft Error Sensitivity (SEFI, SEU, SET)	Low to Very Low	Medium to Low (configuration memory immune)	High
TID Tolerance	High	Low to medium	High

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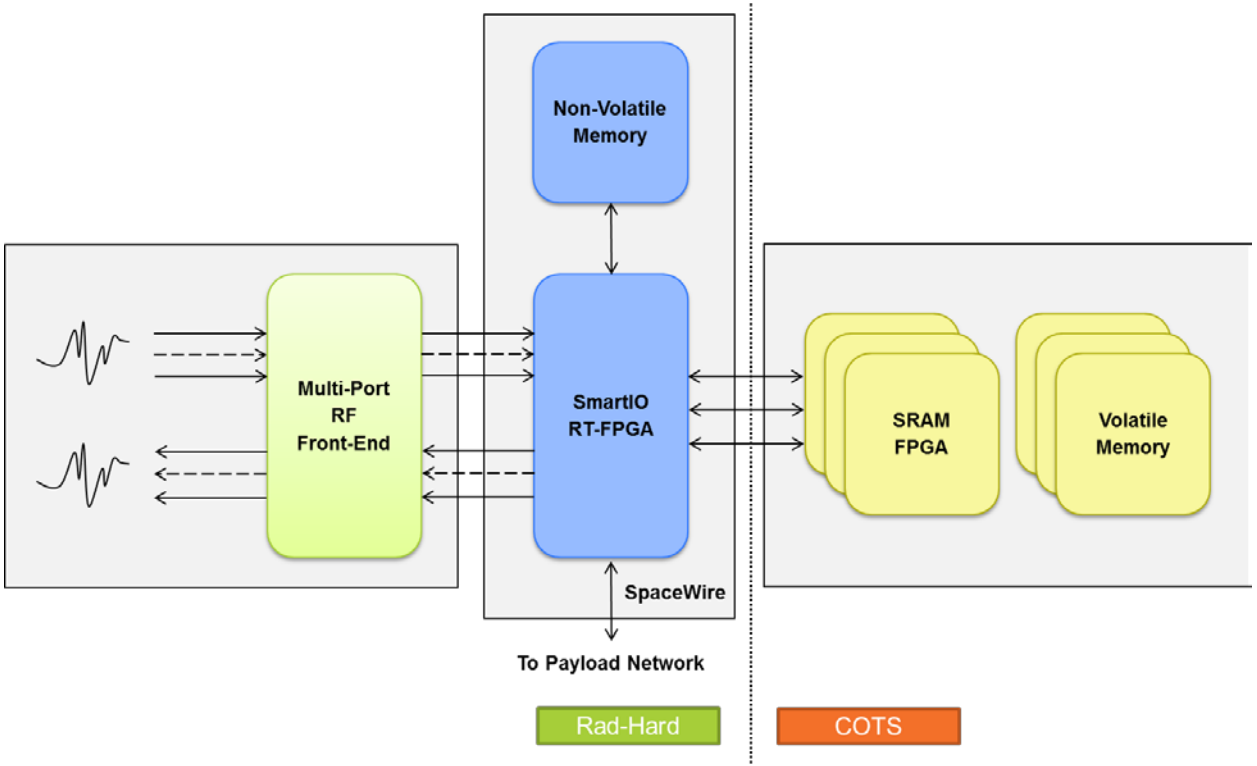
Application to SDR Payloads



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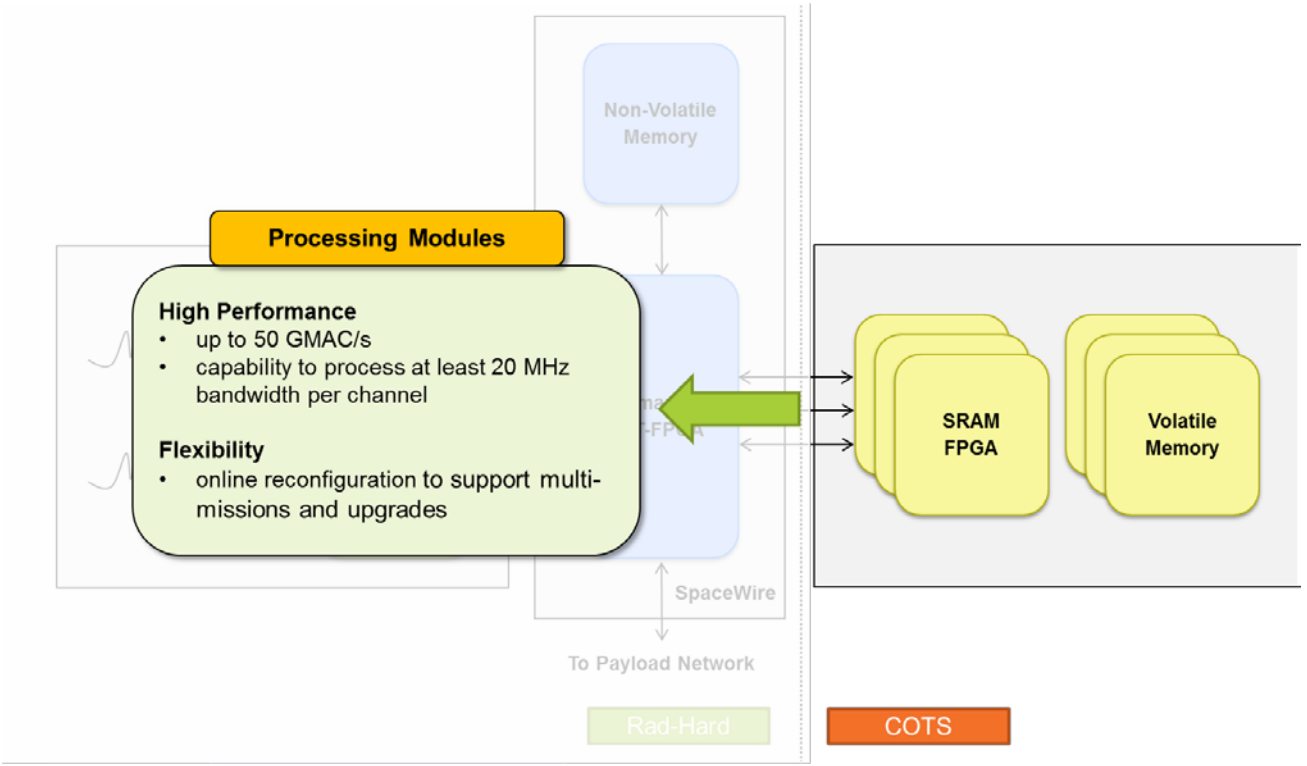
Application to SDR Payloads



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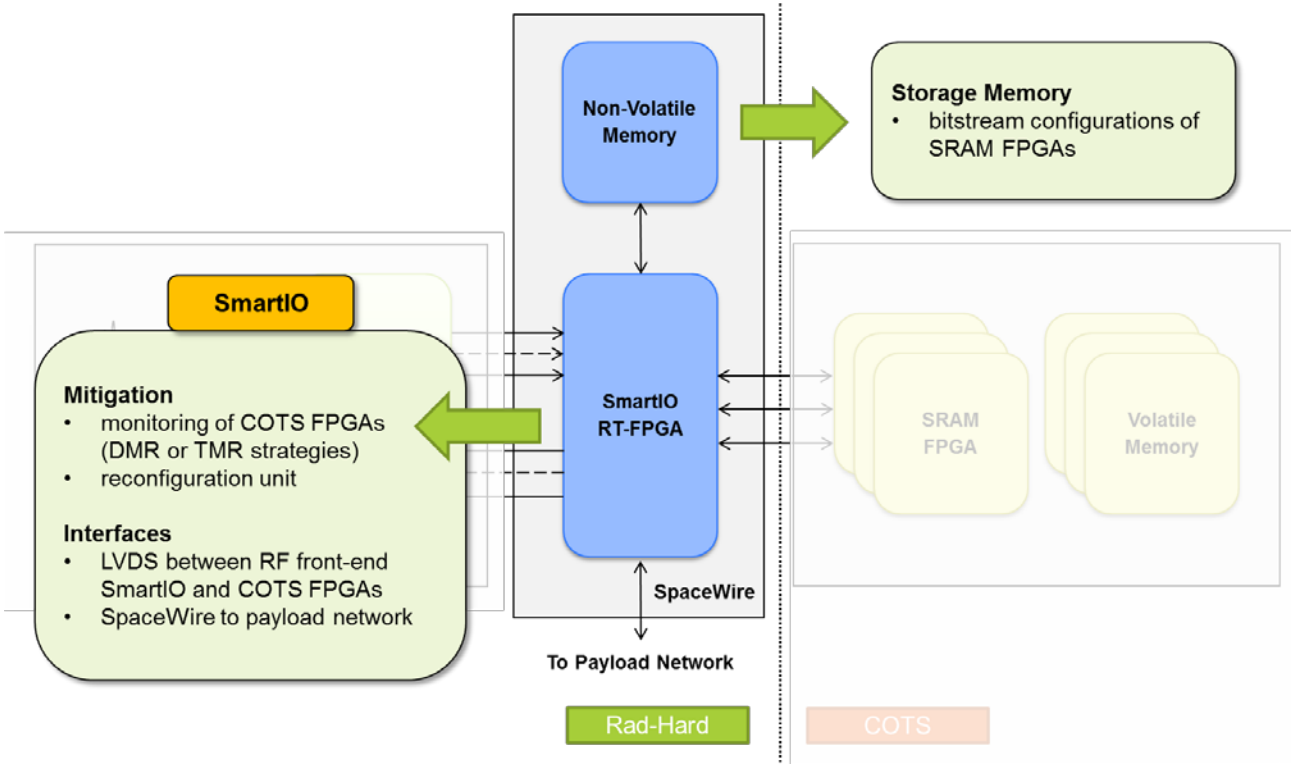
Application to SDR Payloads



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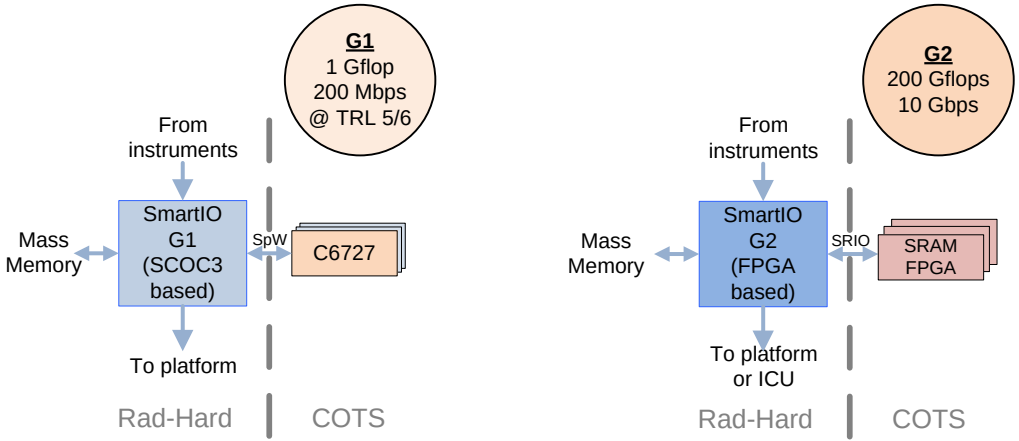
Summary

- **Reprogrammable FPGA's are essential for Payload / Instrument Processing**
- **High performance COTS Based computer study**
  - Demonstration with SCoC3 + DSP C6727
  - FPGA implementation in development (ACTEL + SRAM based FPGA) for Software Defined Radio



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Thank you for your attention

Questions ?

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