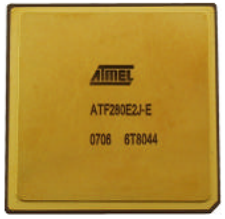
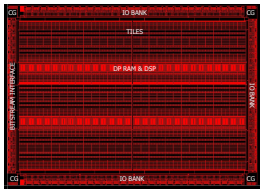
SEFUW: SpacE FPGA Users Workshop 3rd Edition



David Merodio Codinachs (ESA)
David Dangla (CNES)



Sponsors

Coffee breaks and

Cocktail reception during the Demo Session are sponsored by

Organization notes

1. **Presenters**:
    a. Provide the presentations (preferably during the breaks, latest the break prior to your presentation) or have your laptop ready.
    b. Do you agree on having it available at the ESA website? **Default: YES** (the final version can be provided another day)

2. **Attendees**:
    a. Do you agree to be included in the attendees list? **Default: YES**

Useful information

1. **Networking Coffee Break sponsored by CNES CTT and ESA TEC-ED**

2. **Networking Luncheon** at ESTEC main canteen

3. **Wireless access**:
    a. Login and password included at the back of your visitor badge. Valid throughout the workshop

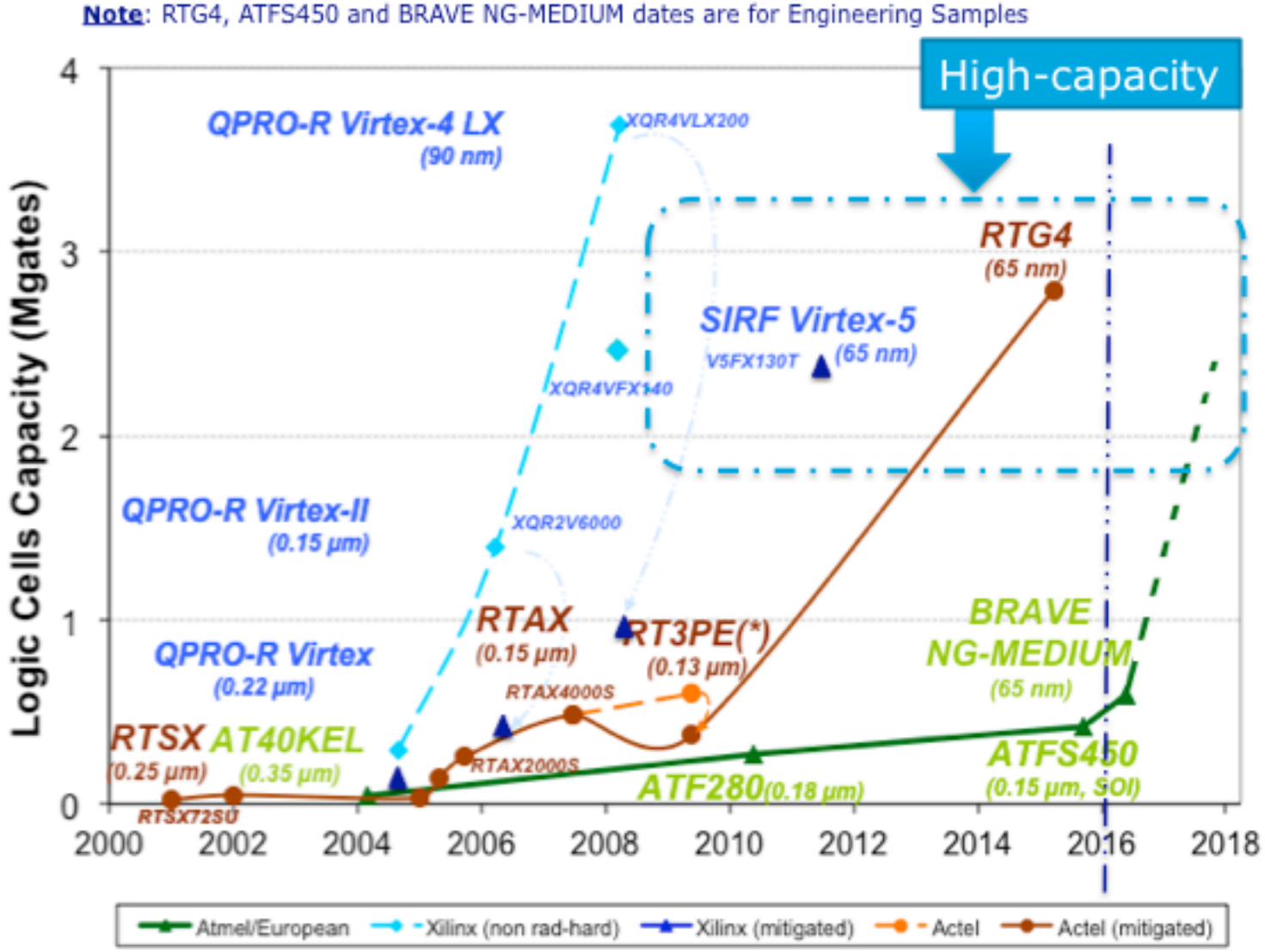
        SSID: **esa-public** Authentication: Open
        Username: *d.merodiocodinachs*
        Password: *xxxxxx*

If your badge does NOT include this information, please report to the Registration Desk

Useful information

1. **Shuttle services (to Noordwijk or the airport)**: please make your reservation at the ESTEC main reception desk

FPGA updates/ trends:
Larger and higher performance FPGAs



BRAVE – Introduction and General objectives (I)

1. BRAVE:

   Big Re-programmable Array for Versatile Environments

2. Main Goal:

> Provide to the Space Industry a High-capacity, high-performance radiation hardened reprogrammable European FPGA

3. Main motivation:

   a. Competitive FPGA capacity, performance and radiation hardness to be used in a wide range of space equipment across all ESA missions in Science, Exploration, Earth Observation, Telecom and Navigation. Also in Launchers and Human Spaceflight.

   b. FPGA unlimited re-programmability extra advantage: enable re-configurable and adaptive systems; and also reduces impacts in the (frequent) event of unexpected design changes or modification

BRAVE – Introduction and General objectives (II)

1. Extra motivations/ considerations:
    a. FPGA cost advantages:
        - FPGAs offer shorter development times, simpler, less expensive design and manufacturing phases than Application Specific Integrated Circuits (ASICs).
        - **SMEs** have access to FPGAs and often cannot afford advanced ASIC technologies (i.e. enable SMEs to develop complex digital functions that otherwise could not afford).
    b. Reduce dependency on USA EAR/ITAR FPGA key components
    c. Extend and keep the European Competence to develop FPGAs and capability to specify and develop future FPGA products for space.

ENJOY THE 3rd DAY OF THE WORKSHOP !!!