SET effects analysis and mitigation on Flash-based FPGAs

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Goal

- Analysis of Single Event Transients (SETs) occurrency
- Effective SET mitigation

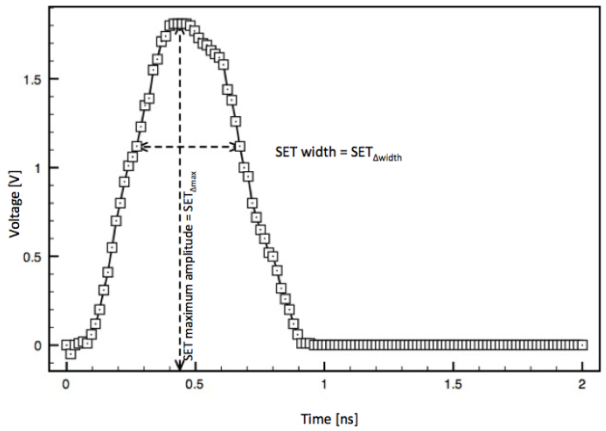
Outline

- SET effects on Flash-based FPGAs
- Single Event Transient Analysis (SETA) tool
  - Analysis
  - Mitigation
  - Experimental results
- Conclusions and future activities

SET effect

- A Single Event Transient (SET) is generated by the injunction of charge collection
  - A charged particle crosses a junction area
  - It generates an amount of current, provoking a “glitch”
  - SET can be indistinguishable from normal signal and exist for notable distances

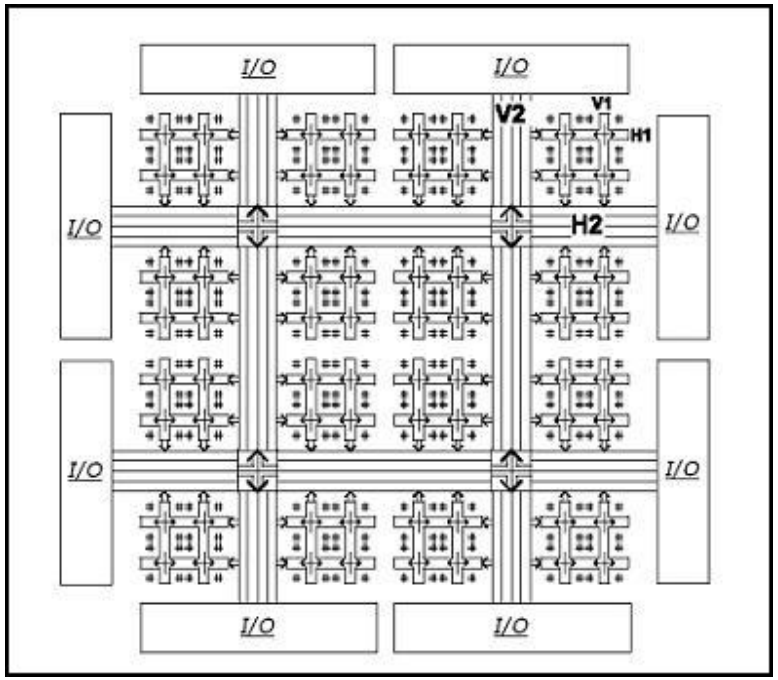
SET width
SET amplitude
Rise ΔV/ΔT
Fall ΔV/ΔT



Circuits on Flash-based FPGAs

0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0

Flash configuration memory

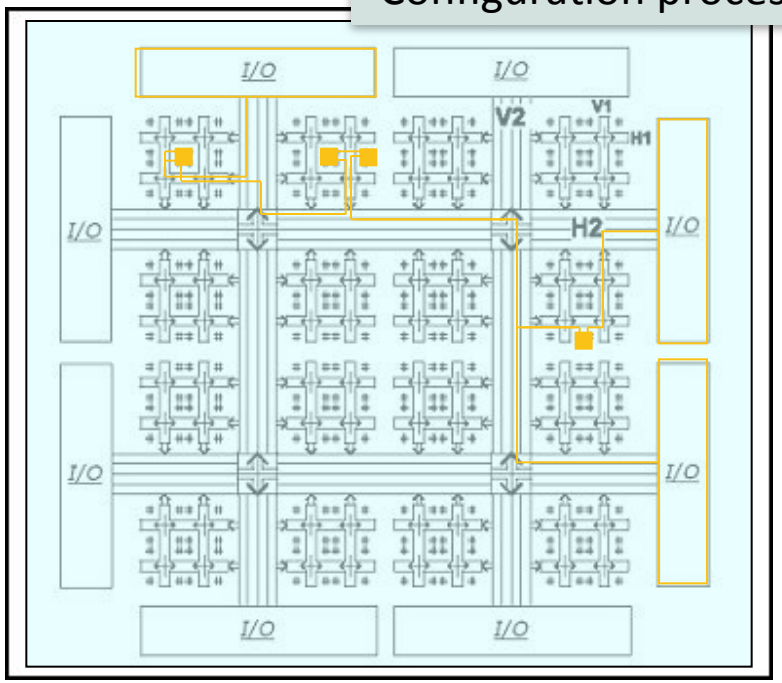


FPGA array

Circuits on Flash-based FPGAs

Configuration process

0	1	0	0	0	0
1	0	0	0	0	0
1	1	0	0	0	0
0	0	0	0	1	0
0	1	0	1	0	0
0	0	0	0	0	0

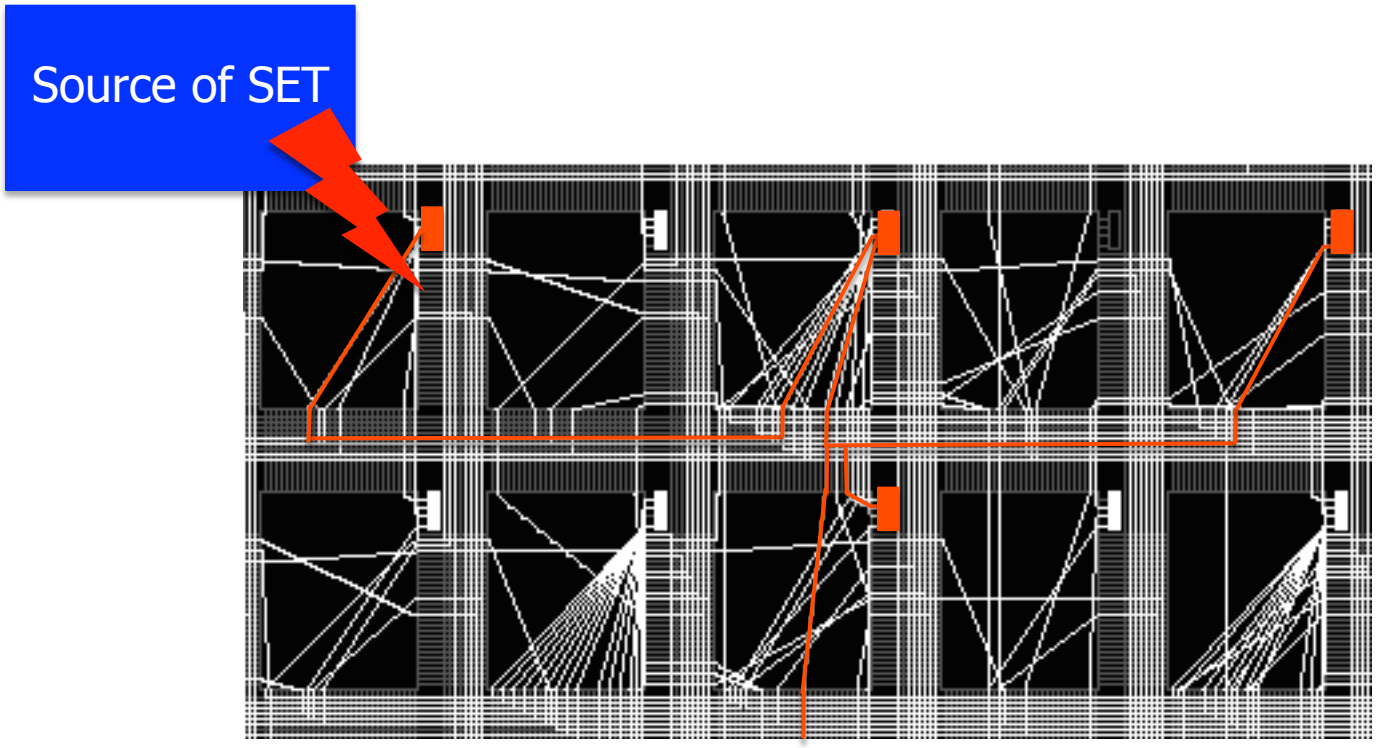


Flash configuration memory

FPGA array

SET scenario

- Considering a place and route design on FPGA
  - Fixed logic cells
  - Defined number of routing segments



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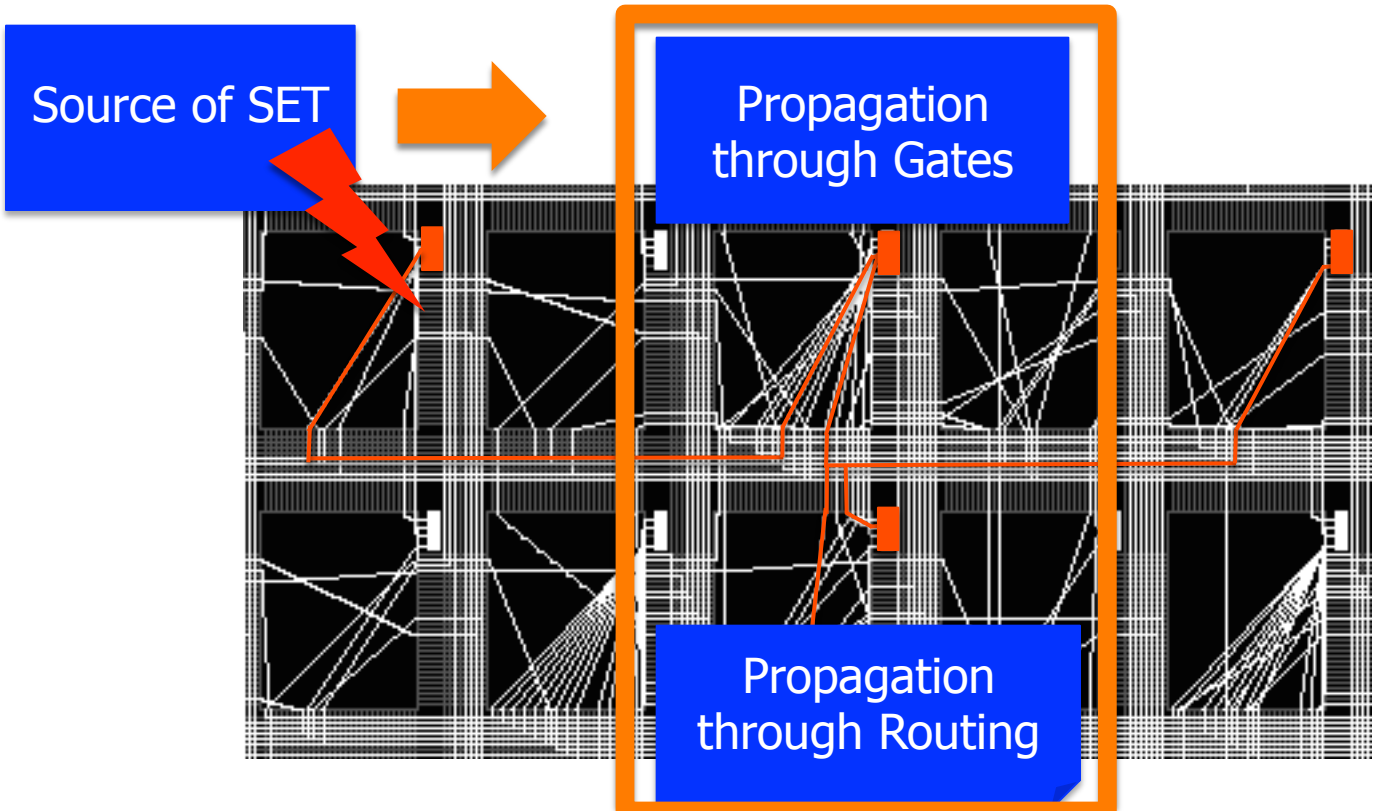

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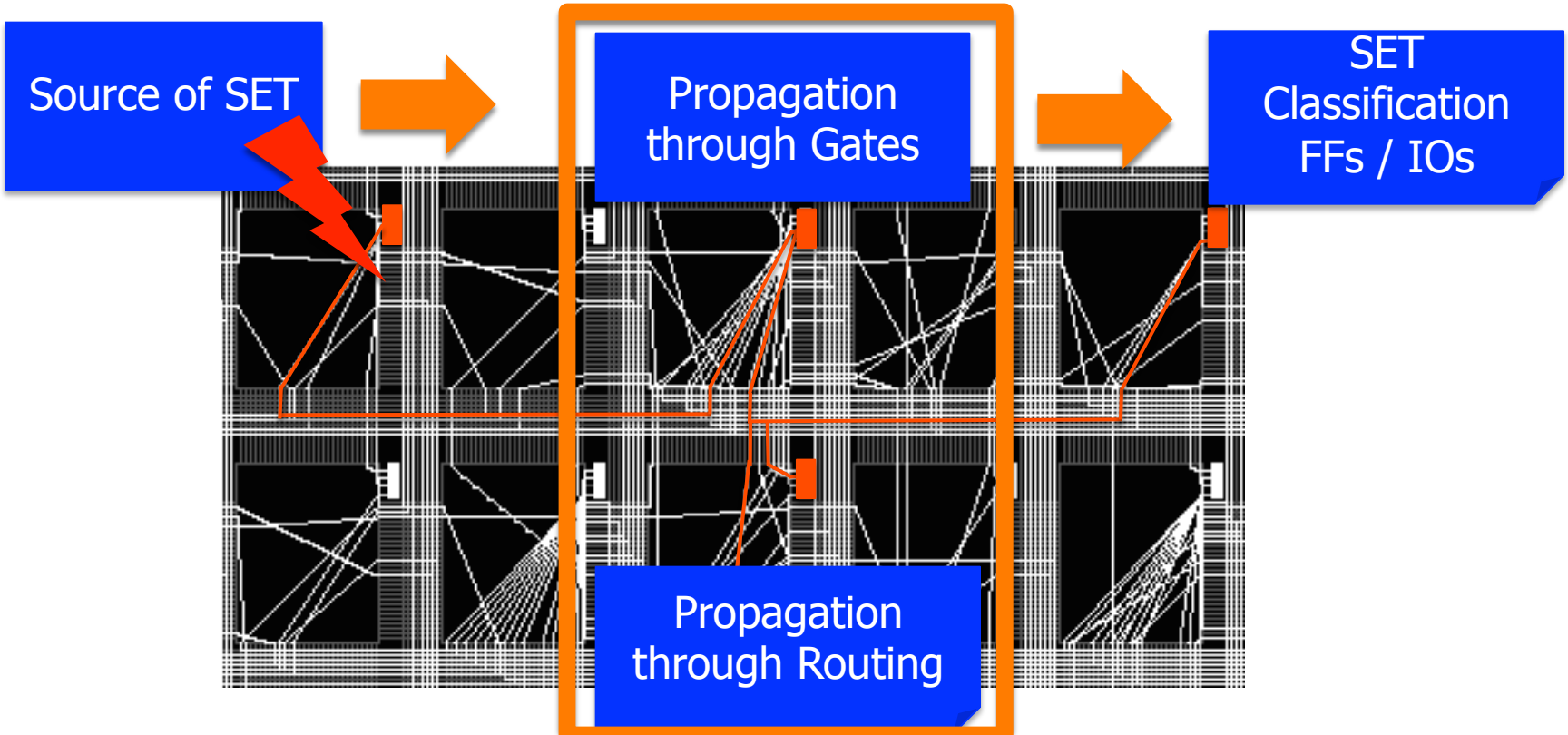


SET Propagation through gates

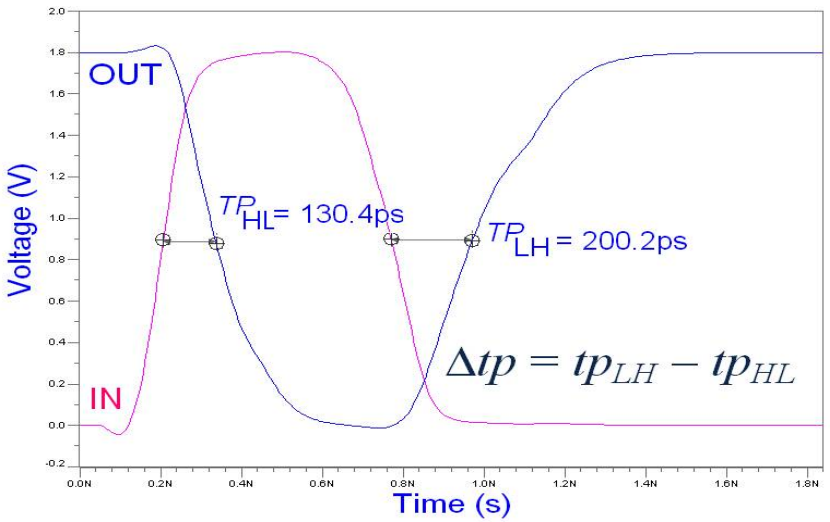
[Wirth et al, NSREC 2008]

Fist Region: If($\tau_n < k*tp$) then $\tau_{n+1} = 0$

Second Region: If ($\tau_n > (k+3)*tp$) then $\tau_{n+1} = \tau_n + \Delta tp$

Third Region: If ($(k+1)*tp < \tau_n < (k+3)*tp$) then $\tau_{n+1} = (\tau_n^2 - tp^2)/\tau_n + \Delta tp$

Fourth Region: If ($k*tp < \tau_n < (k+1)*tp$) then $\tau_{n+1} = (k+1)*tp(1 - e^{(k-(\tau n / tp))}) + \Delta tp$



For a 1→0→1 transition Δtp is defined as:

$\Delta tp = tpHL - tpLH$

For a 0→1→0 transition Δtp is defined as:

$\Delta tp = tpLH - tpHL$

Source of SET
Propagation through gates
Propagation through routing
SET classification on FFs or IOs

SET Propagation through gates

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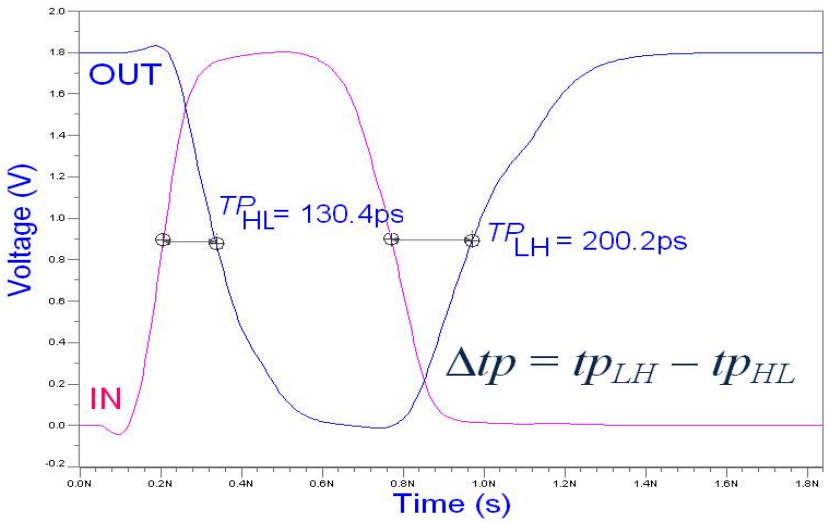

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- **V Propagation through gates**
- **Propagation through routing**
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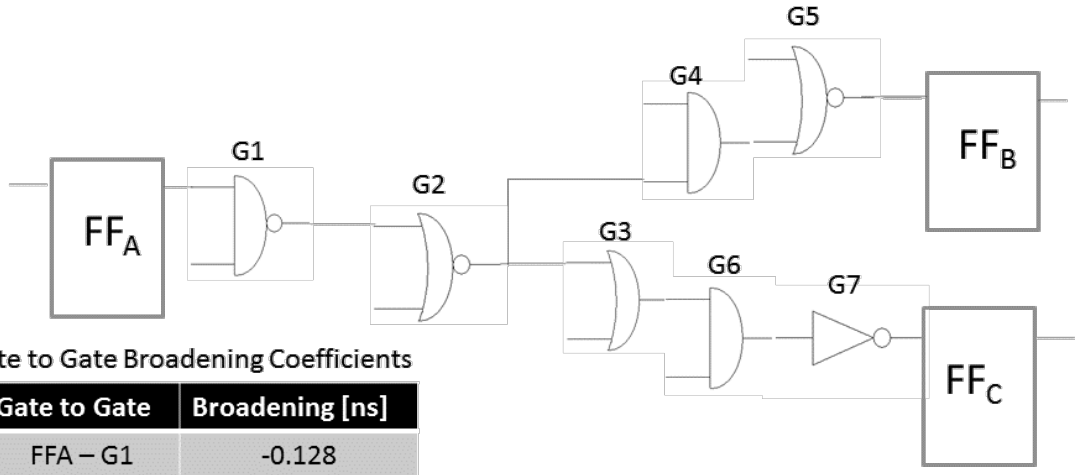
SET Propagation through routing

[Sterpone et al, RADECS 2014]



Gate to Gate Broadening Coefficients

Gate to Gate	Broadening [ns]
FFA – G1	-0.128
G1 – G2	0.458
G2 – G4	0.070
G2 – G3	-0.090
G3 – G6	0.480
G6 – G7	0.092
G7 - FFC	0.140
G4 – G5	-0.094
G5 - FFB	0.130

FFs maximal broadening pulses

Flip-Flop	Maximal Pulse [ns]
FFB	0.436
FFC	0.952

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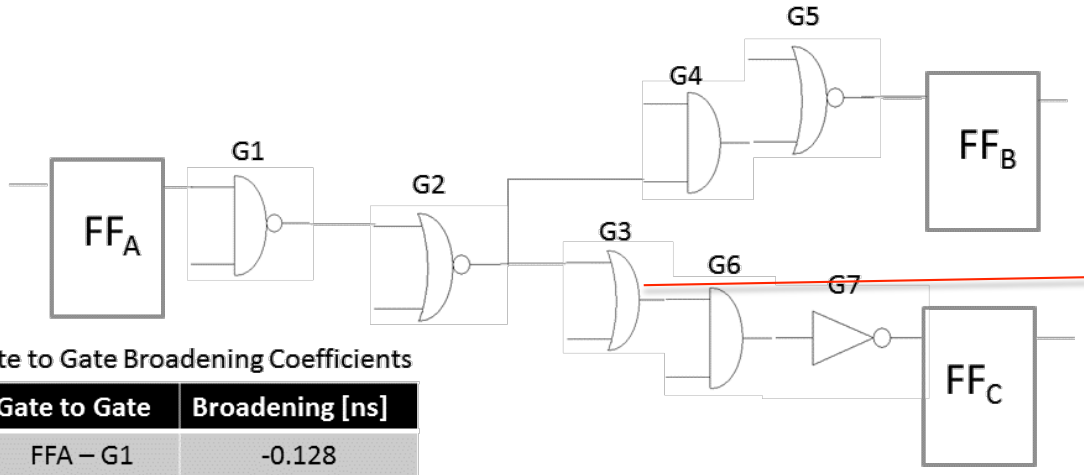

Propagation Induced Pulse Broadening

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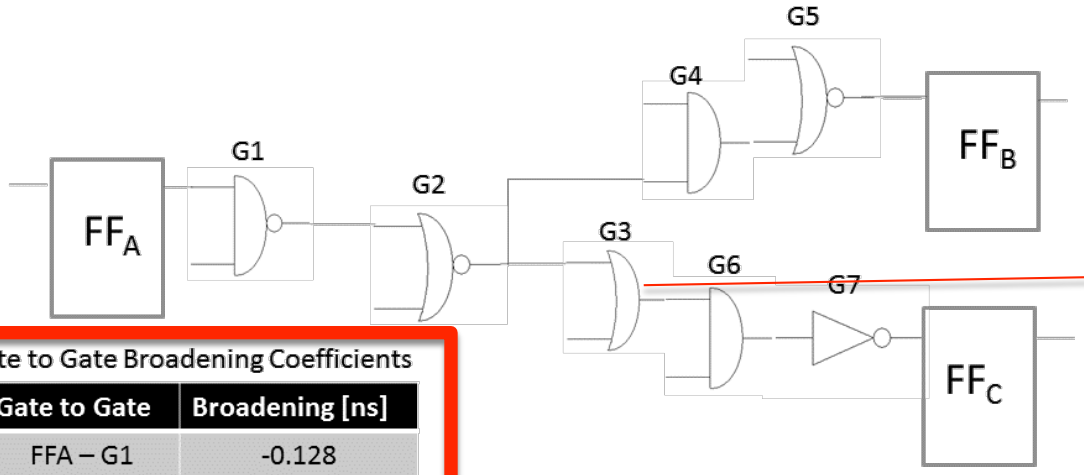

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Propagation Induced Pulse Broadening

Gate to Gate Characterization

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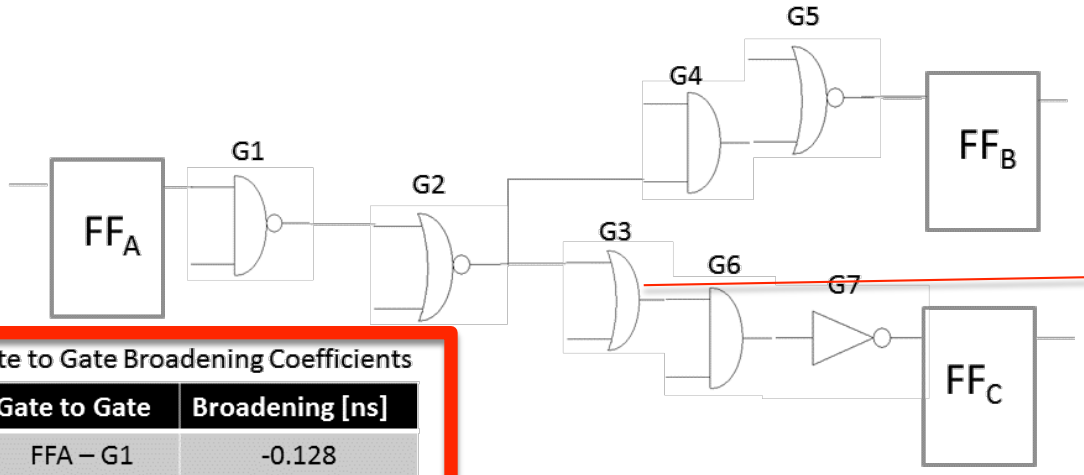

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Propagation Induced Pulse Broadening

Gate to Gate Characterization

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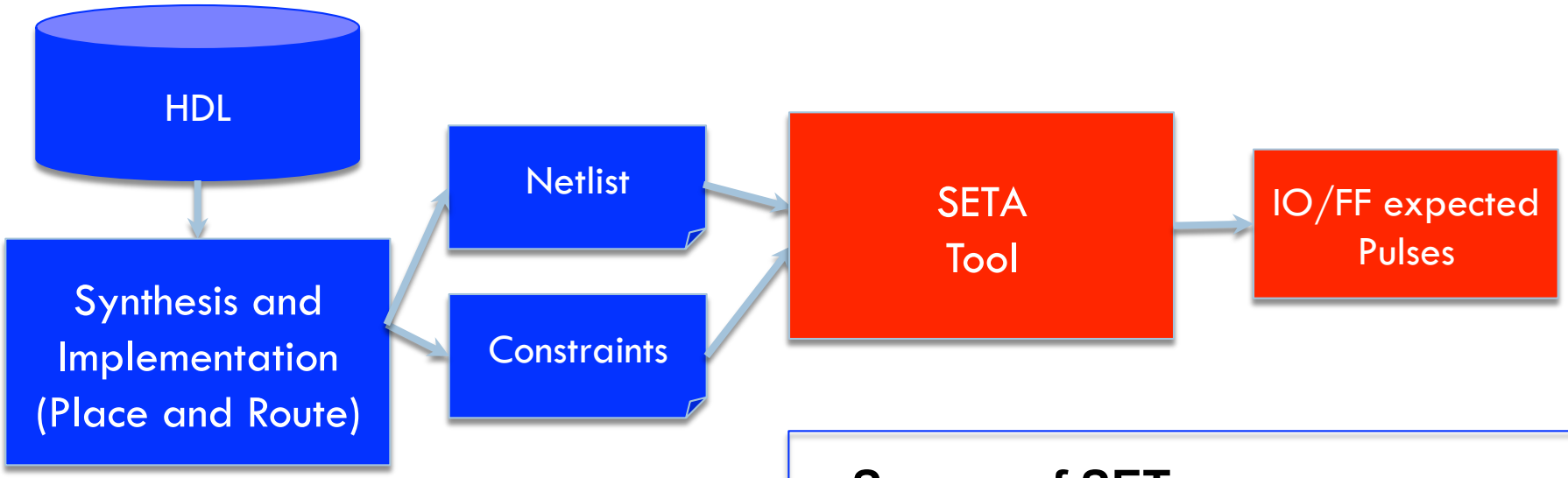
SET classification on FFs or IOs

SET classification on FFs and IOs

- A tool has been developed:
  - Single Event Transient Analyzer (SETA)



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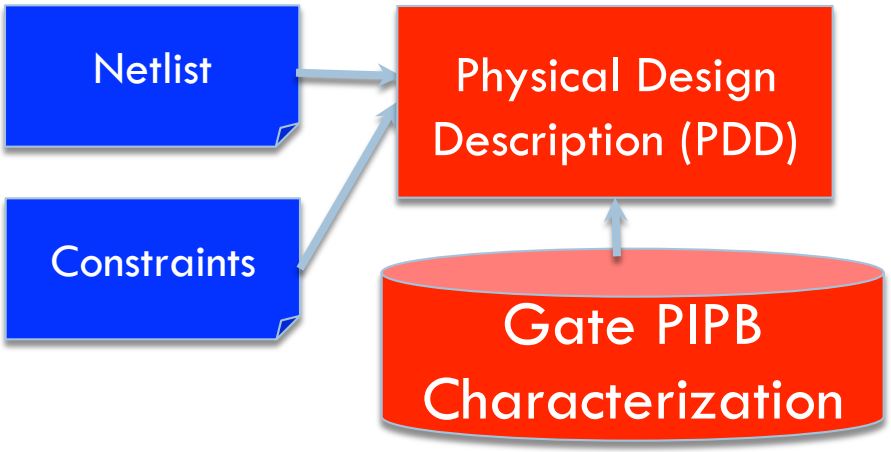

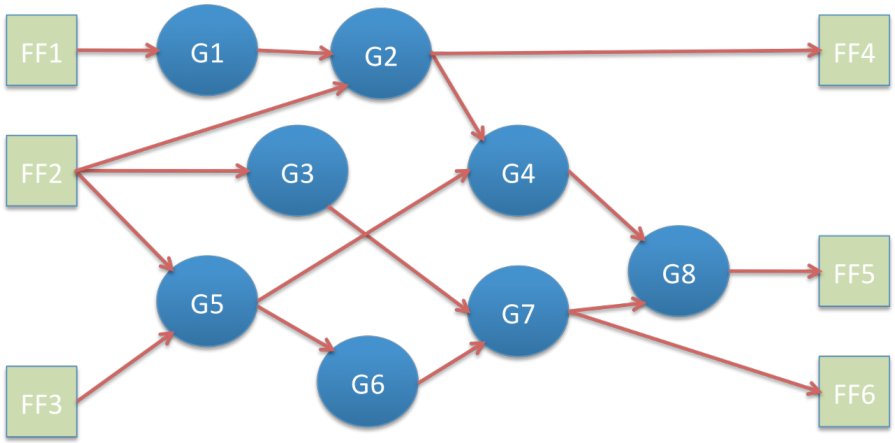

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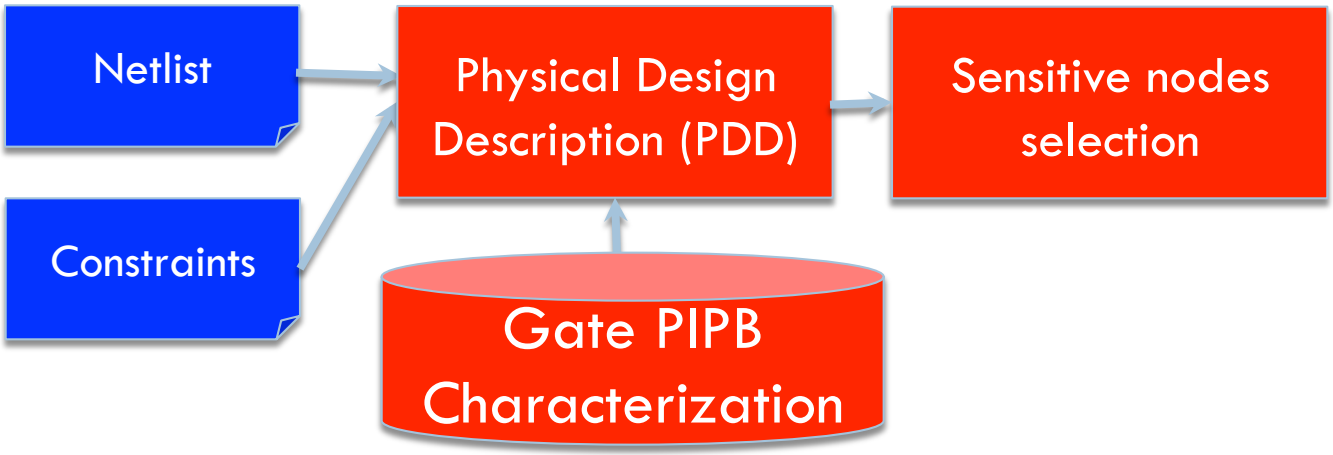

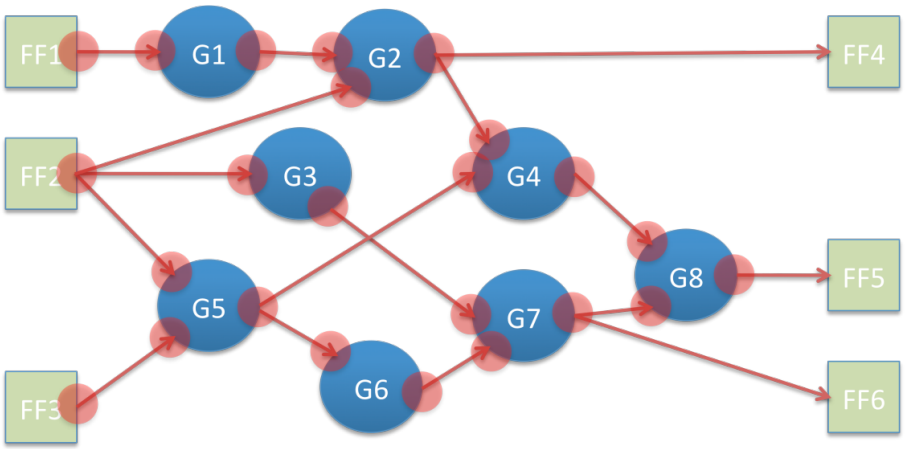

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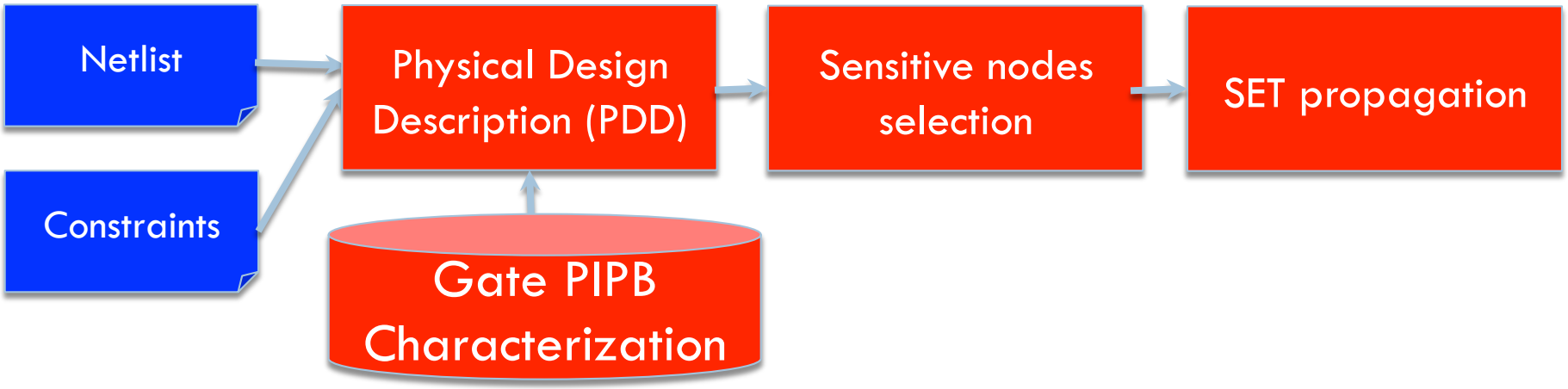

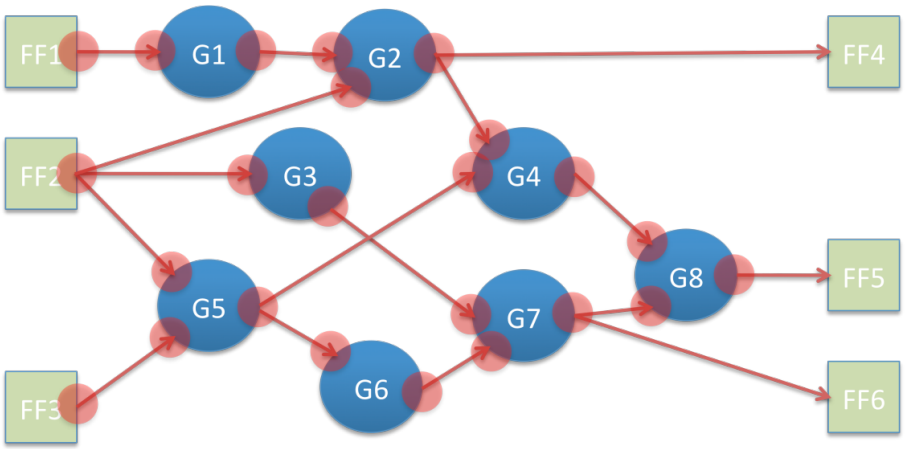

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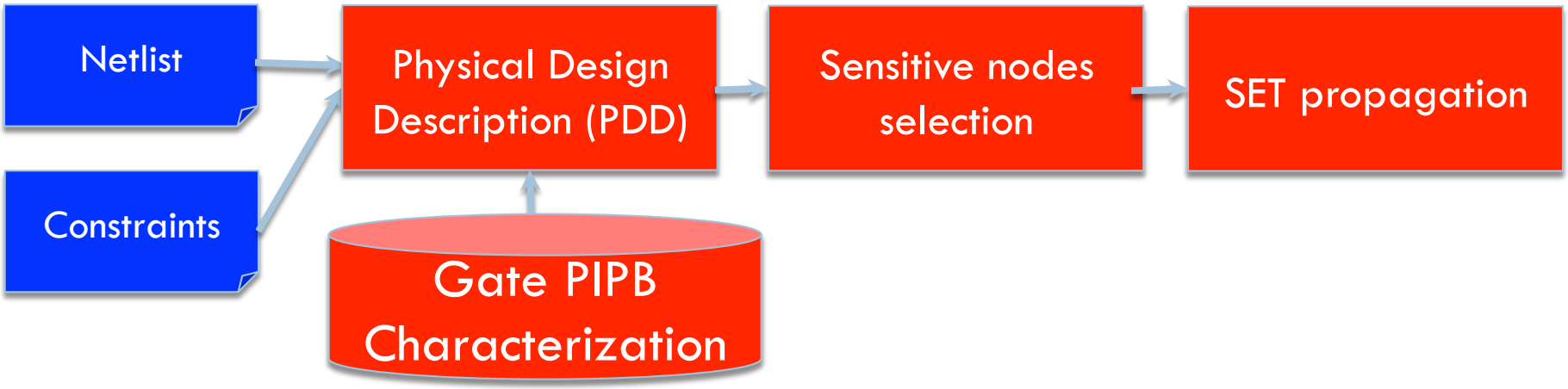

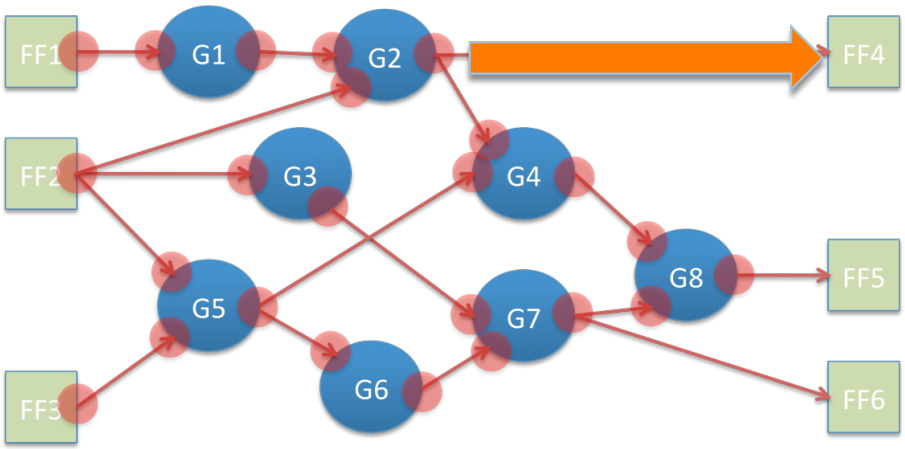

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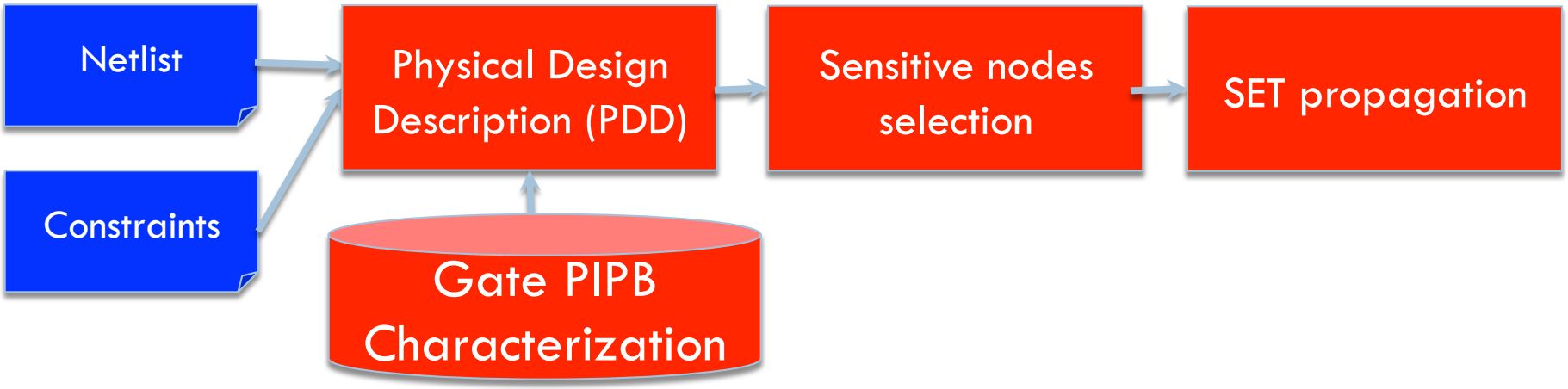

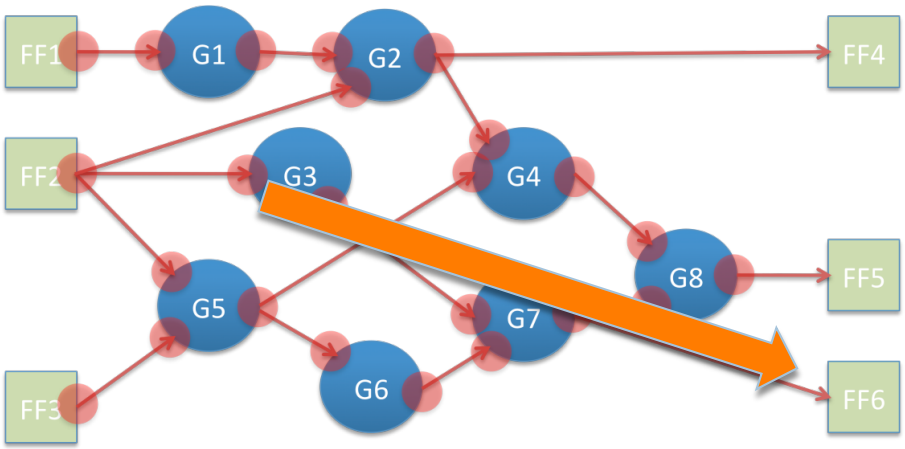

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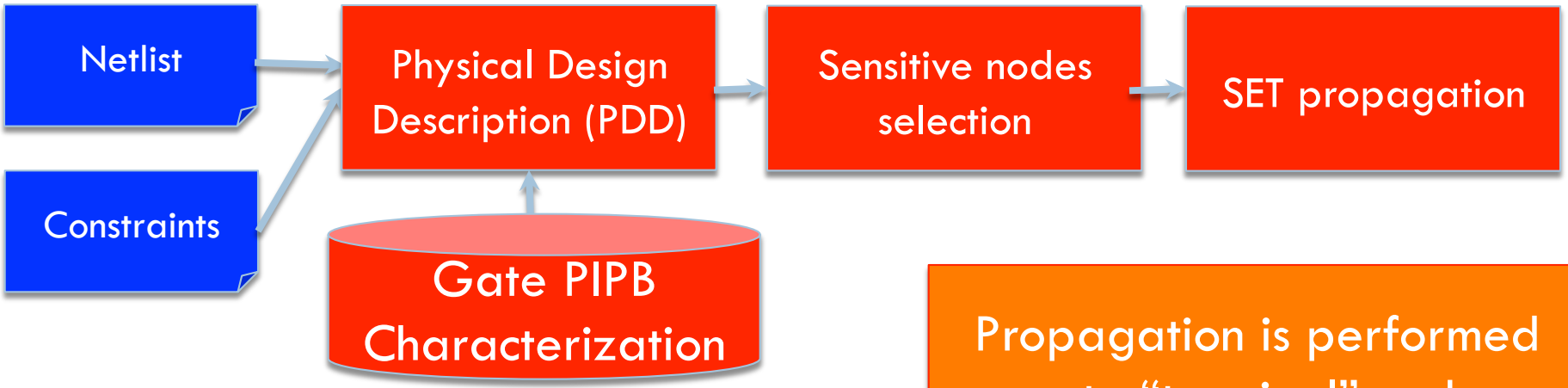
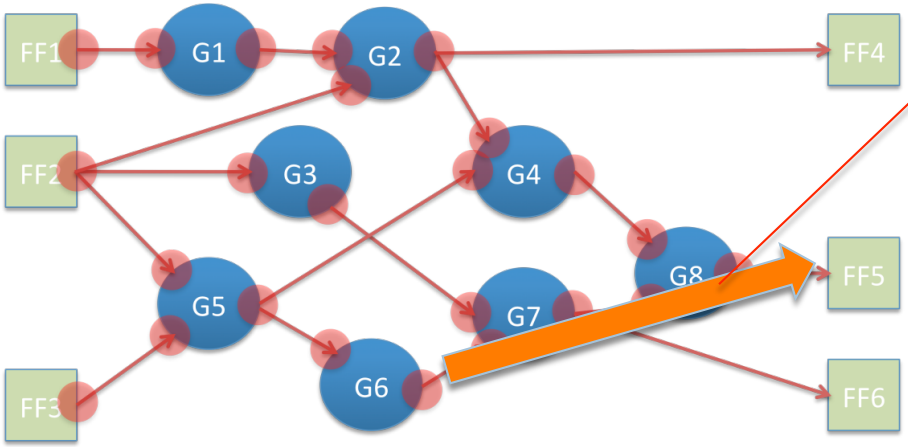
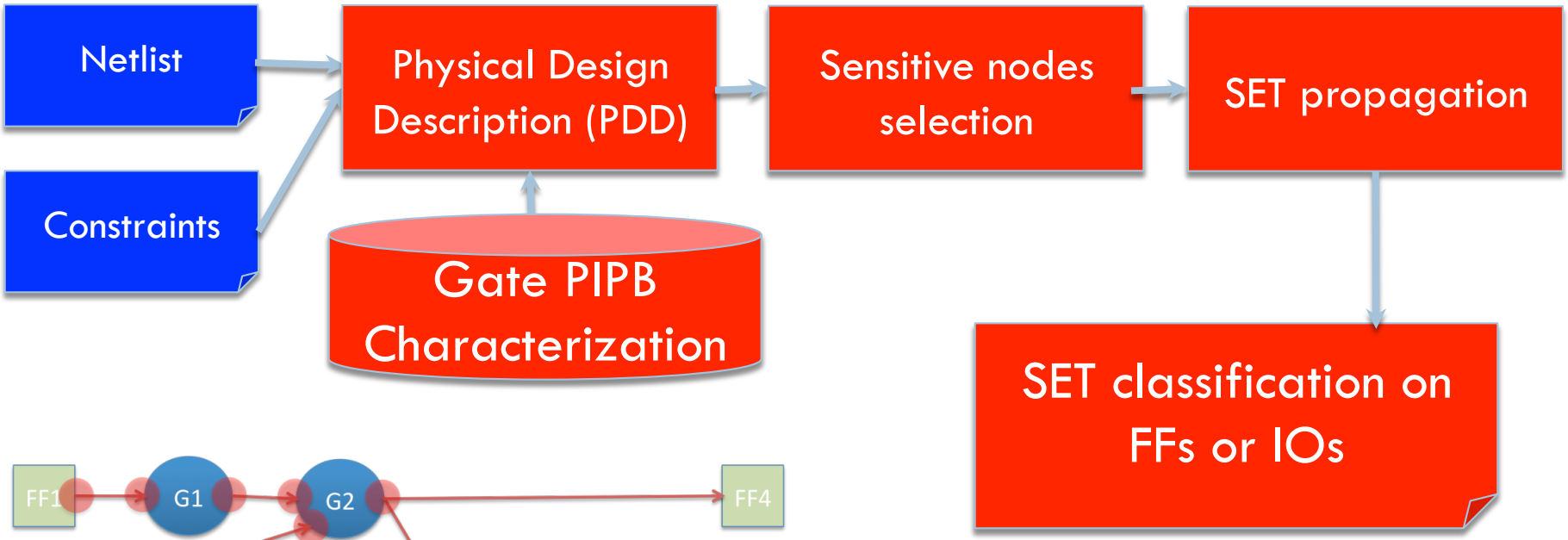


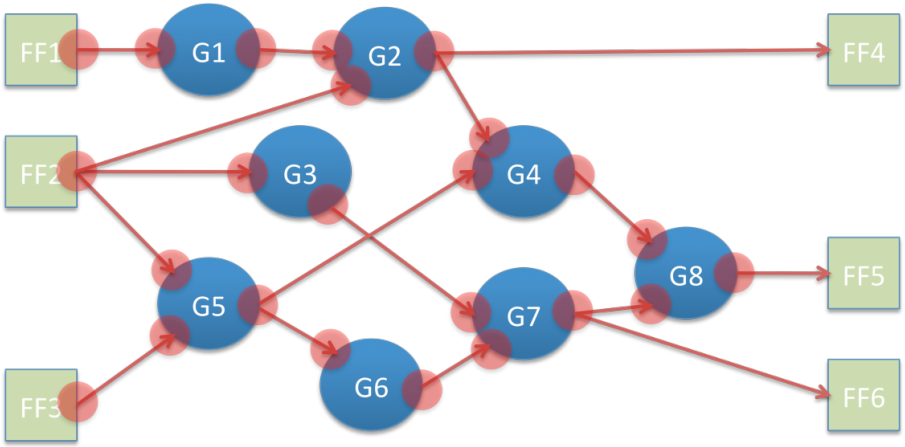


Propagation is performed up to "terminal" nodes (IOs / FFs)

Source of SET
V Propagation through gates
V Propagation through routing
SET classification on FFs or IOs

SETA tool





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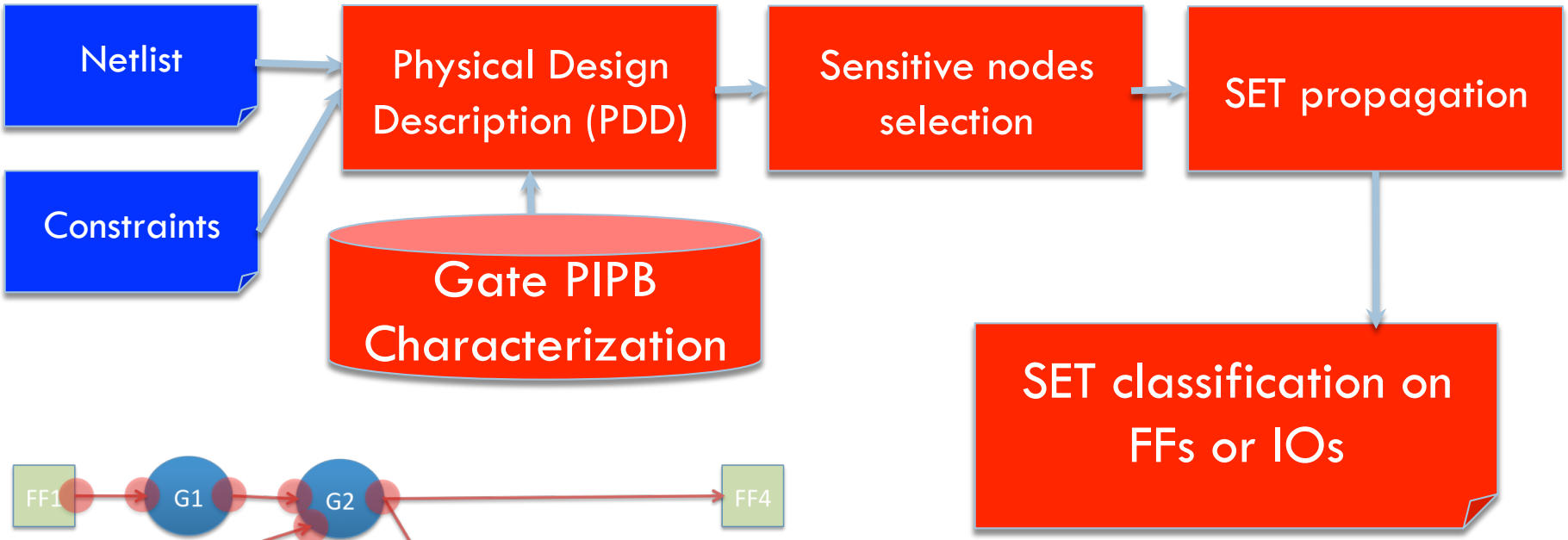
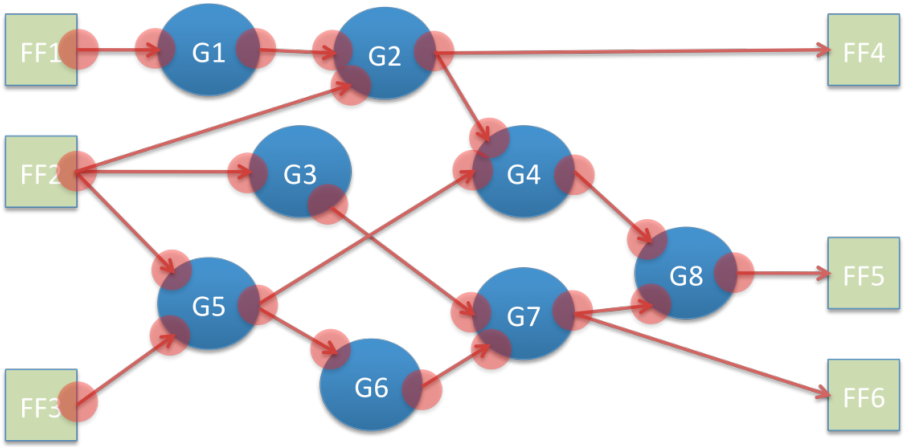


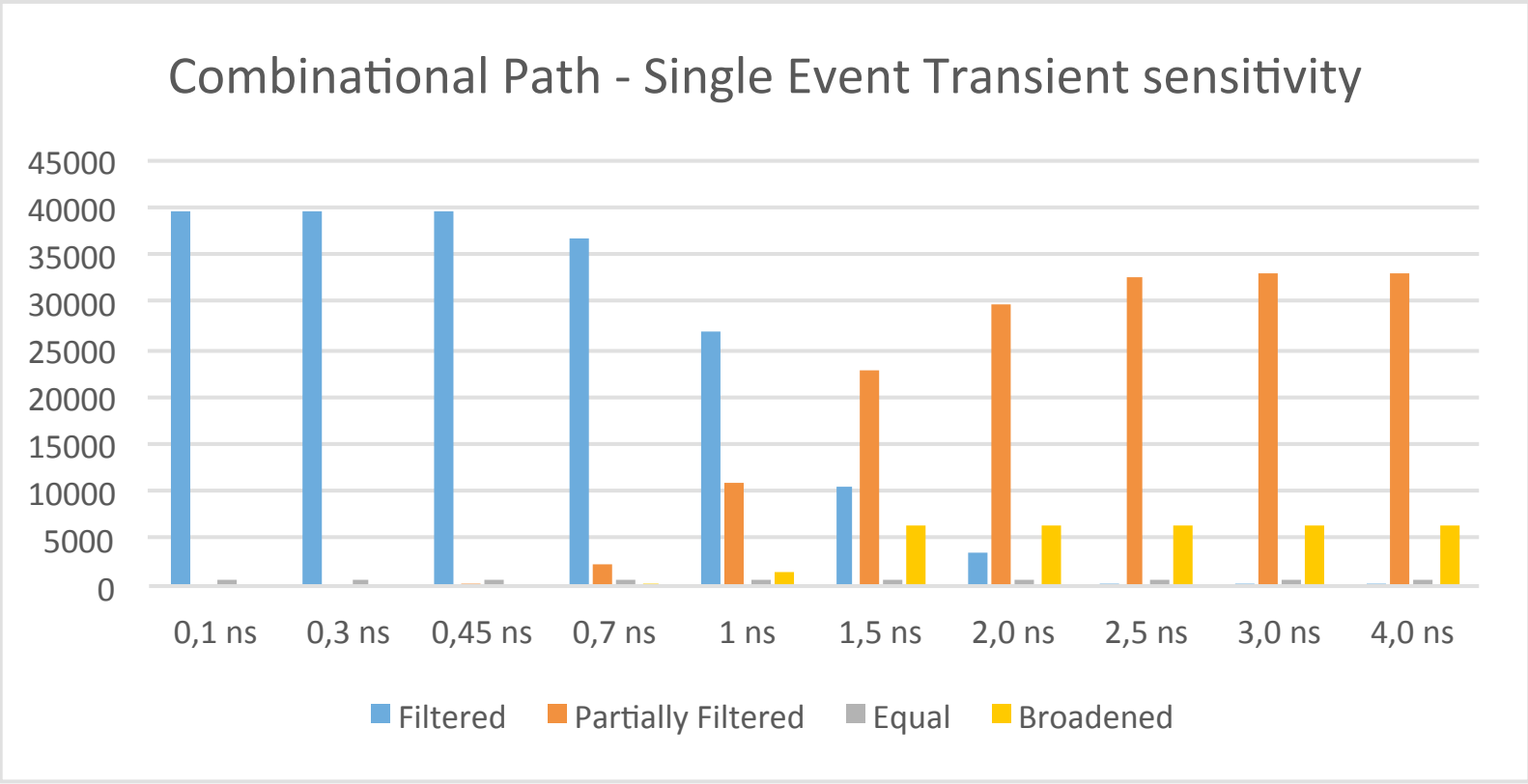


- Source of SET
- V Propagation through gates
- V Propagation through routing
- V SET classification on FFs or IOs

SET classification on FFs and IOs

- The classification identifies the number of SET:
  - Totally filtered
  - Partially filtered
  - Equally propagated
  - Broadened

SETA results – EUCLID project (WP1)



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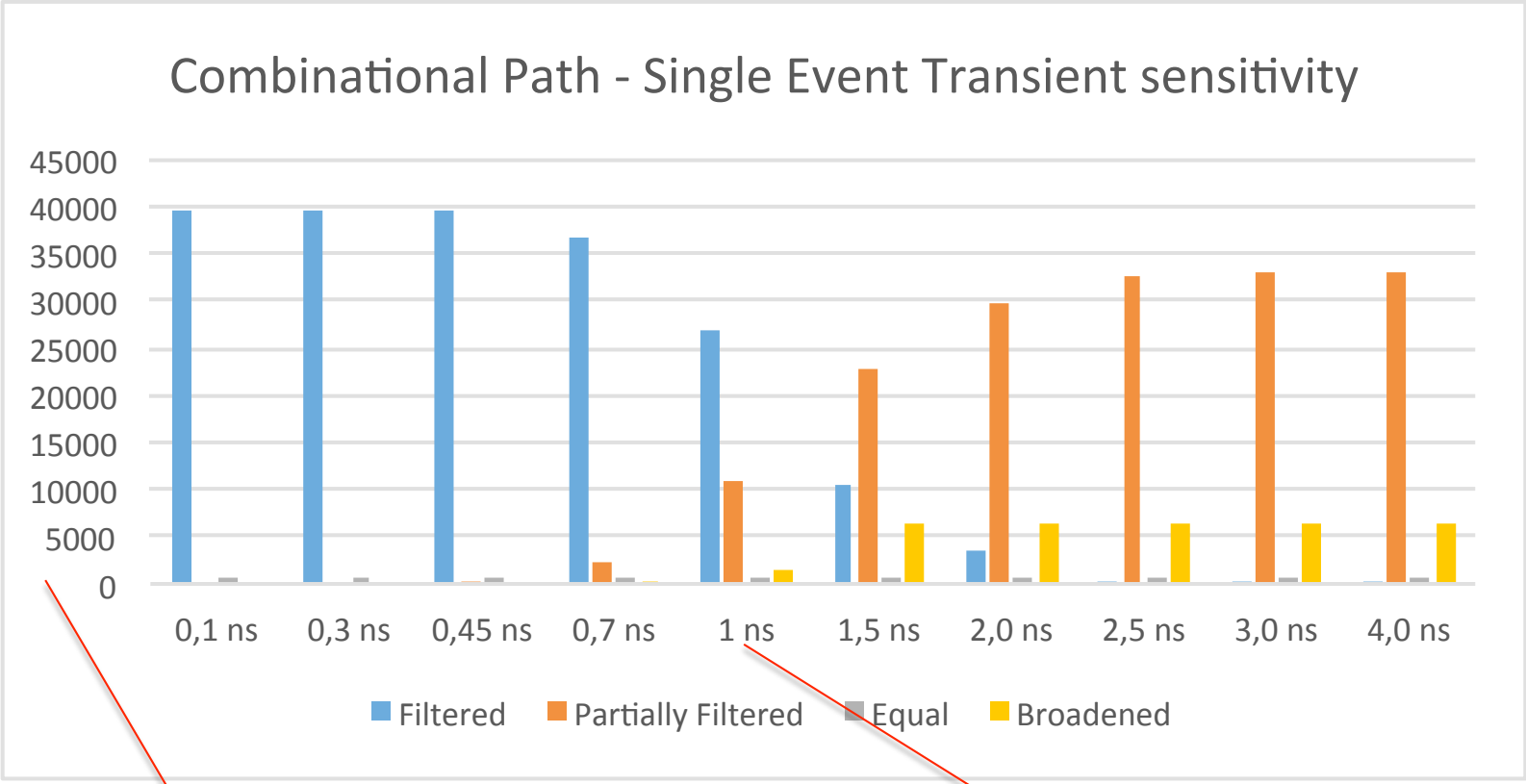


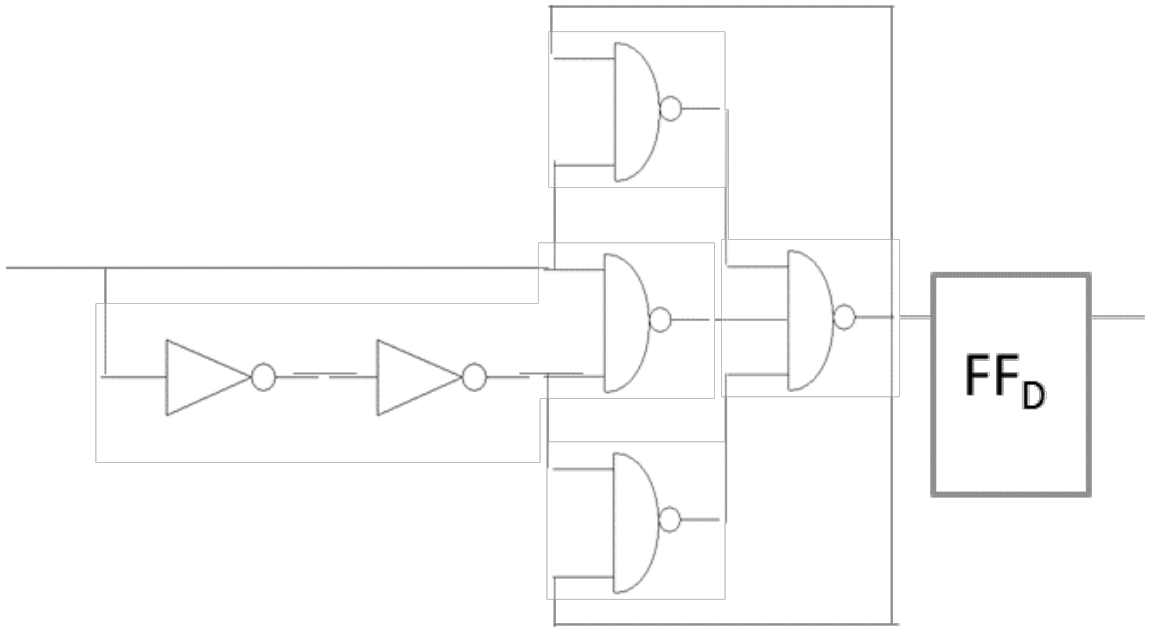
Total number of analyzed SET

Type of SET per injected pulse

SET: mitigation

[Sterpone and Du, IEEE ETS 2014]

- Selective guard gate (GG) mapper
  - Inserting a GG logic structure in the input of the selected FF



SET: mitigation solution 1

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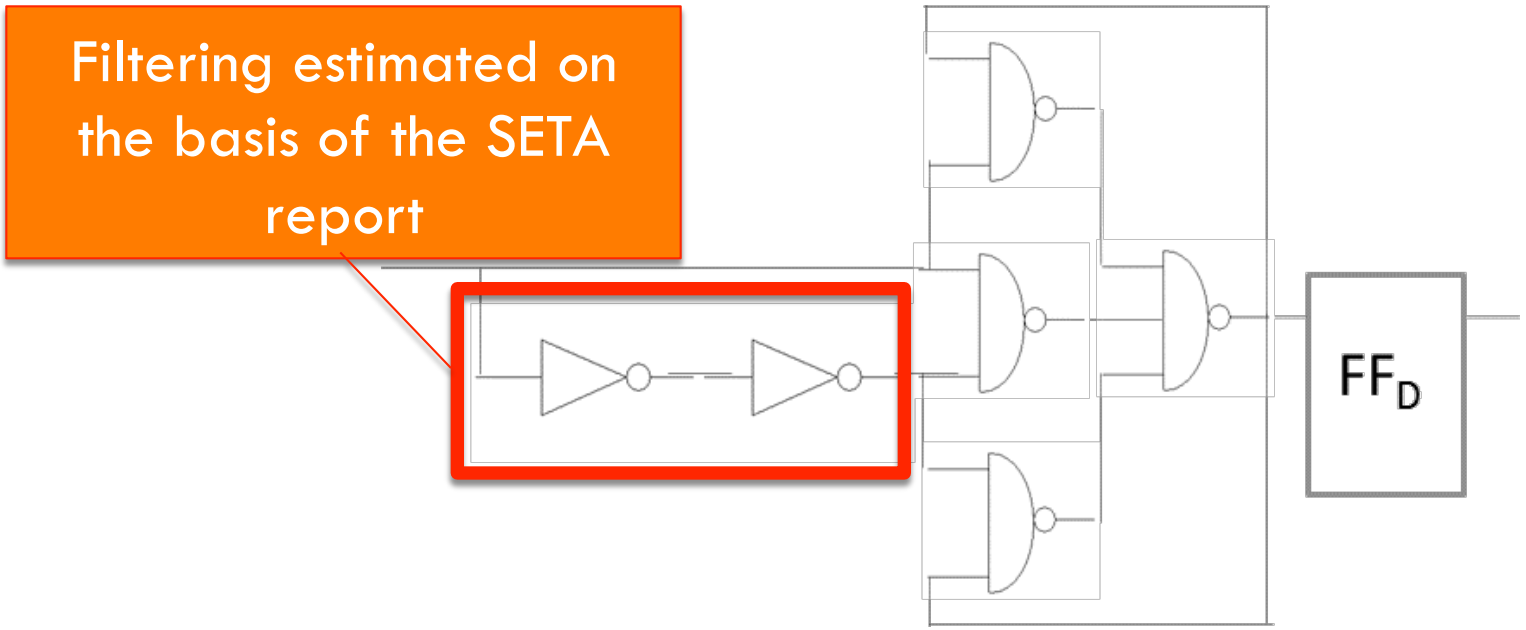
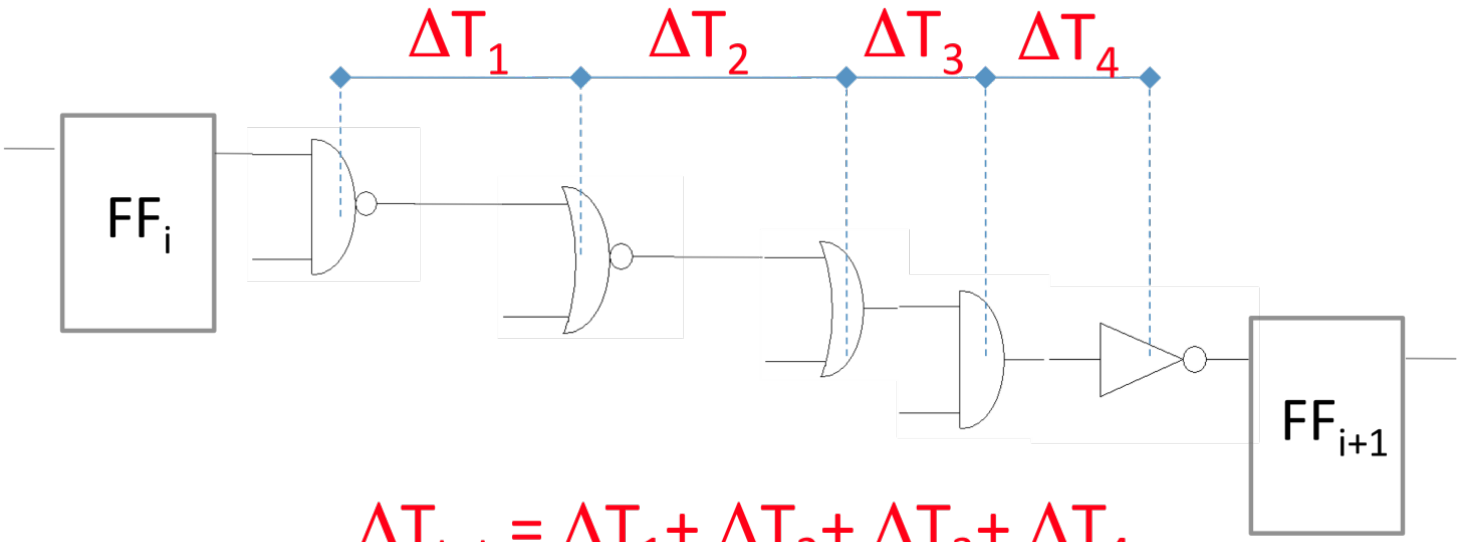


SET: mitigation solution 2

[Sterpone and Du, IEEE ETS 2014]

- Accurate placement acting on the critical paths
  - Distance between gates is modified in order to maximize the electrical filtering effect



$$\Delta T_{tot} = \Delta T_1 + \Delta T_2 + \Delta T_3 + \Delta T_4$$

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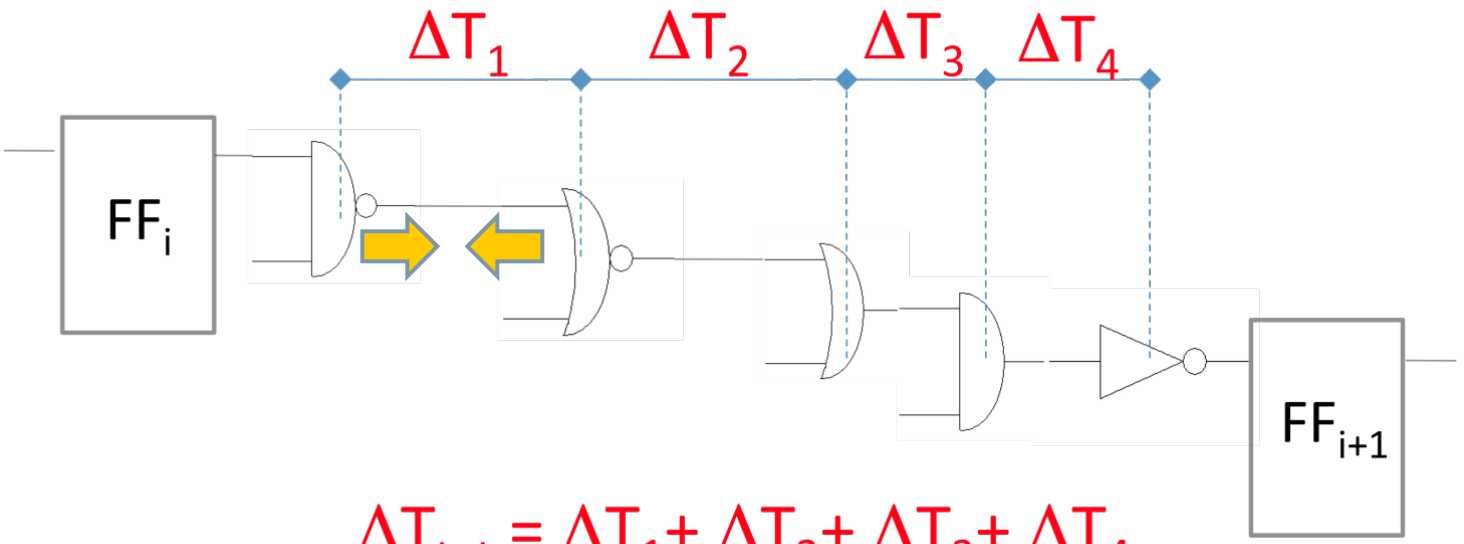

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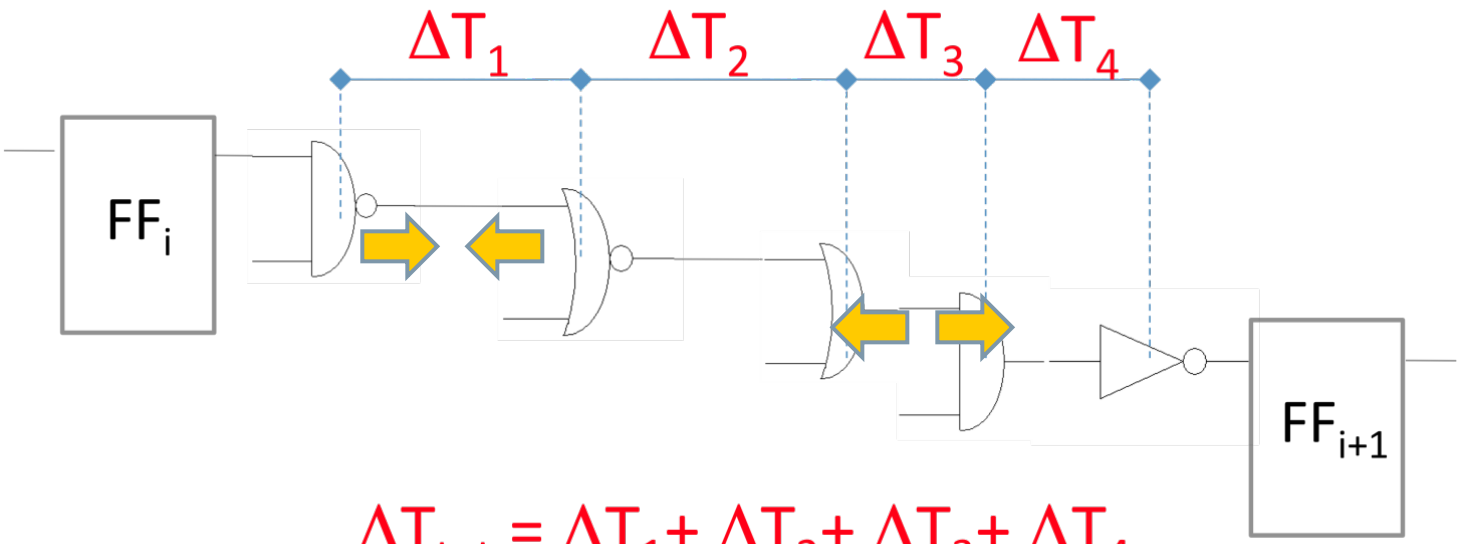
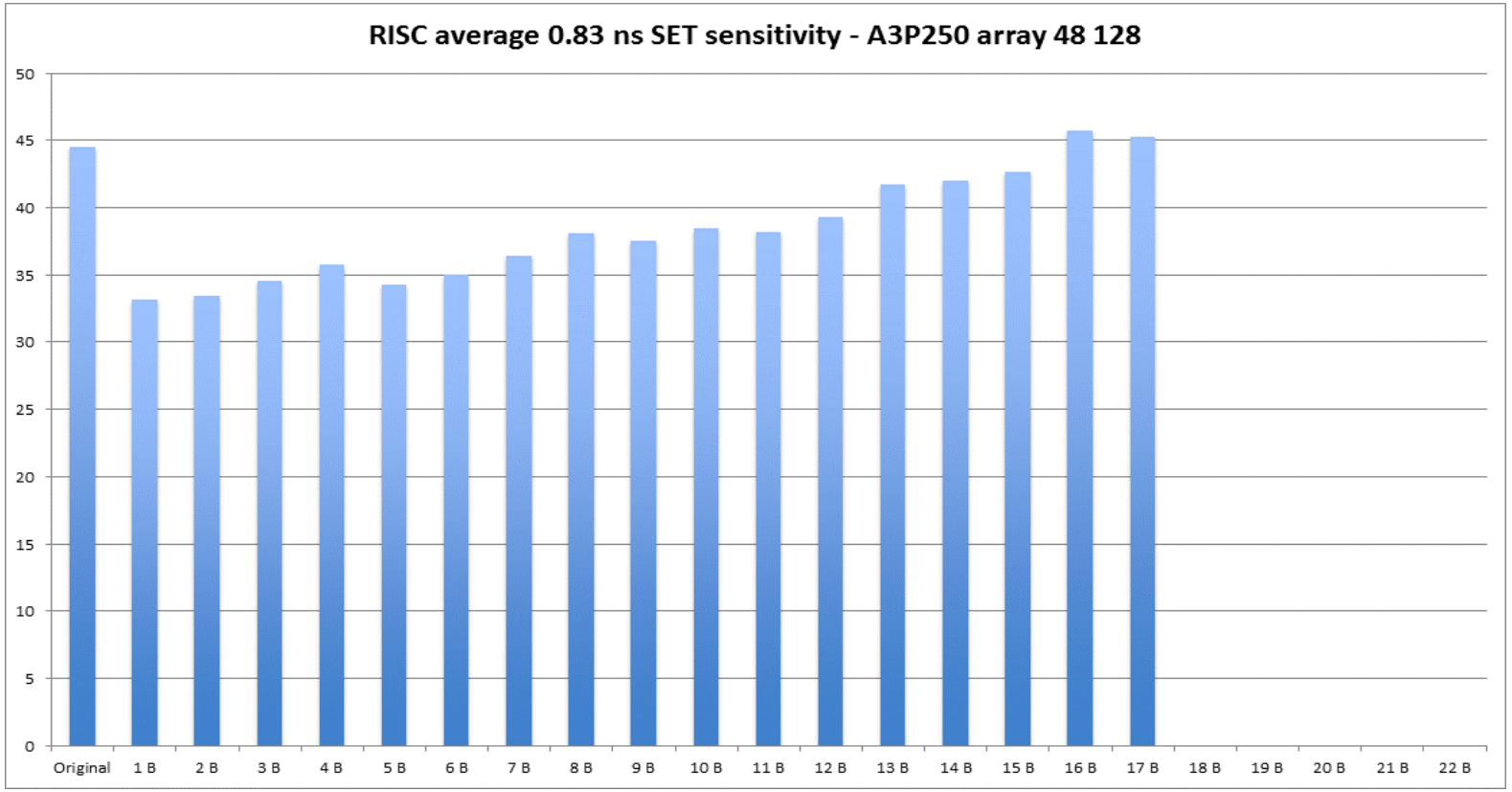


SET: mitigation results

Average SET sensitivity



Different place and route constraints

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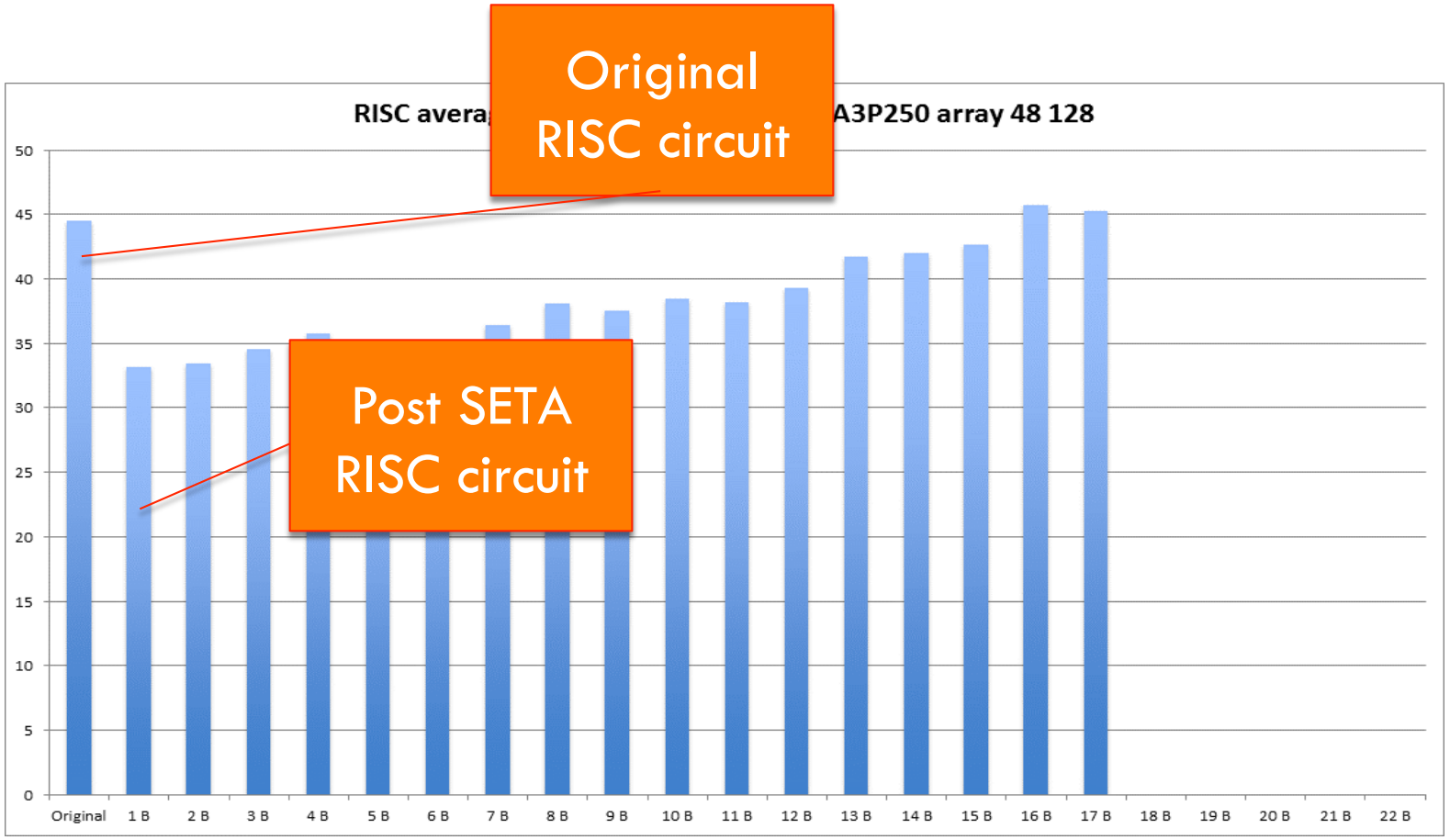

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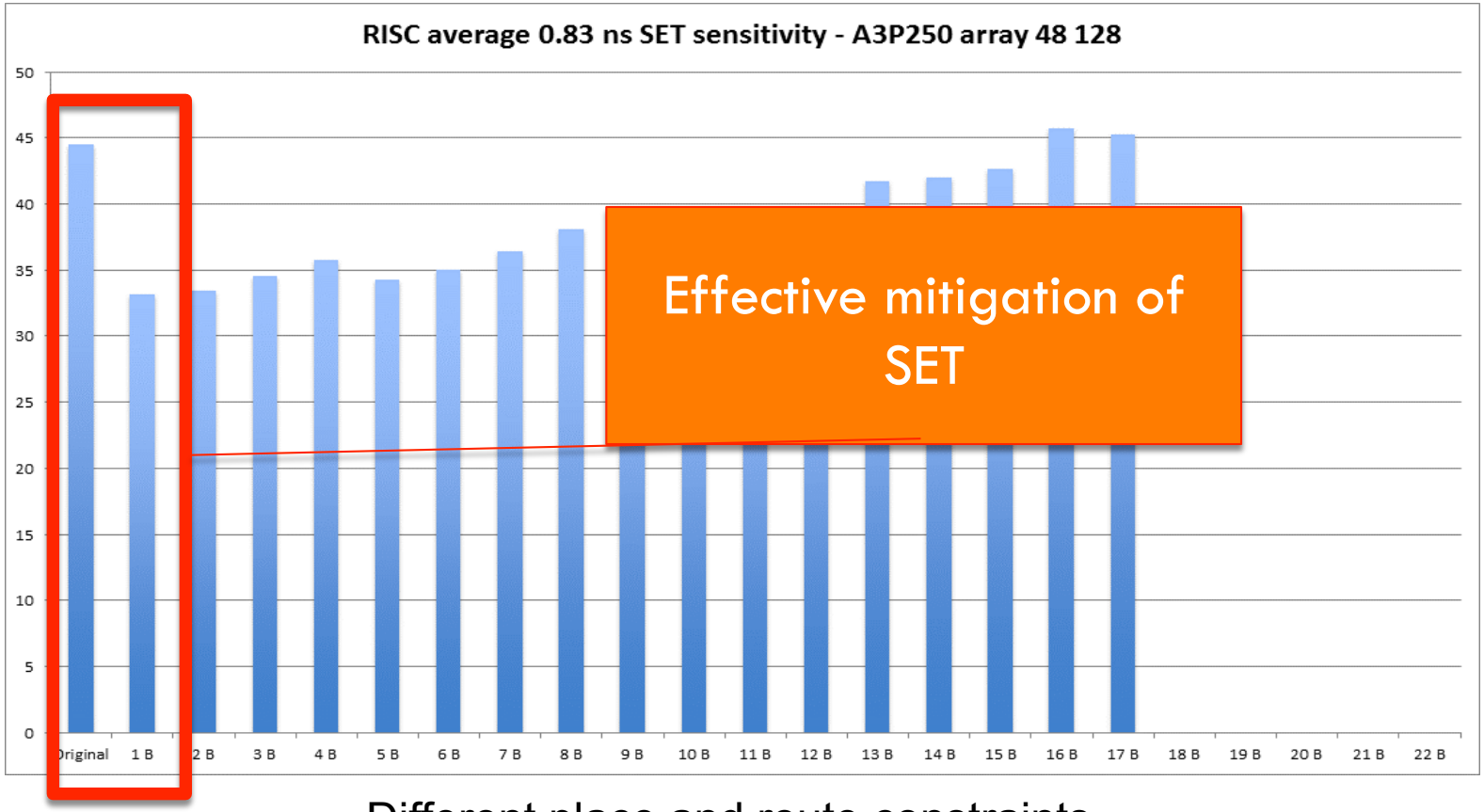

Different place and route constraints

SET: mitigation radiation test results

- Heavy ions test performed at the Cyclotron of the Université Catholique de Louvain (UCL)
  - Kripton ion with a fluence of 3.04E8 (particles)
  - Average flux 1E4 (particles/sec)
  - RISC working frequency of 20MHz on ProASIC3 A3P250

RISC processor version	SEE Cross-section [MeV cm²/mg]
Unhardened	1.45E-9
Full TMR + GG	6.37E-10
Our Approach	3.12E-12

SET: in conclusion…

- SETA tools are available
  - Effective analysis of SET propagation
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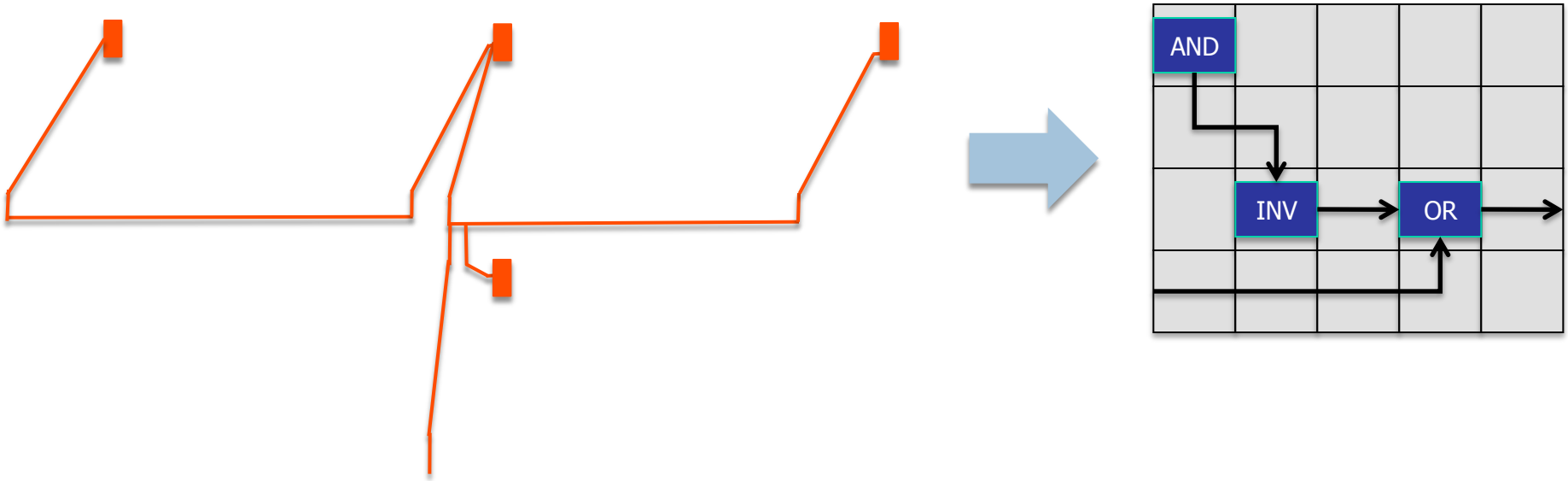
V **Propagation through gates**
V **Propagation through routing**
V **SET classification on FFs or IOs**

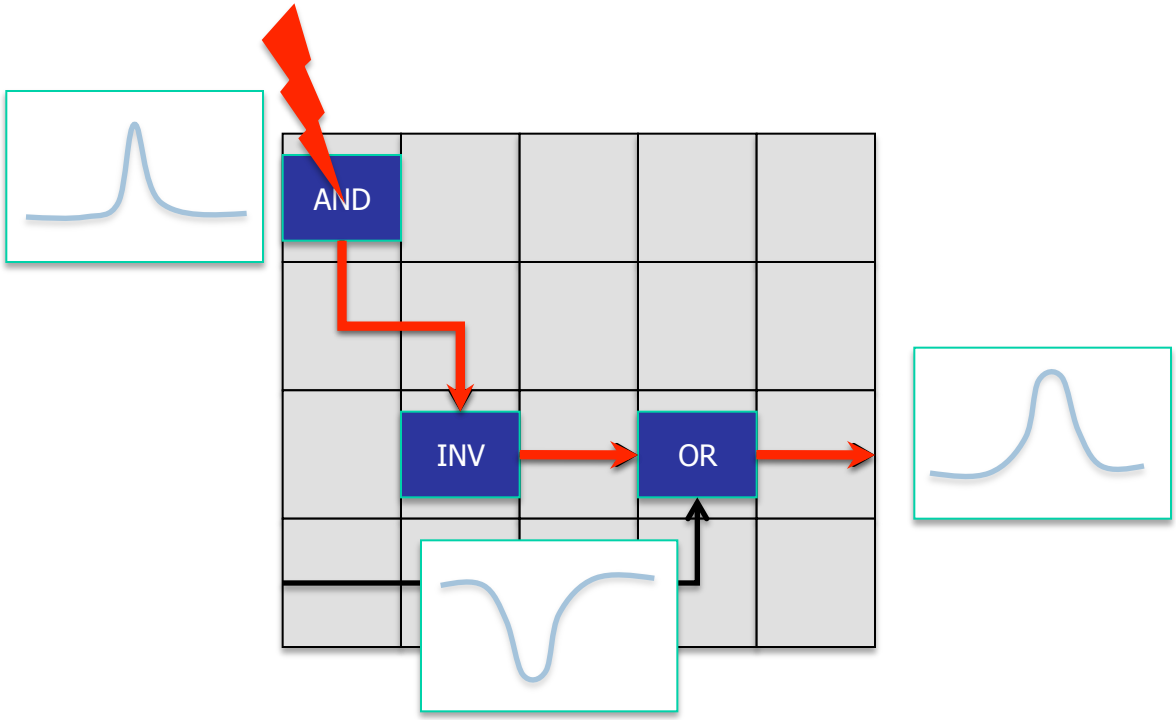
Physical Design Description

- The circuit is modeled as a graph
  - Cell functionality
  - Routing model



SET generation phenomena

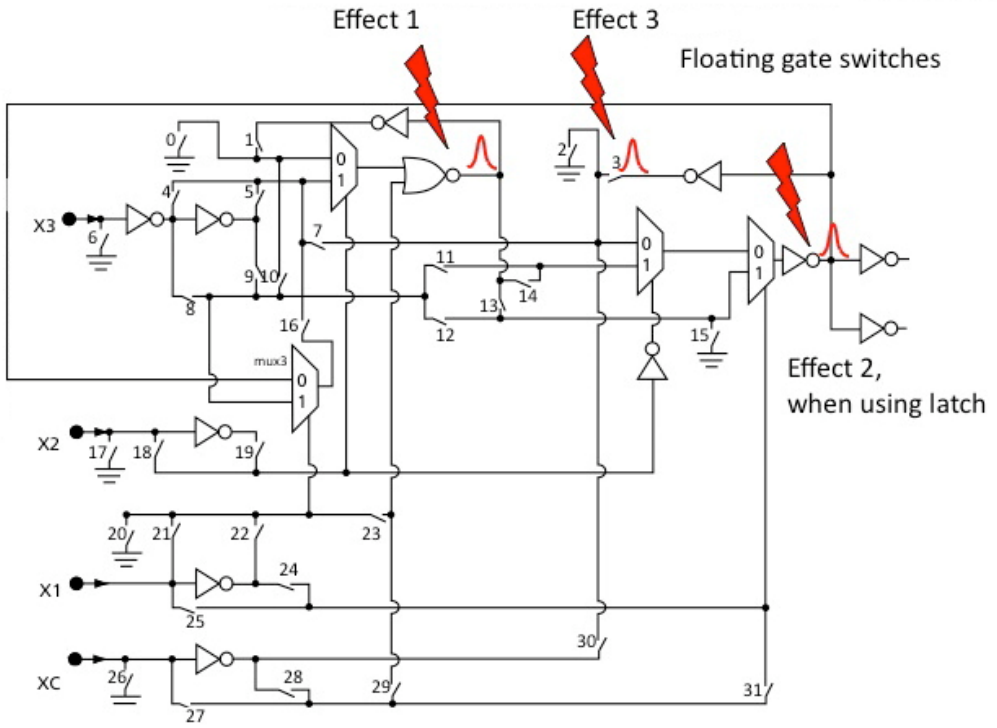
- Particle hitting a sensitive node
  - **Generate a SET pulse**
  - Propagates through the logic



SET generation phenomena

- SET generation is related to
  - Linear Energy Transfer (LET)
  - VersaTile architecture
  - Technology

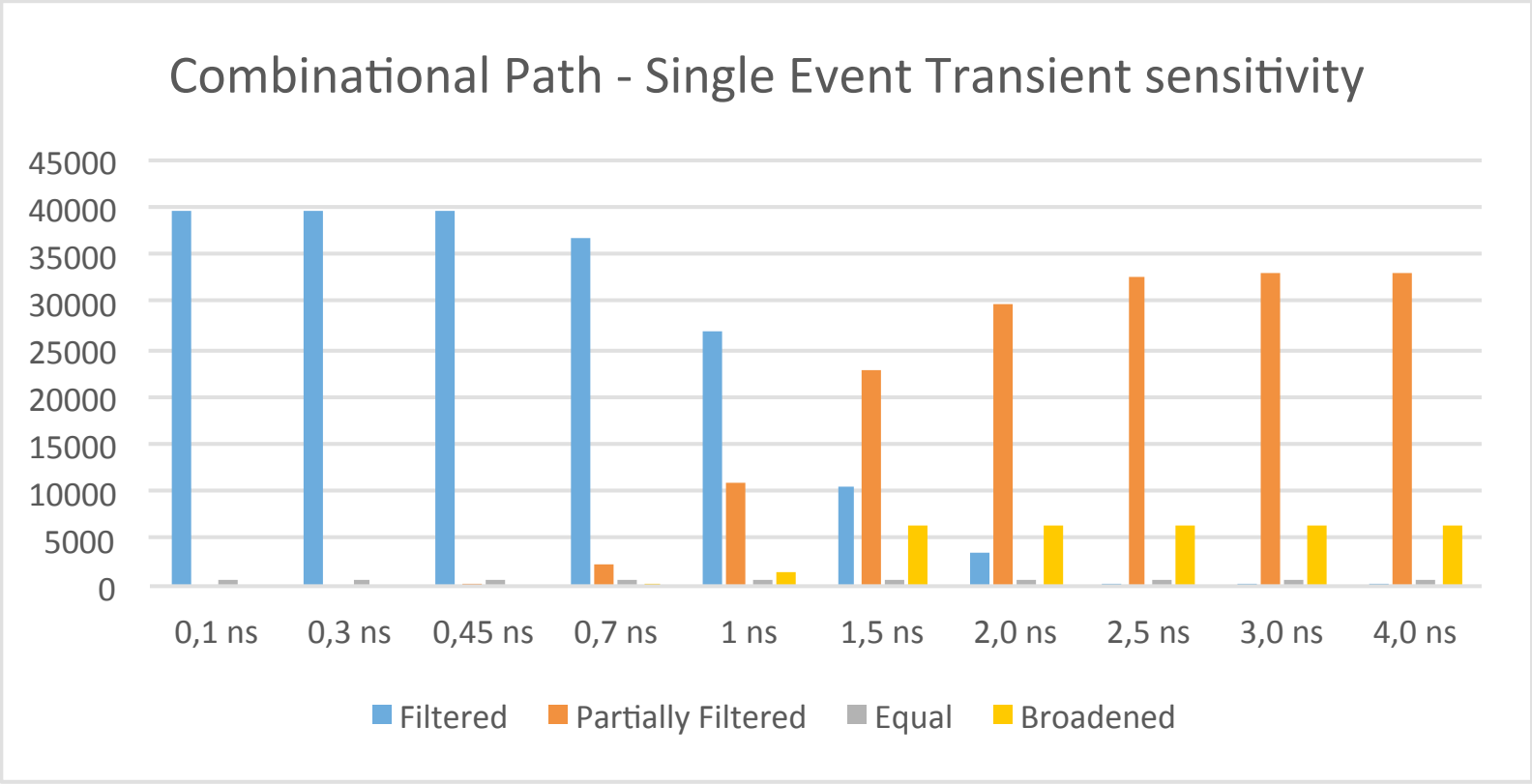
[Azimi, Du, Sterpone, Micro Rel, 2015]
[Azimi and Sterpone, IEEE DDECS 2016]



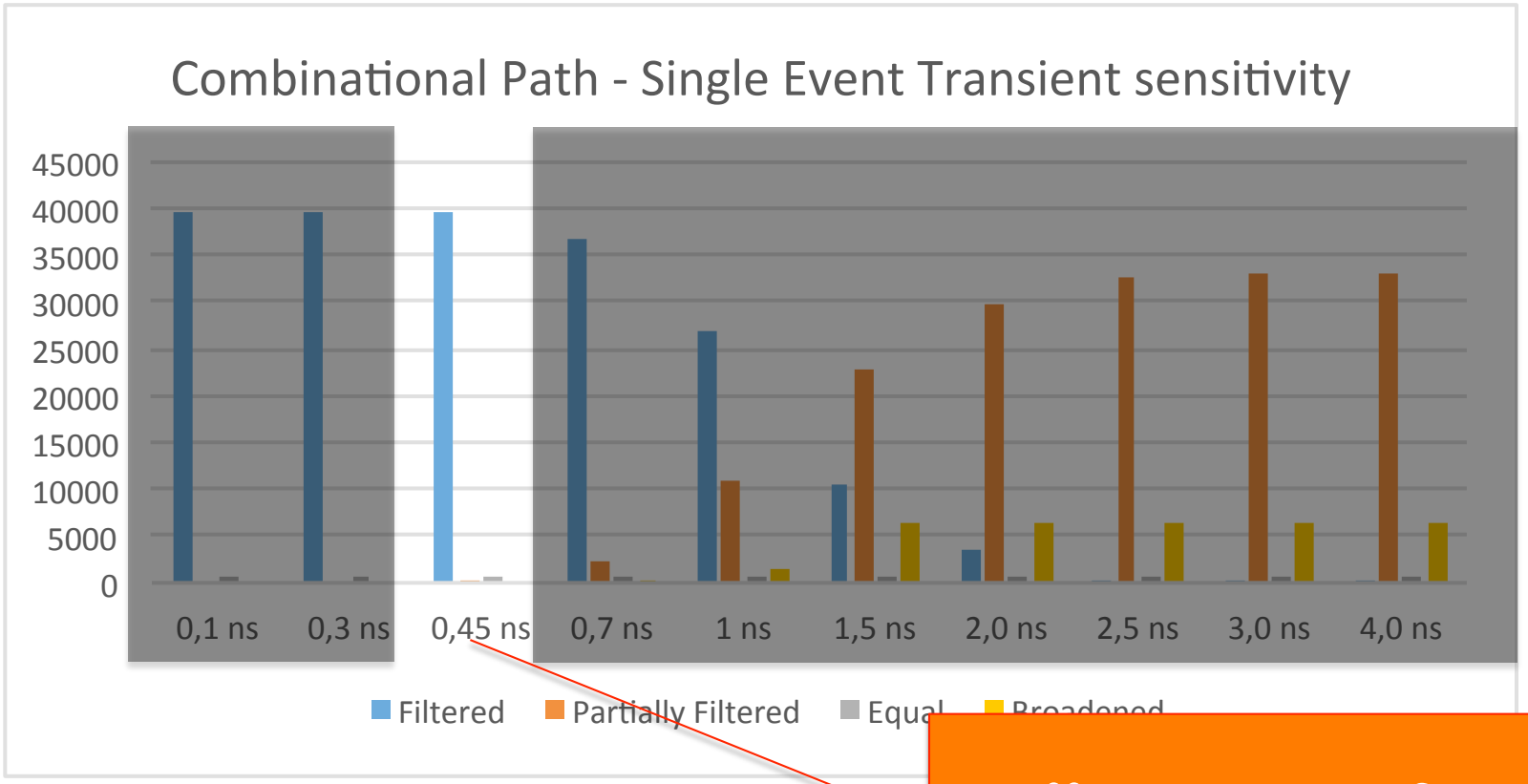
Why SET generation ?

- The type of source SET is mandatory to understand the exact type of propagation
  - Mitigation GG insertion is related to SET length
- It is necessary to establish the absolute SET count
  - Calculation of the realistic IOs/FFs error rate for the whole space mission duration

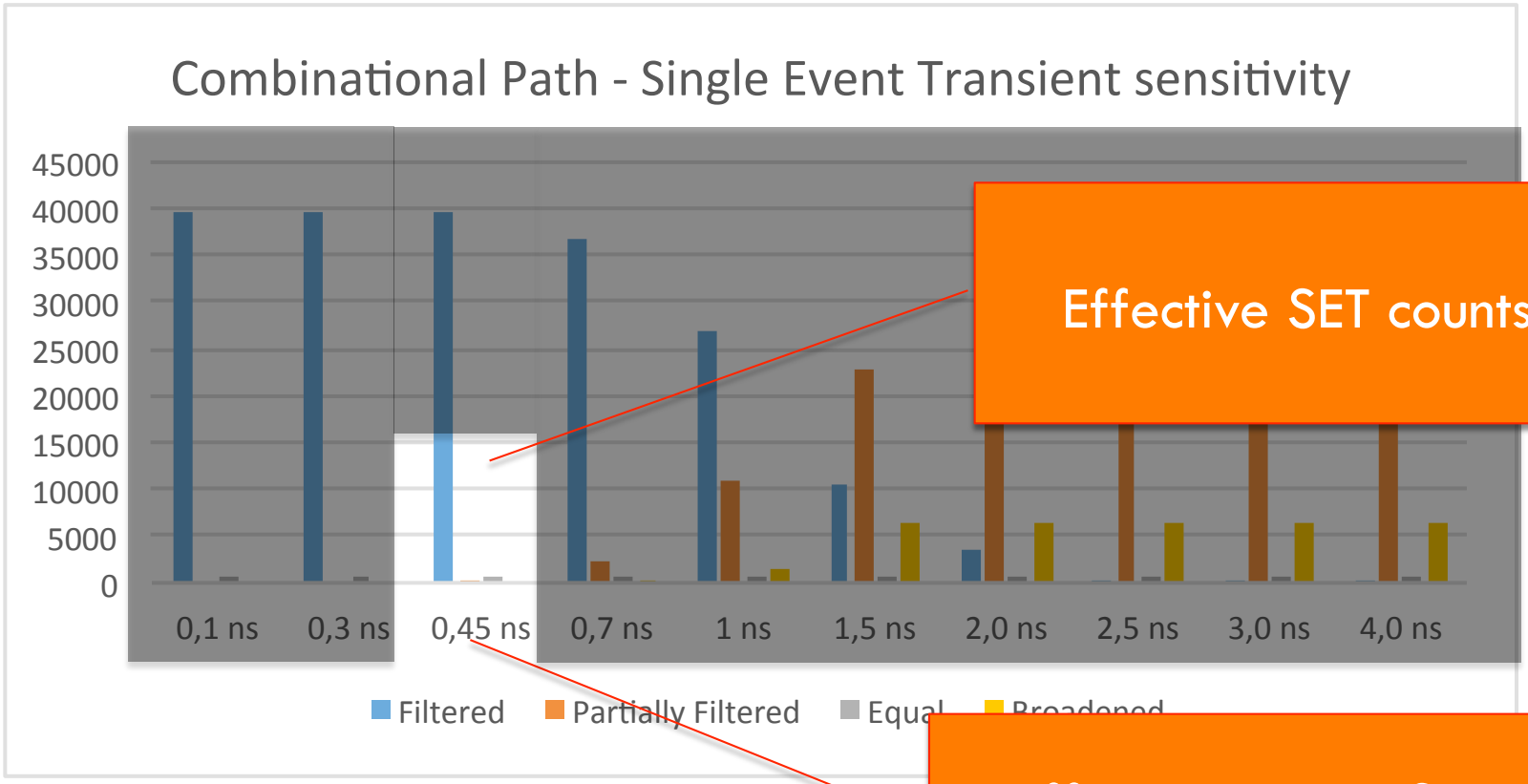
Why SET generation ?



Identification of source SET length



Identification of effective SET counts



Thank you!

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