# Highly Reliable System-on-Chip using Dynamical Reconfigurable FPGAs

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# Goal



- Analysis of Single Event Upset sensitivity of SRAM-based FPGAs
  - Identification of Single Points of Failure (SPFs)
  - Error rate estimation
- Mitigation

# Outline



- Introduction: SEU scenario
- Verification and Error Rate Integrated tool (VERI-Place)
  - Configuration memory Database
  - Execution flow
  - Results and Classification
- Experimental results
  - Radiation test and Fault Injection
- Conclusions and future works

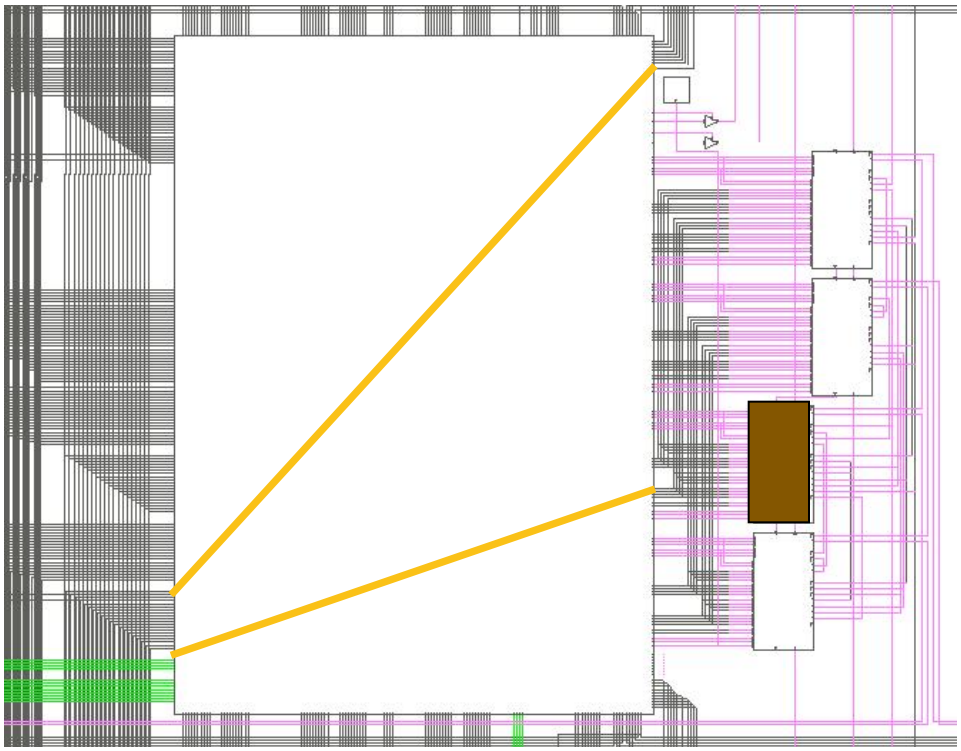
# SEU scenario



- The bitstream

| | | | | | |
|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 |

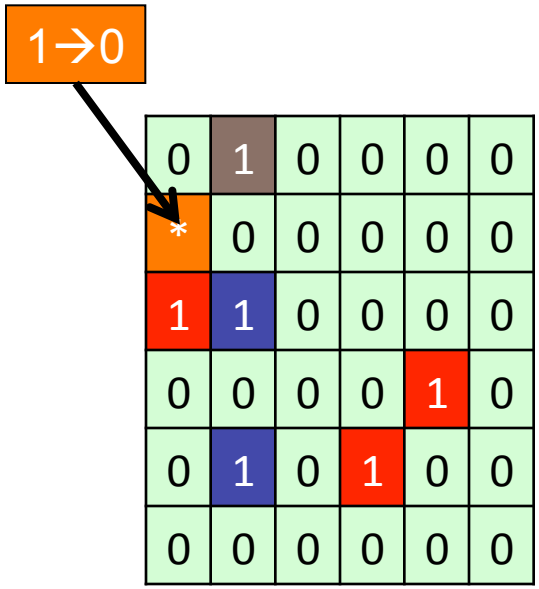
- The original netlist



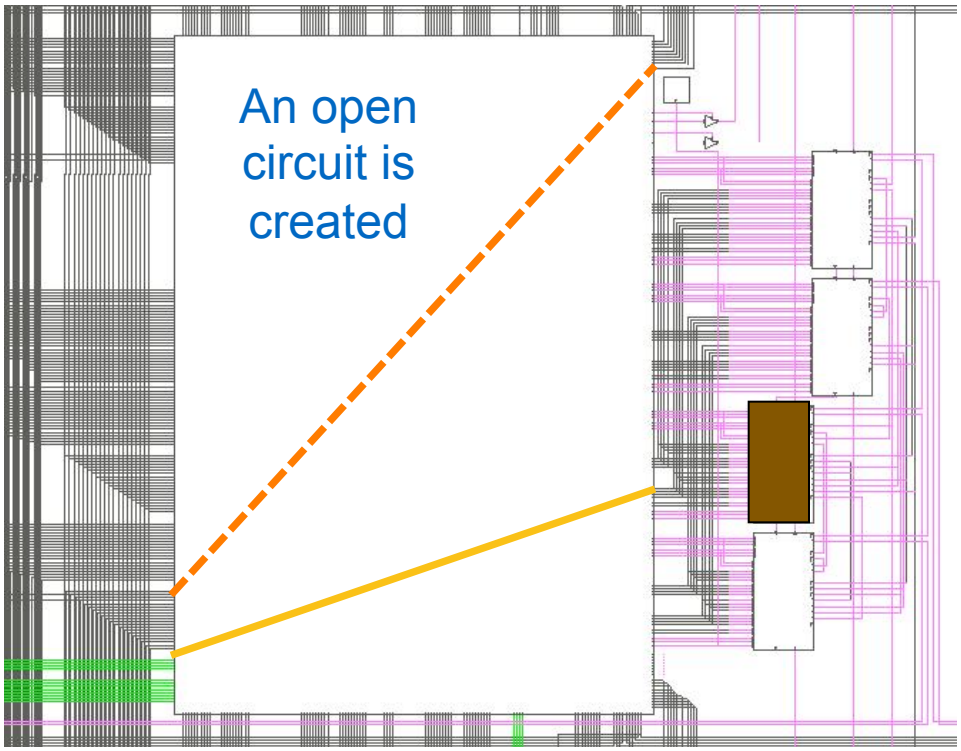
# SEU scenario



- The bitstream



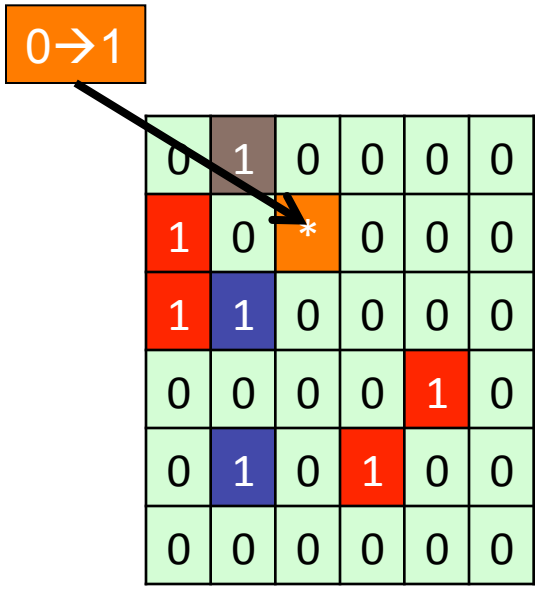

- The corrupted netlist



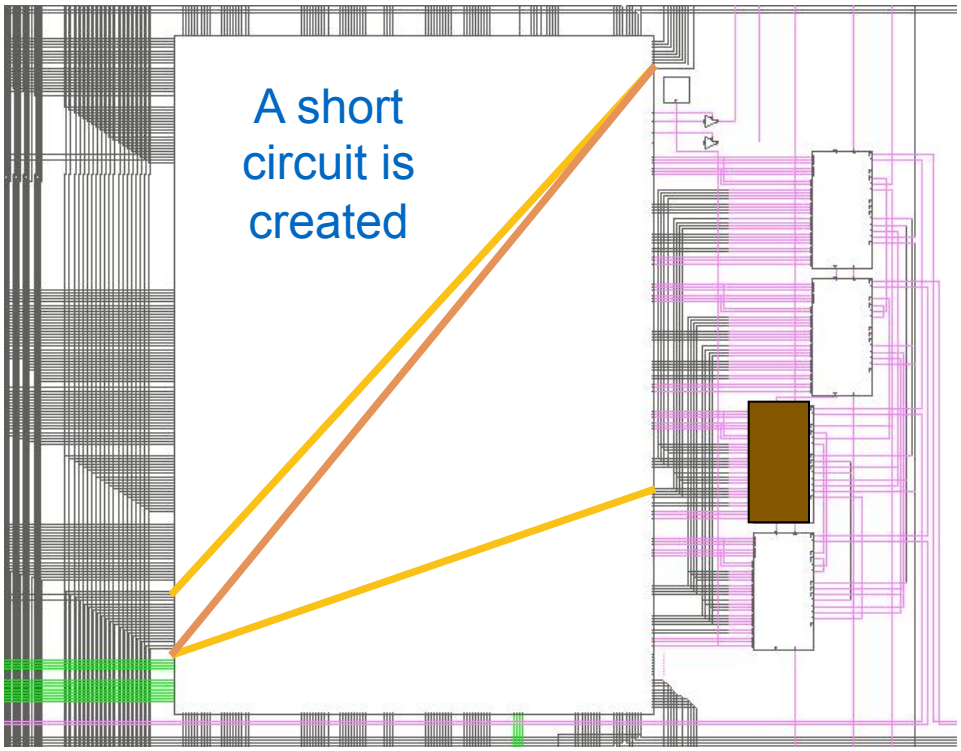
# SEU scenario



- The bitstream



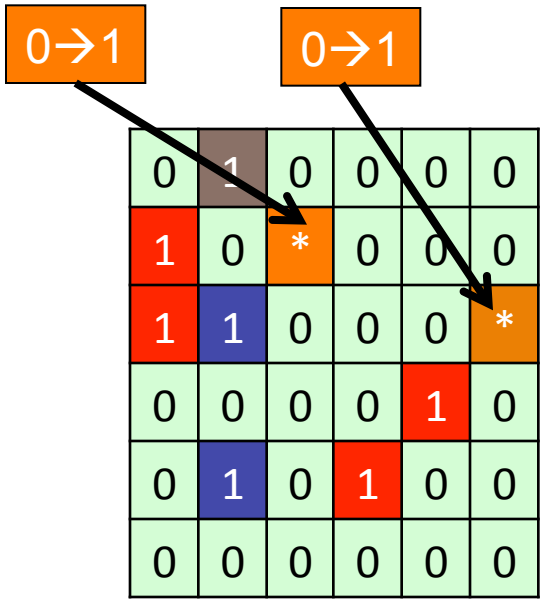

- The corrupted netlist



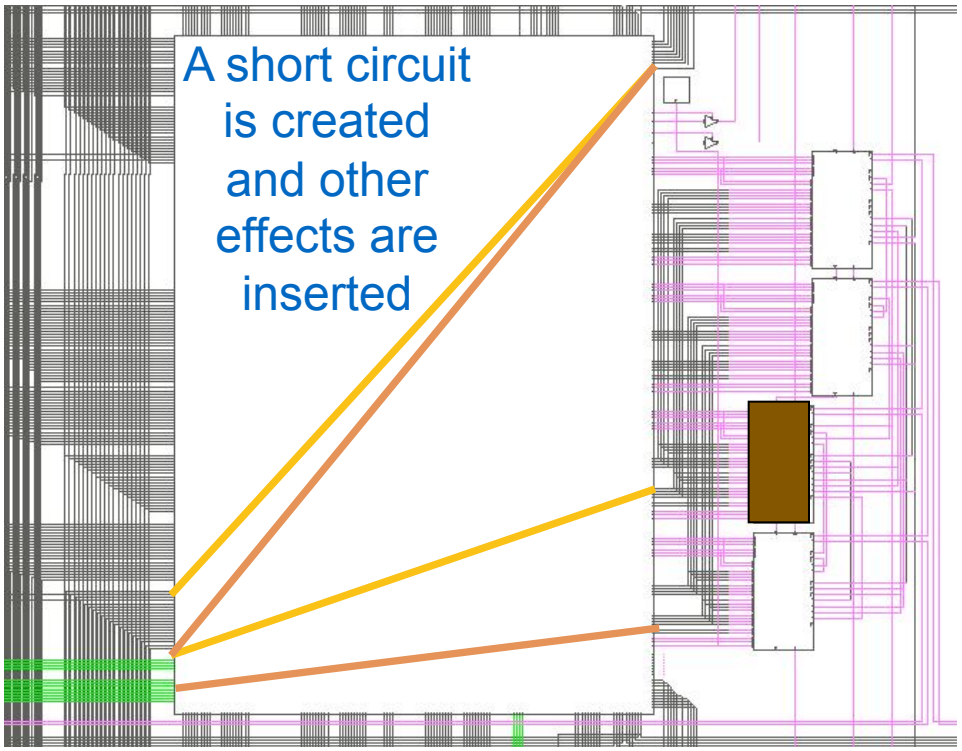
# SEU scenario: accumulation of 2-bit



- The bitstream



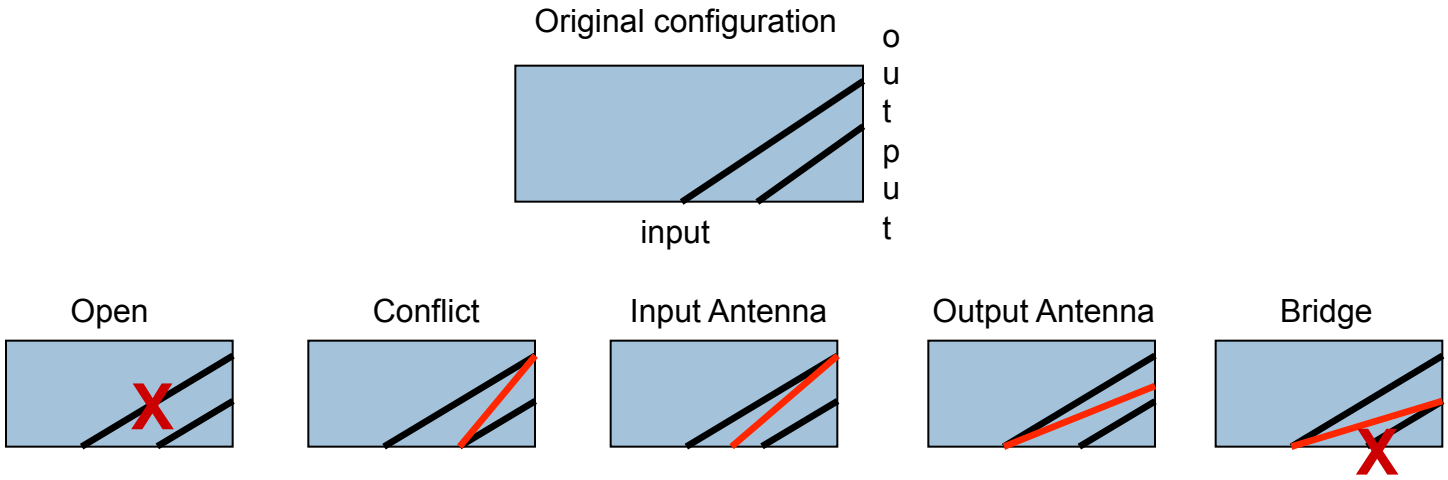

- The corrupted netlist



# SEU scenario



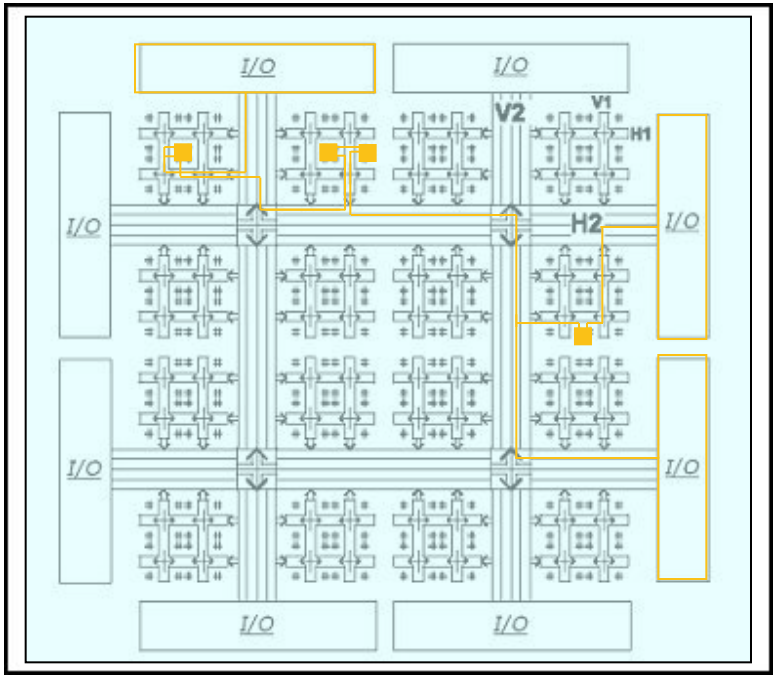
- SEU within the configuration memory
  - FPGA resource not affected : **NO ERROR**
  - FPGA resource affected : **ERROR**
- SEU induced architectural modification
  - **Logic Element:** **LUT, MUX, FF Config**
  - **Interconnections:** **Switchbox**



# SEU scenario



| | | | | | |
|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 |




FPGA configuration memory

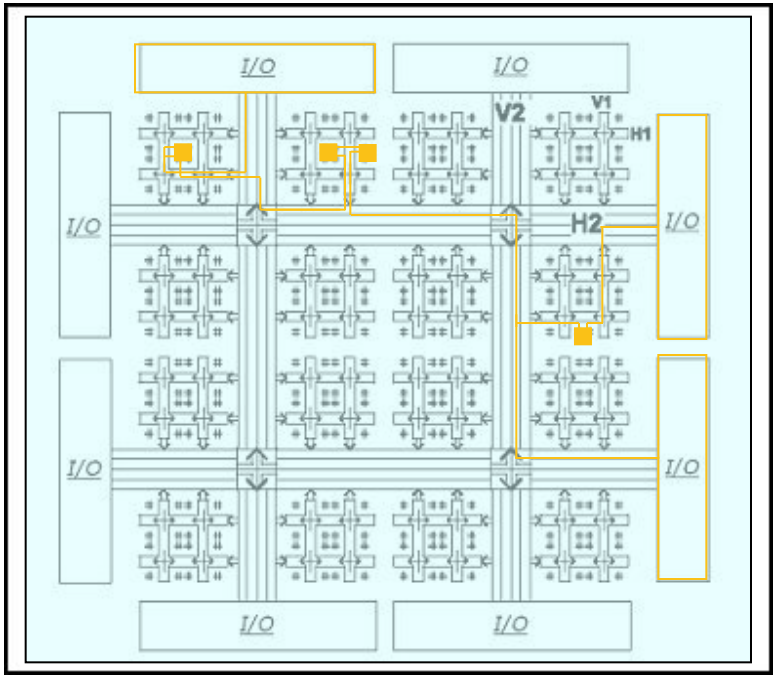
FPGA array

Execution time

# SEU scenario



| | | | | | |
|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 |



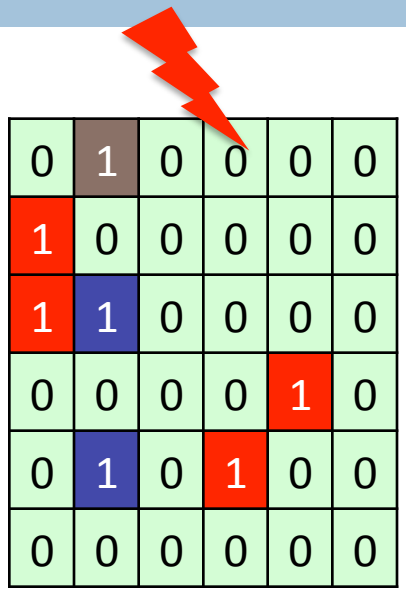

FPGA configuration memory

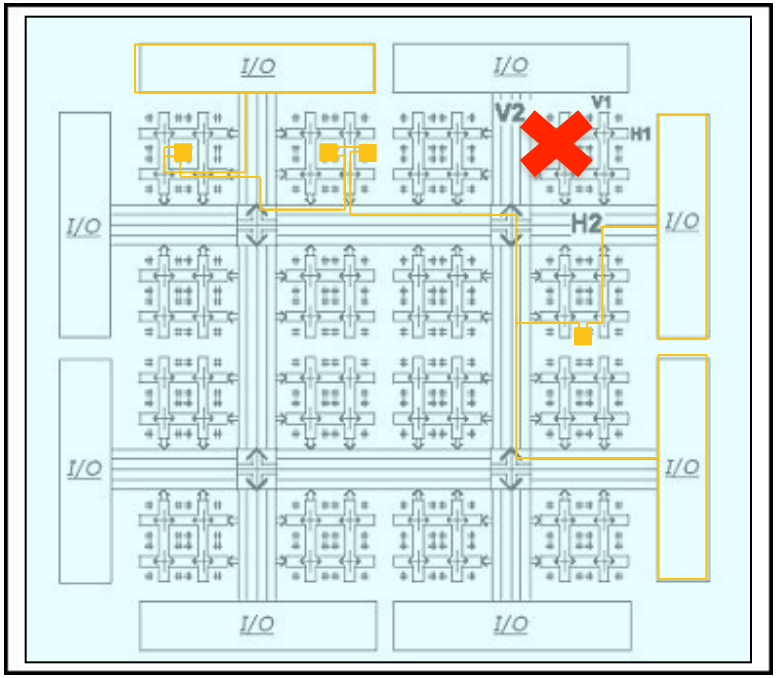
FPGA array

Execution time

# SEU scenario






FPGA configuration memory

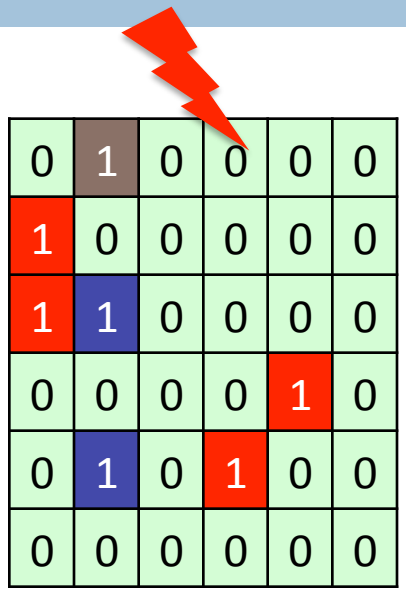
FPGA array

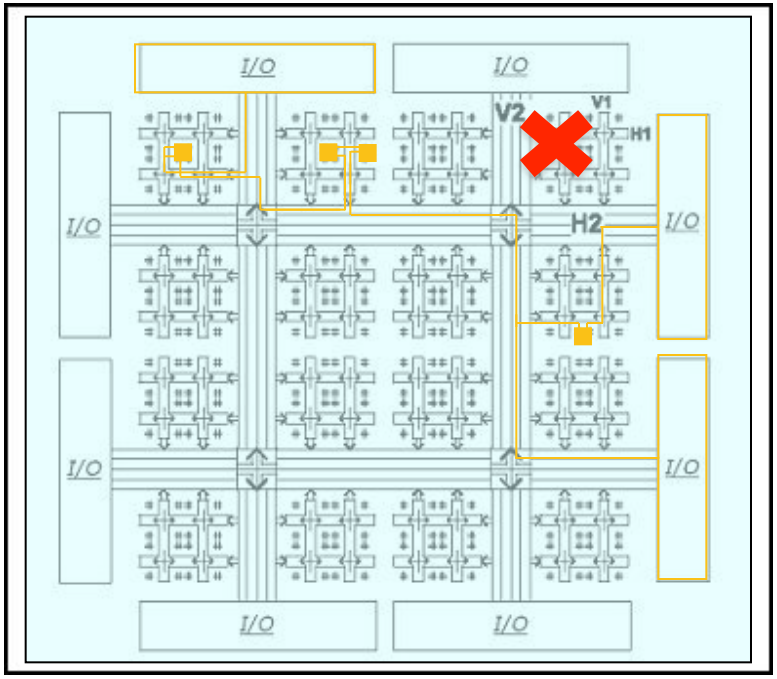
Execution time

SEU effect

# SEU scenario






FPGA configuration memory

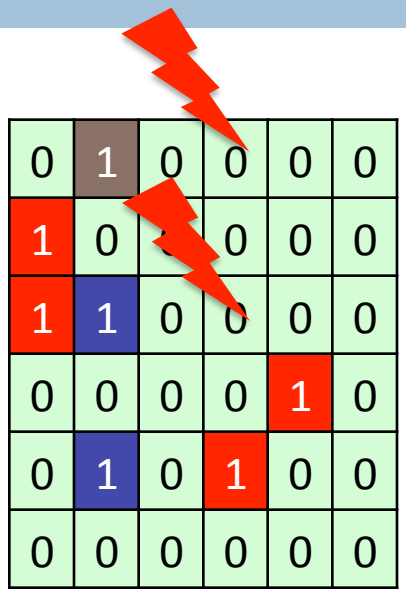
FPGA array

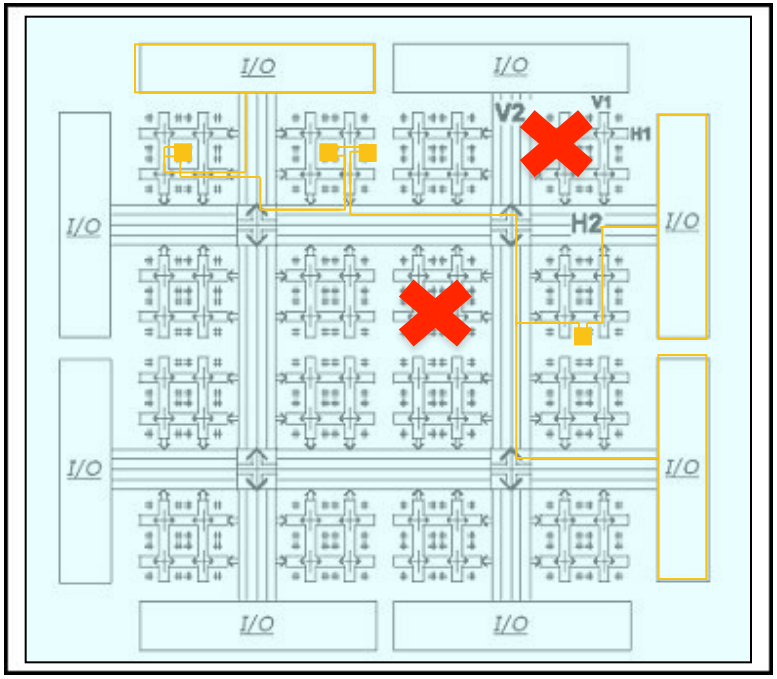
Execution time

SEU effect: No error

# SEU scenario






FPGA configuration memory

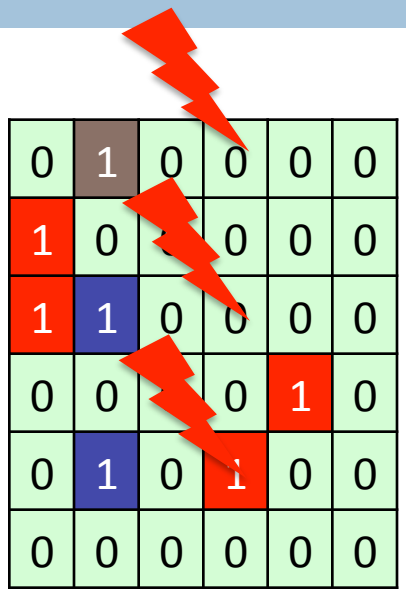
FPGA array

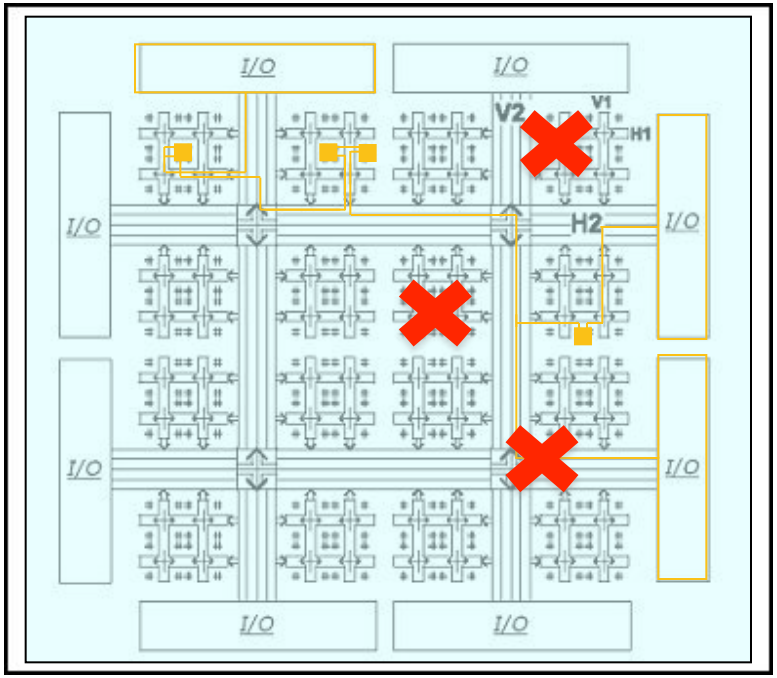
Execution time

SEU effect: No error

# SEU scenario






FPGA configuration memory

FPGA array

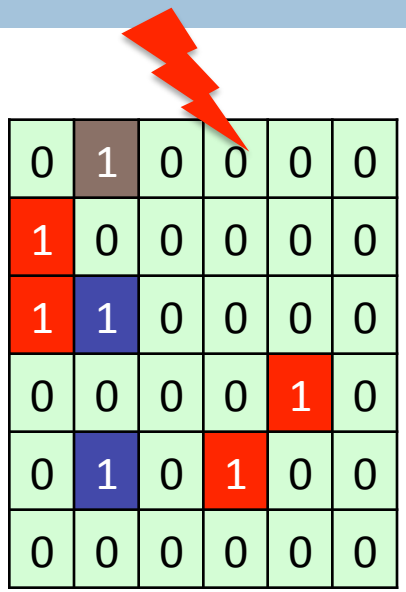
Execution time

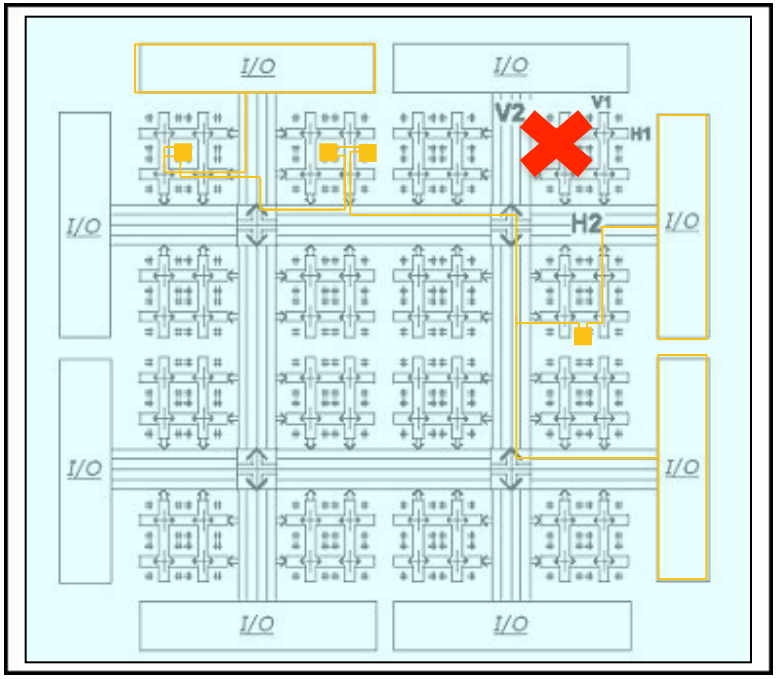
SEU effect: No error

**SEU effect: Error**

# SEU scenario with scrubbing






FPGA configuration memory

FPGA array

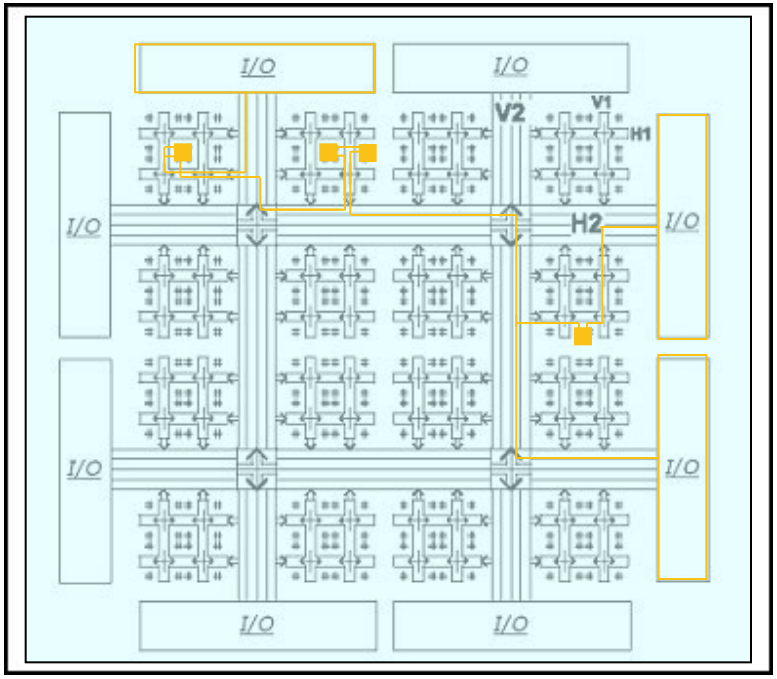
Execution time

SEU effect

# SEU scenario with scrubbing



| | | | | | |
|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 |




FPGA configuration memory

FPGA array

Execution time

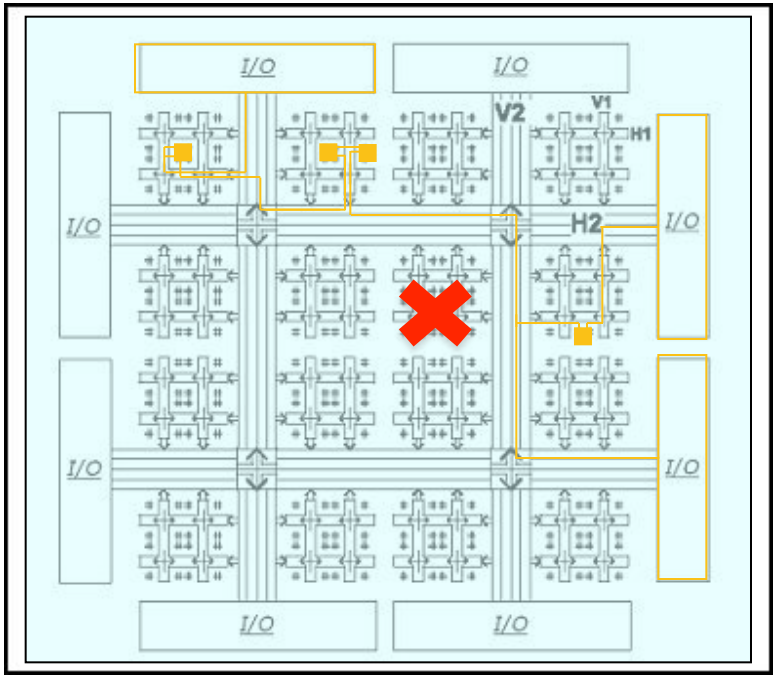
SEU effect

Scrub cycle

# SEU scenario with scrubbing



| | | | | | |
|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 |




FPGA configuration memory

FPGA array

Execution time

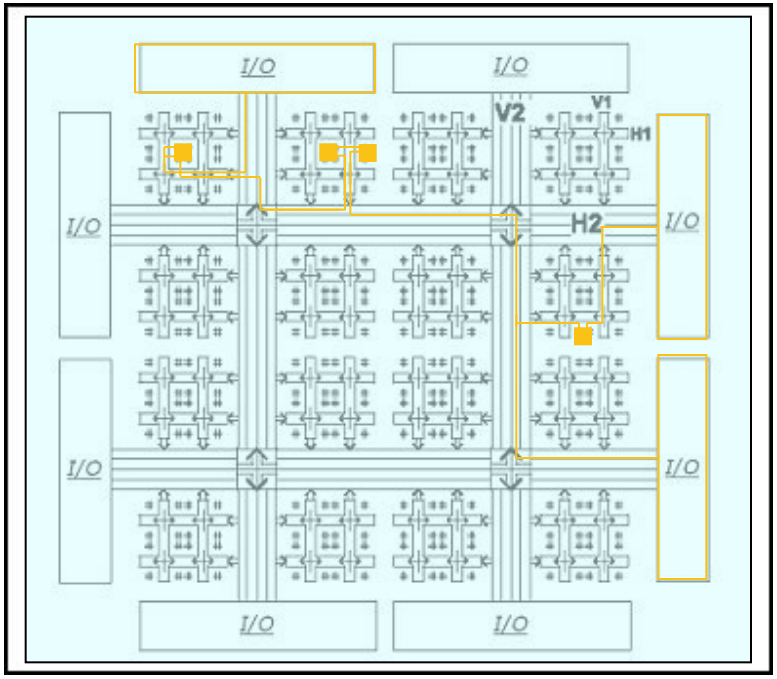
SEU effect

Scrub cycle

# SEU scenario with scrubbing



| | | | | | |
|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 |




FPGA configuration memory

FPGA array

Execution time

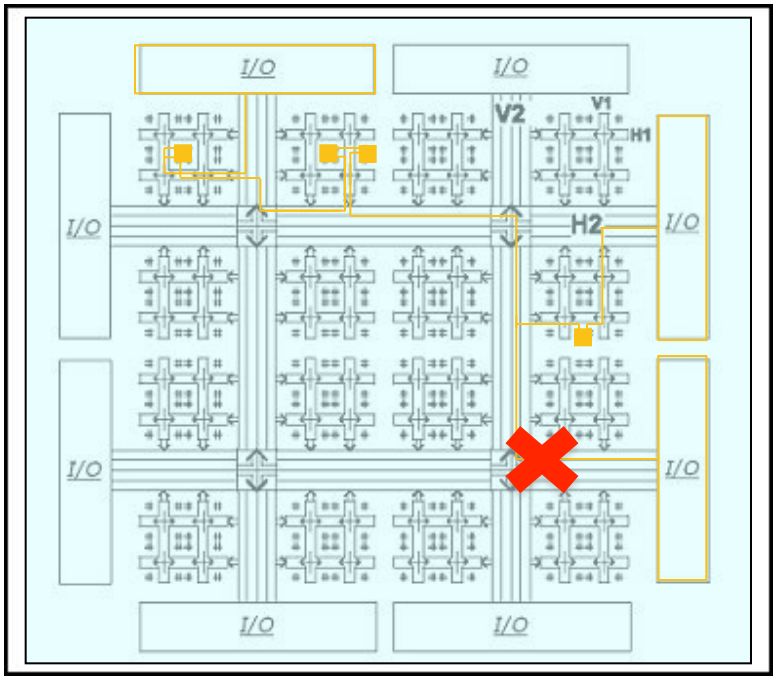
SEU effect

Scrub cycle

# SEU scenario with scrubbing



| | | | | | |
|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 |




FPGA configuration memory

FPGA array

Execution time

SEU effect

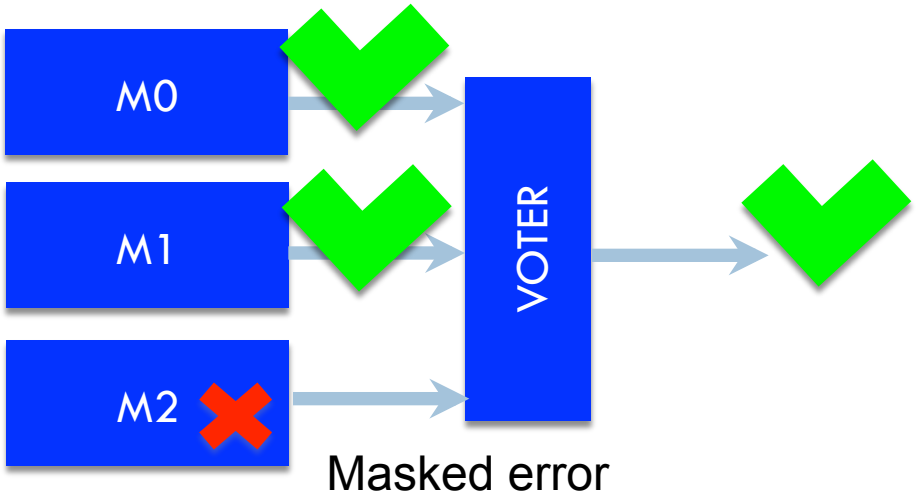
Scrub cycle

**SEU effect: Error**

# SEU scenario



**TMR**

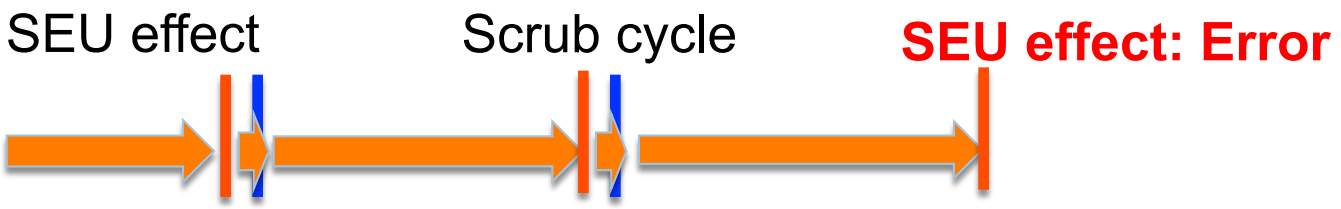



- The application of Netlist-based TMR and scrubbing is an effective solution
  - Drawbacks: power consumption and functional availability

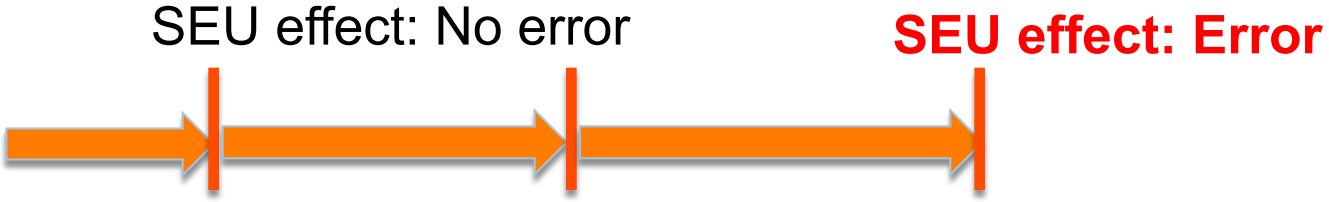
# SEU scenario



**with scrubbing**

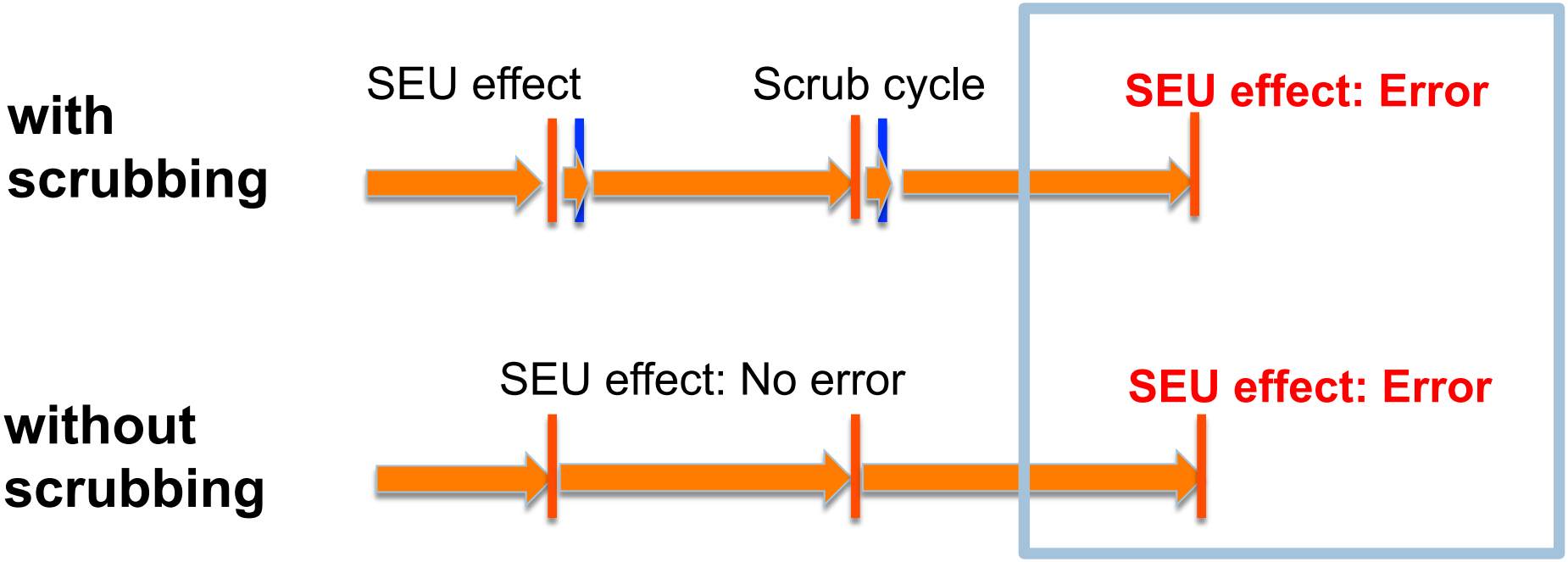



**without scrubbing**



# SEU scenario






**Errors affecting the circuit outputs happen at the same time**

- **Probability of SEU location**
- Avoid of SPFs: **TMR is a MUST**

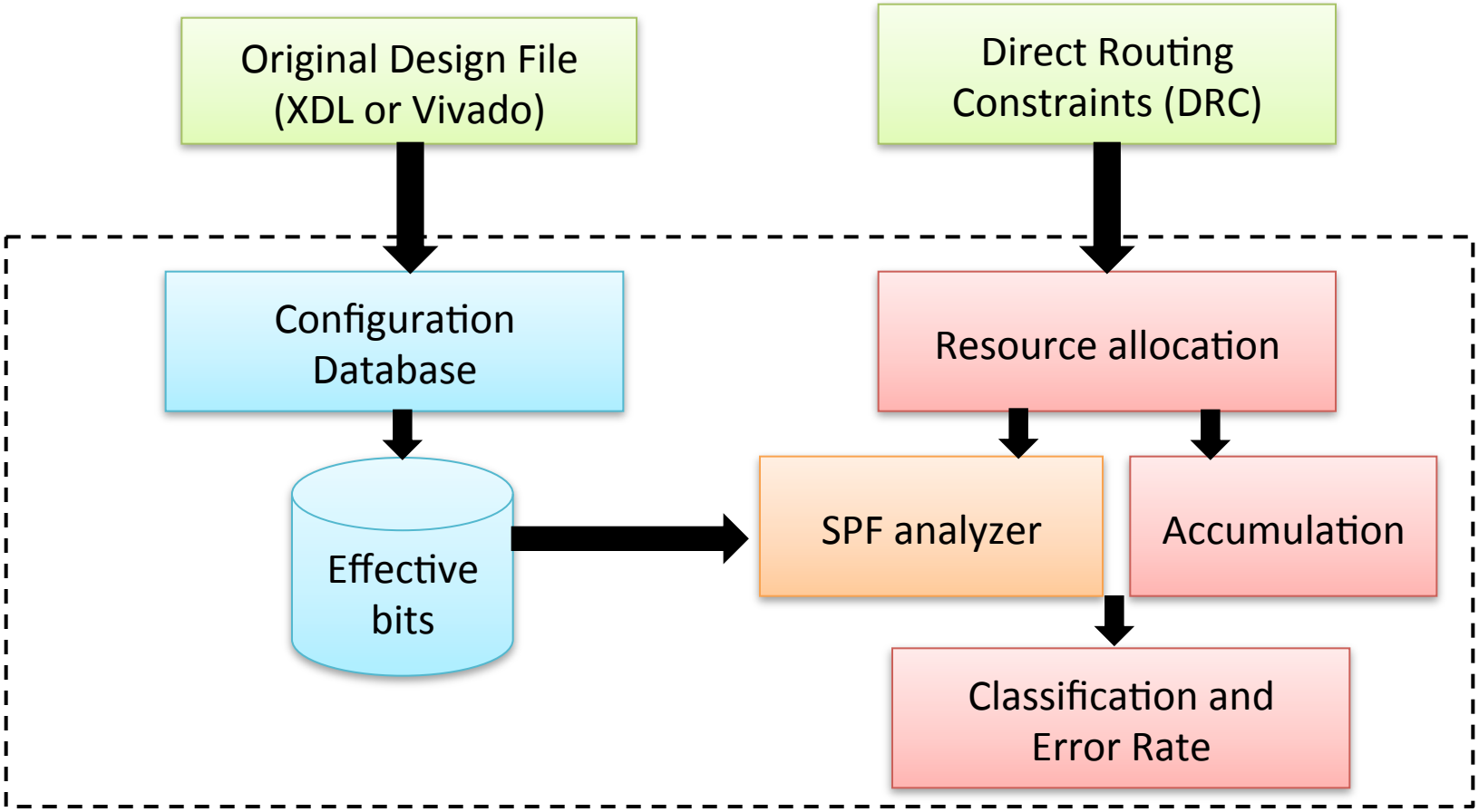
# The proposal: VERI-Place tool



- Measurement of the Application Error Probability (AEP)
  - Number of SEUs in the FPGAs configuration memory until an output error is observed
- Analysis of different design techniques
  - Fault tolerance (DWC, TMR, XTMR,…)
  - Static
  - Dynamic
  - Partial and dynamic

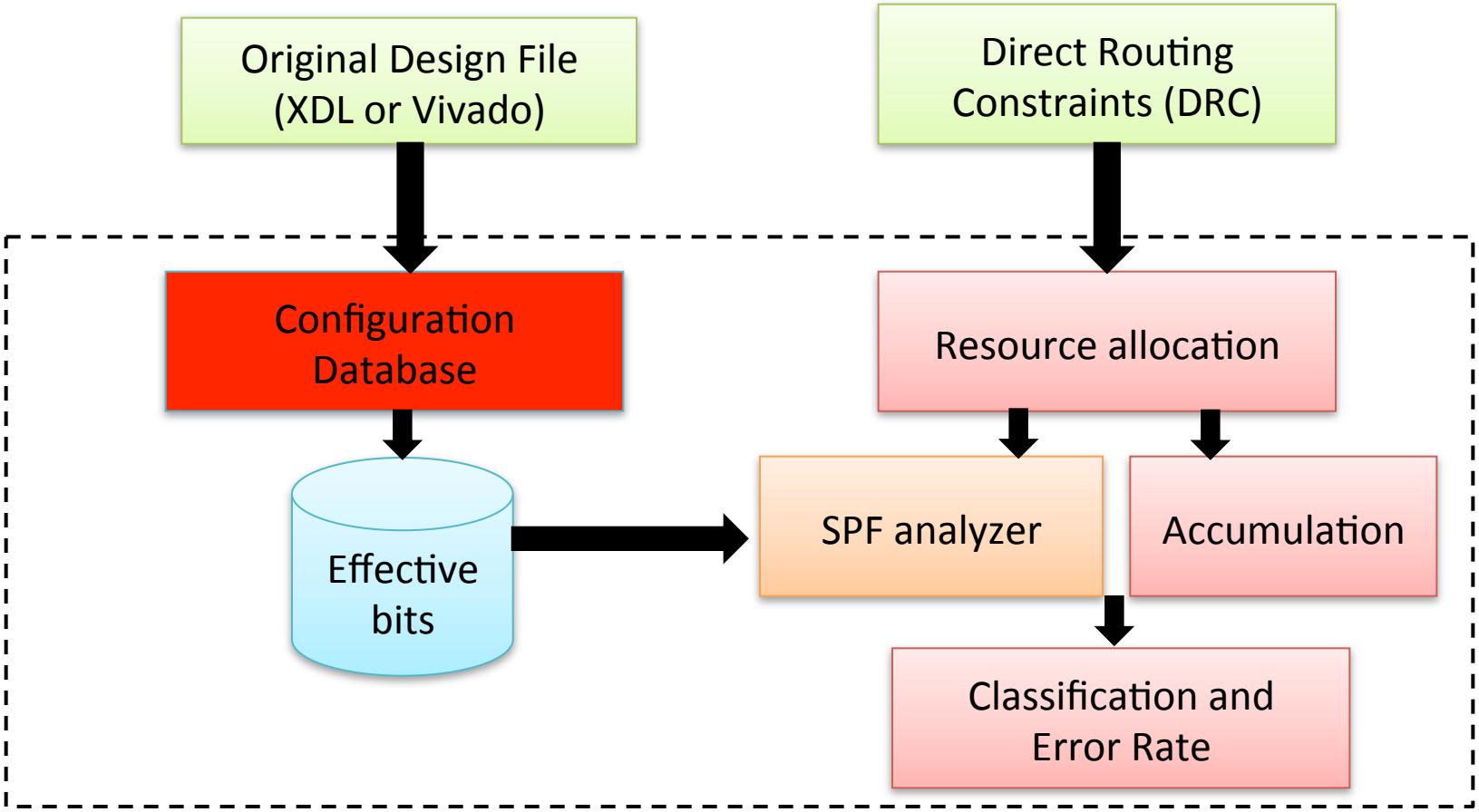
# The proposal: VERI-Place tool





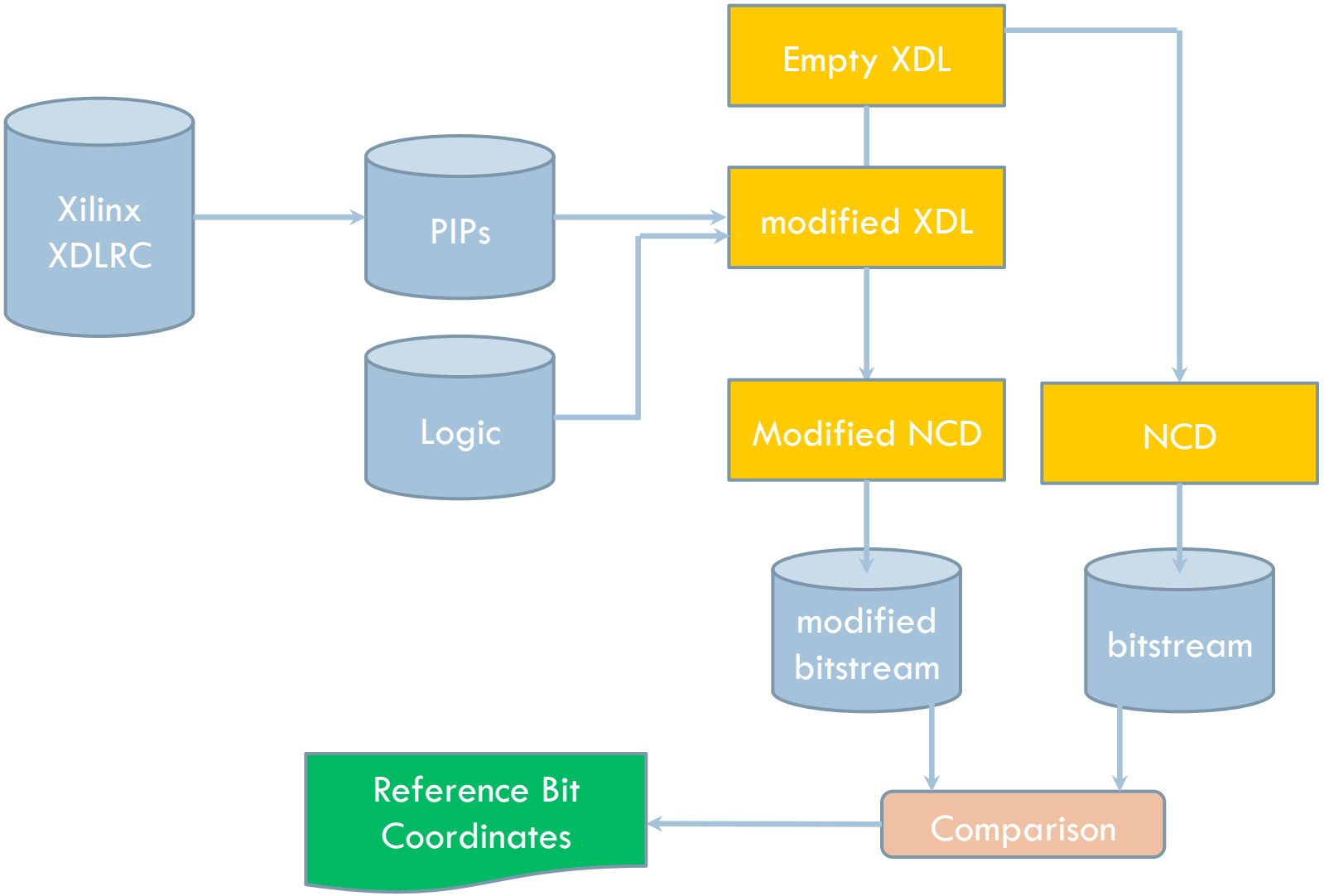
# The proposal: VERI-Place tool





# Configuration memory DB





# Configuration memory DB



| Device Name | Total PIP [#] | Effective PIP [#] |
|---|---|---|
| XC5VLX50T-FF1136 | 18,975,457 | 15,695 |
| XC7K70E-2FBG676 | 29,466,958 | 21,081 |
| XC7K325T-2FBG900 | 123,919,224 | 21,081 |

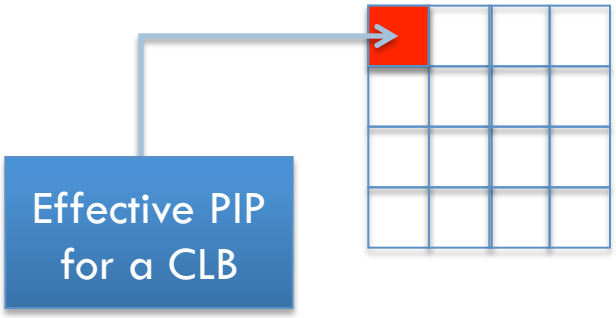
- PIPs of the whole FPGA architecture
- PIPs replica are on different CLB positions
- A PIP requires about 30-35 seconds to be decoded
  - XC7K70E would require about 32 years!
- FPGA array is regular, apart from *specific* architectural PIPs
  - unique PIPs of a given FPGA device are distinguishable

# Configuration memory DB



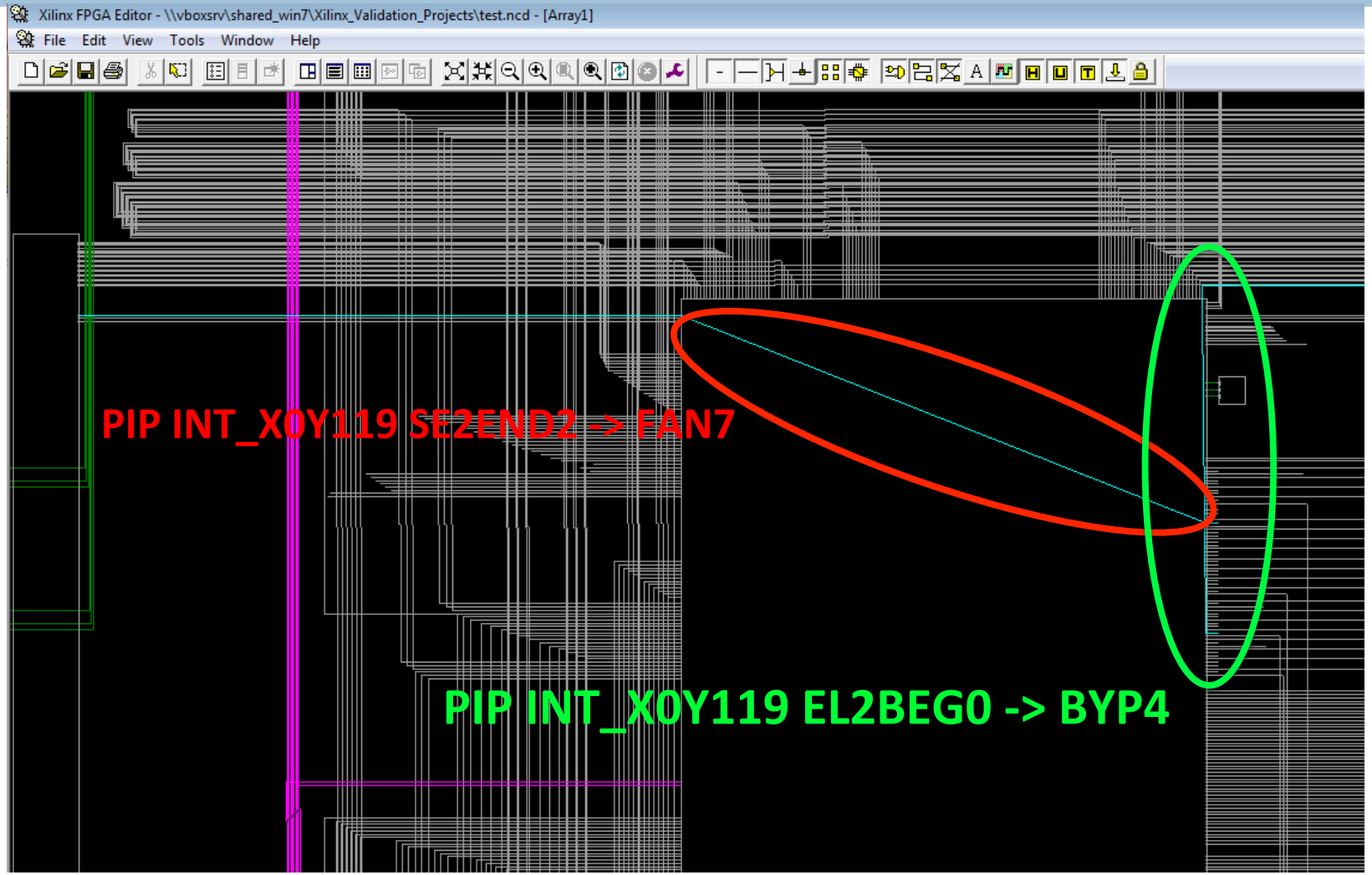
| Device Name | Effective PIPs [#] | Decoding [days] |
|---|---|---|
| XC5VLX50T-FF1136 | 15,695 | ≈6.5 |
| XC7K70E-2FBG676 | 21,081 | ≈8.6 |
| XC7K325T-2FBG900 | 21,081 | ≈12.3 |

- The decoding is performed on effective PIPs
- The whole PIP coding is generated calculating the configuration memory offset between different CLBs



# Real Coding Xilinx Virtex-5LX50T





# Real Coding Xilinx Virtex-5LX50T



- PIP INT_X0Y119 SE2END2 -> FAN7

3.693.213
3.693.214
3.693.831
3.693.835

**4 configuration memory bits.**
**In order to have the PIP these bits must be fixed at logic value ‘1’**

- PIP INT_X0Y119 EL2BEG0 -> BYP4

3.693.214
3.693.216
3.693.810
3.693.813

**4 configuration memory bits.**
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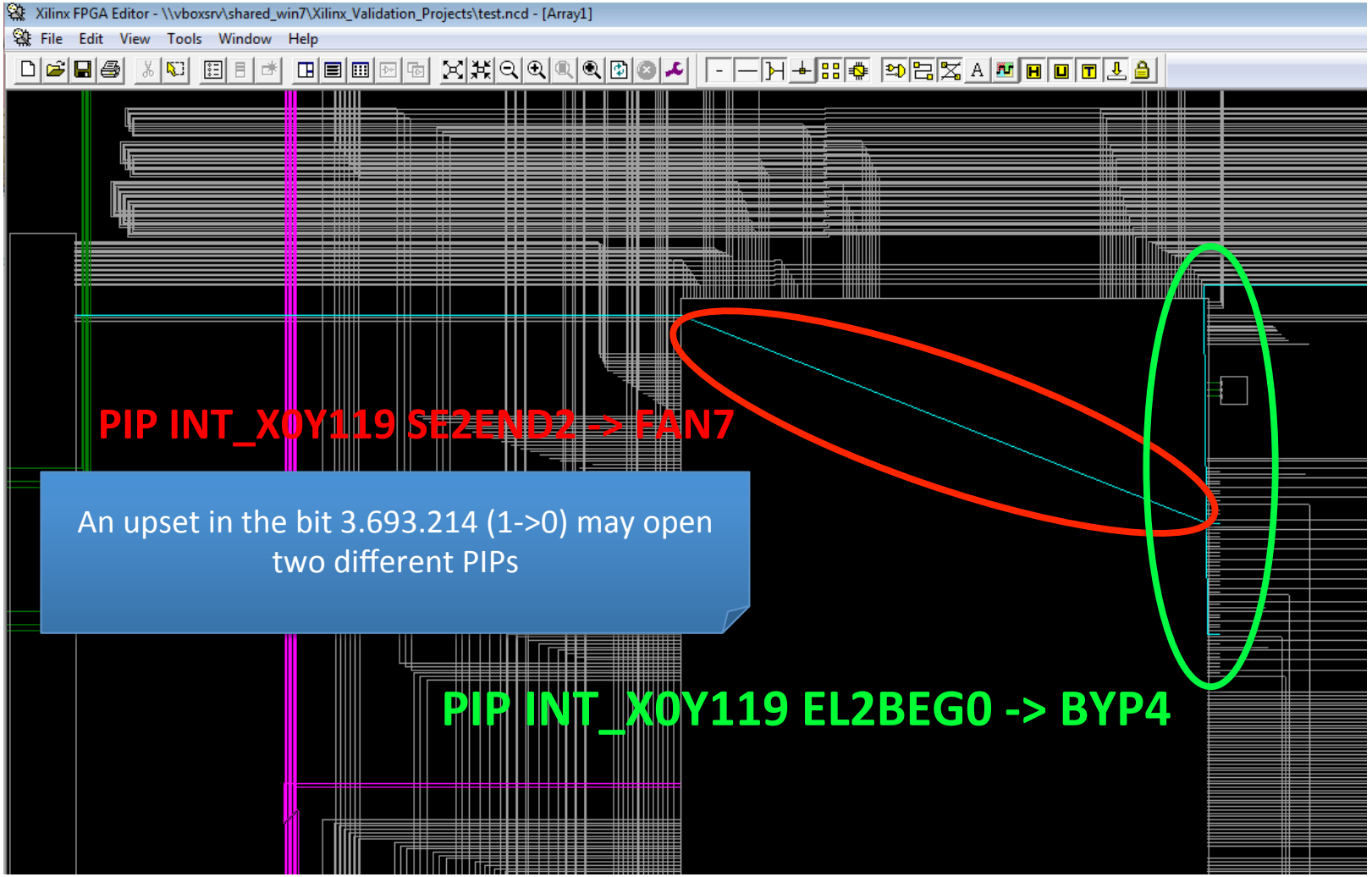
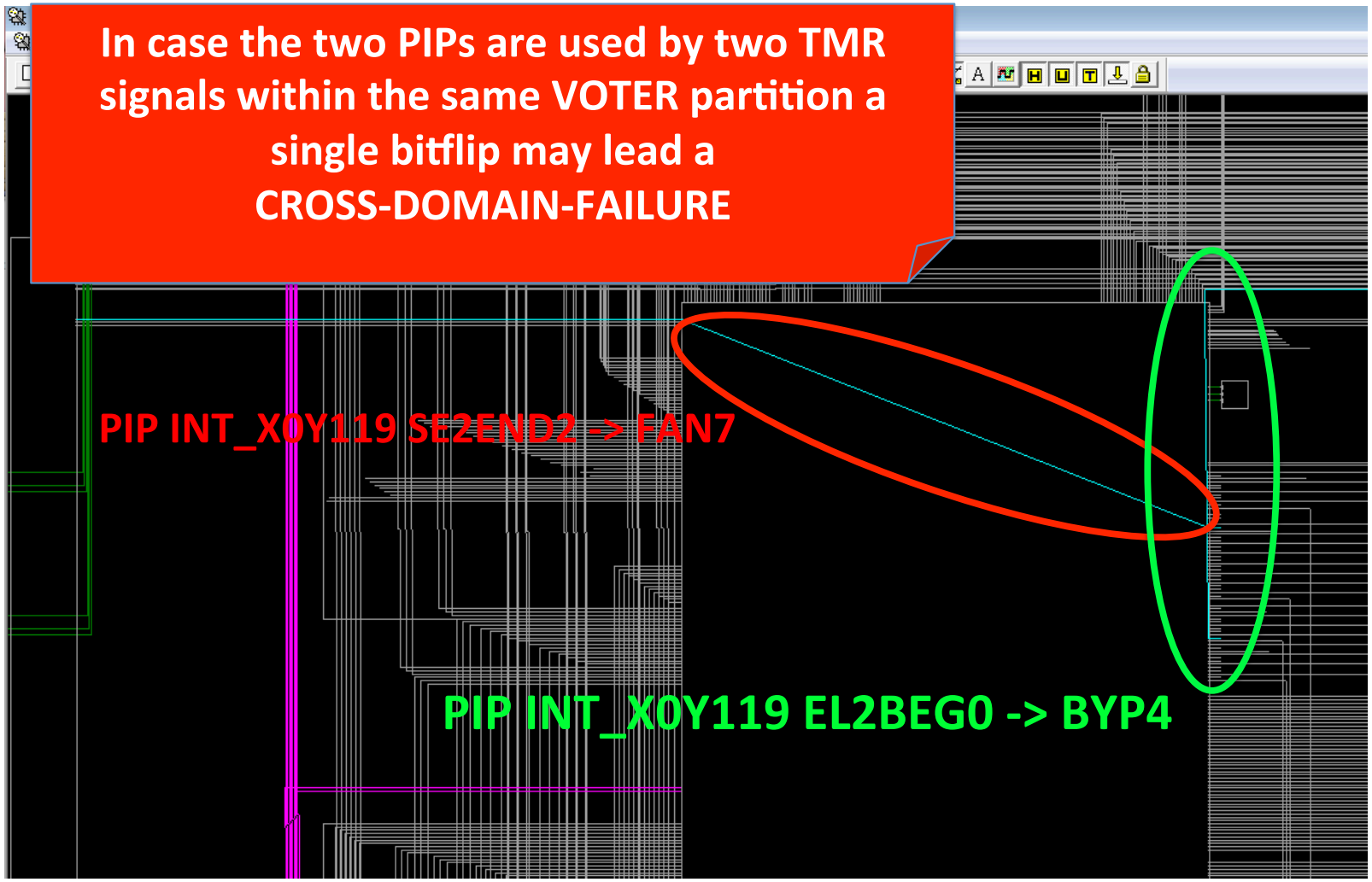


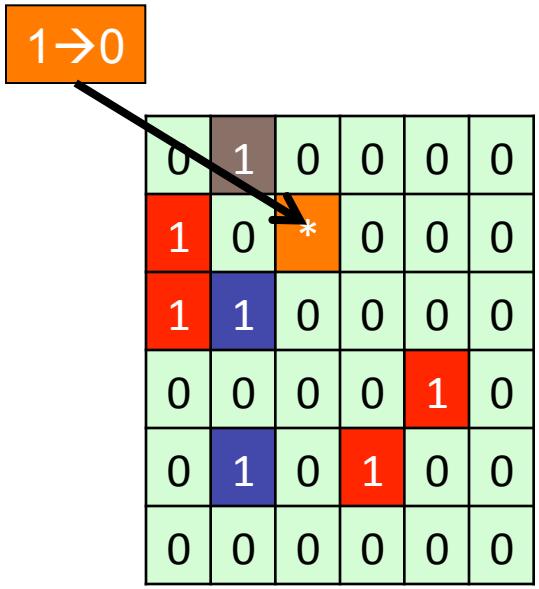
# Real Coding Xilinx Virtex-5LX50T

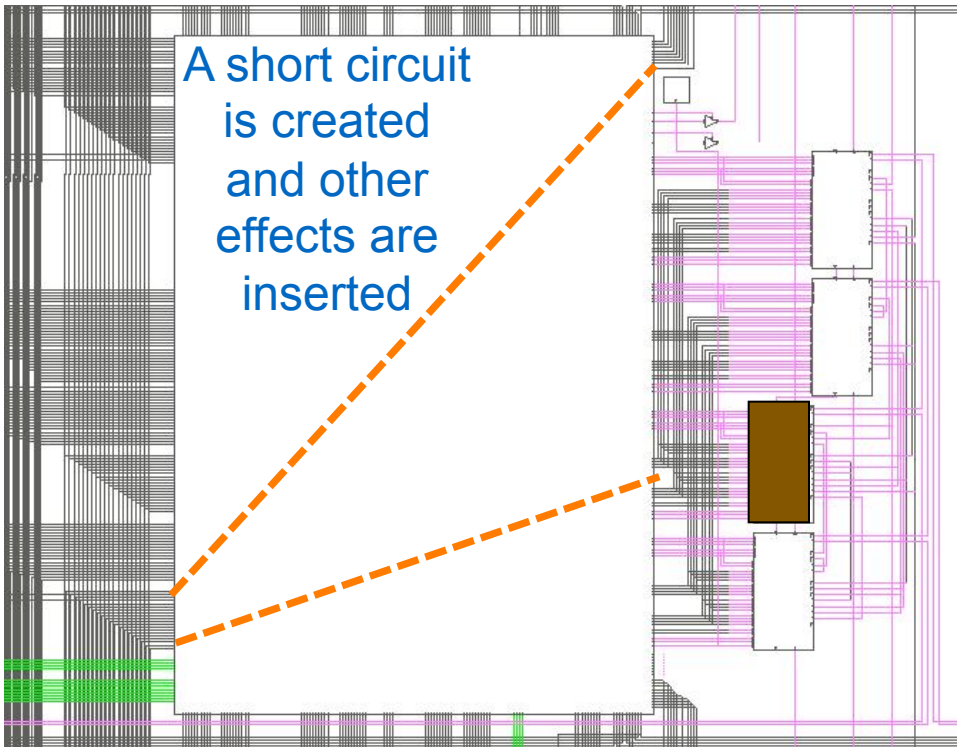




# 1-bit controlling multiple PIPs

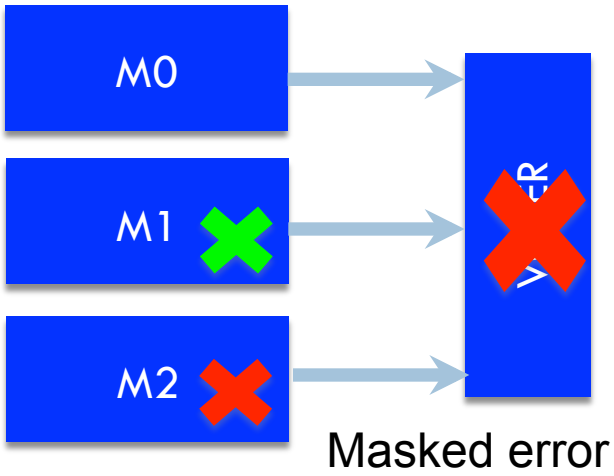


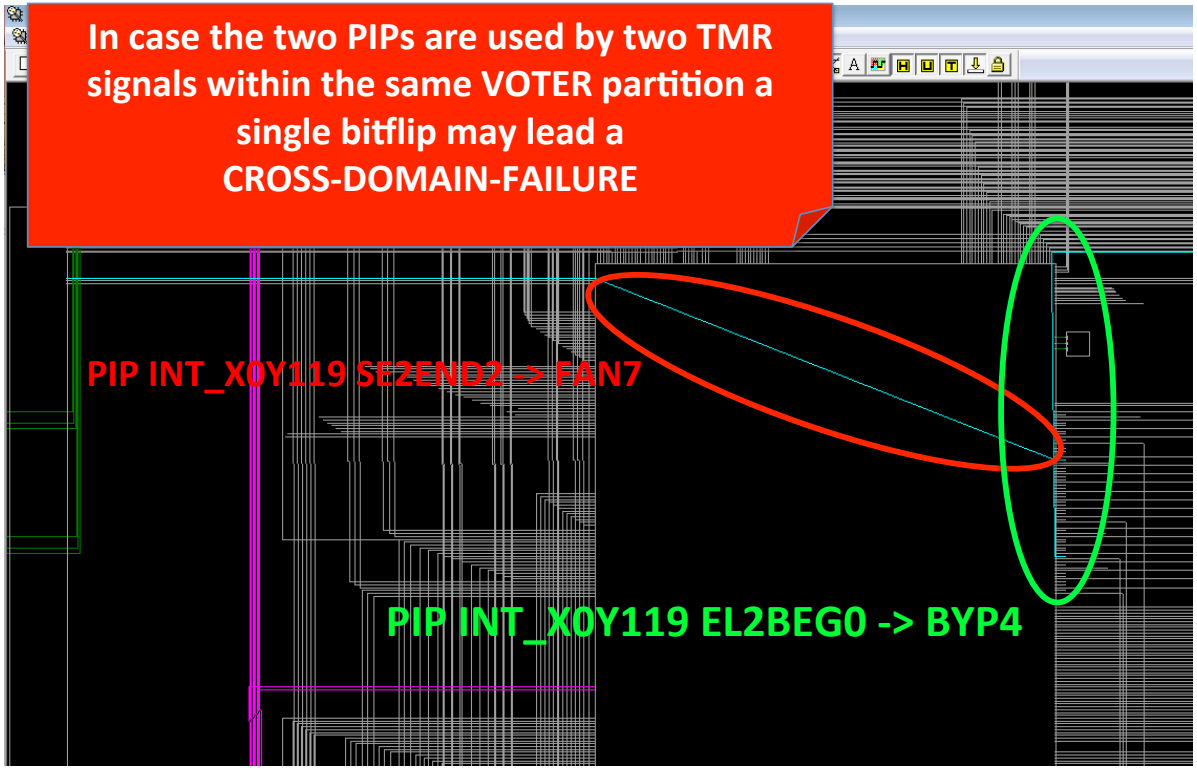


# Real Coding Xilinx Virtex-5LX50T





# Results and Classification



- Identification of all the architecturally relevant sensitive bits
  - If affected, these configuration memory bits may change the physical structure of the circuit

# Results and Classification



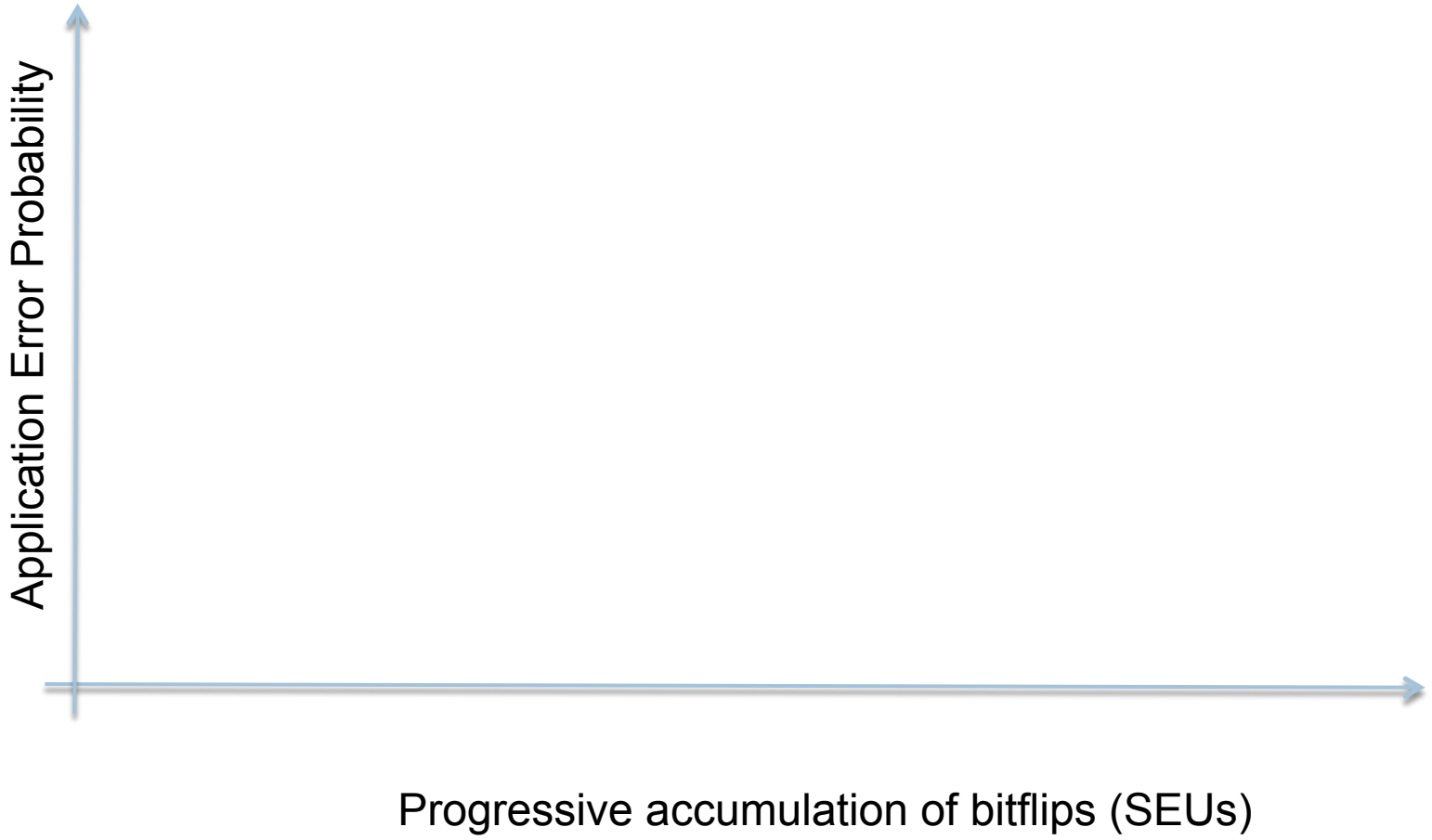
- Identification of the configuration memory bits that if affected generate a **Single Point of Failure** (SPF)

```
-- Bit Reference 13661788 Location X 60 Y 186
-- TMR Sensitive ID 1 X 60 Y 186
-- Domain 0 - Net 1: net "uAHBUART/count_reg_TR0<20>”
--          - PIP 1:   pip INT_X60Y186 BYP_BOUNCE5 -> IMUX_B29
-- Domain 1 - Net 2: net "uAHBUART/count_reg_TR1<20>”
--          - PIP 2:   pip INT_X60Y186 WL2BEG1 -> IMUX_B26
```

# Results and Classification



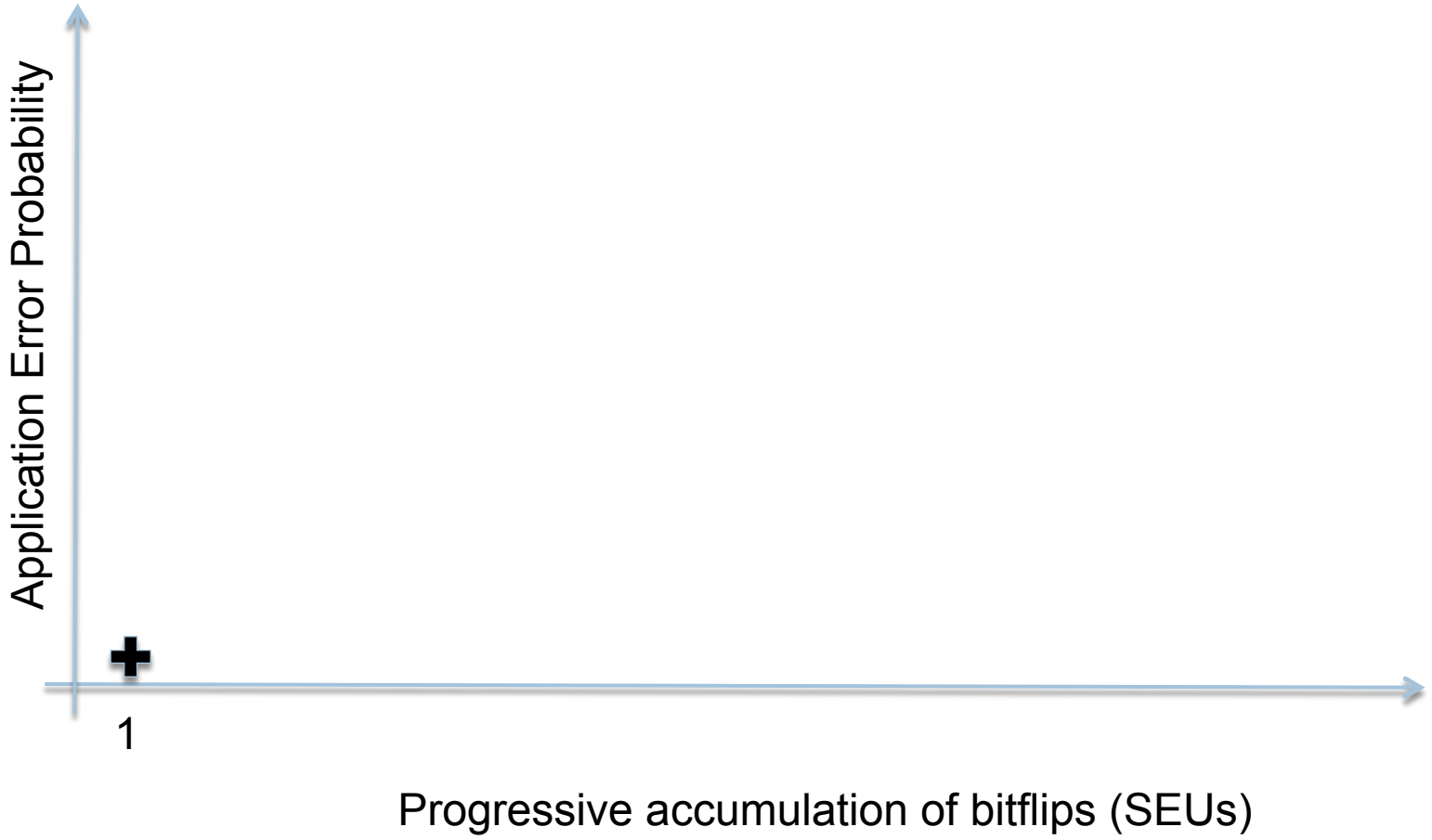
- Calculation of the Application Error Probability



# Results and Classification



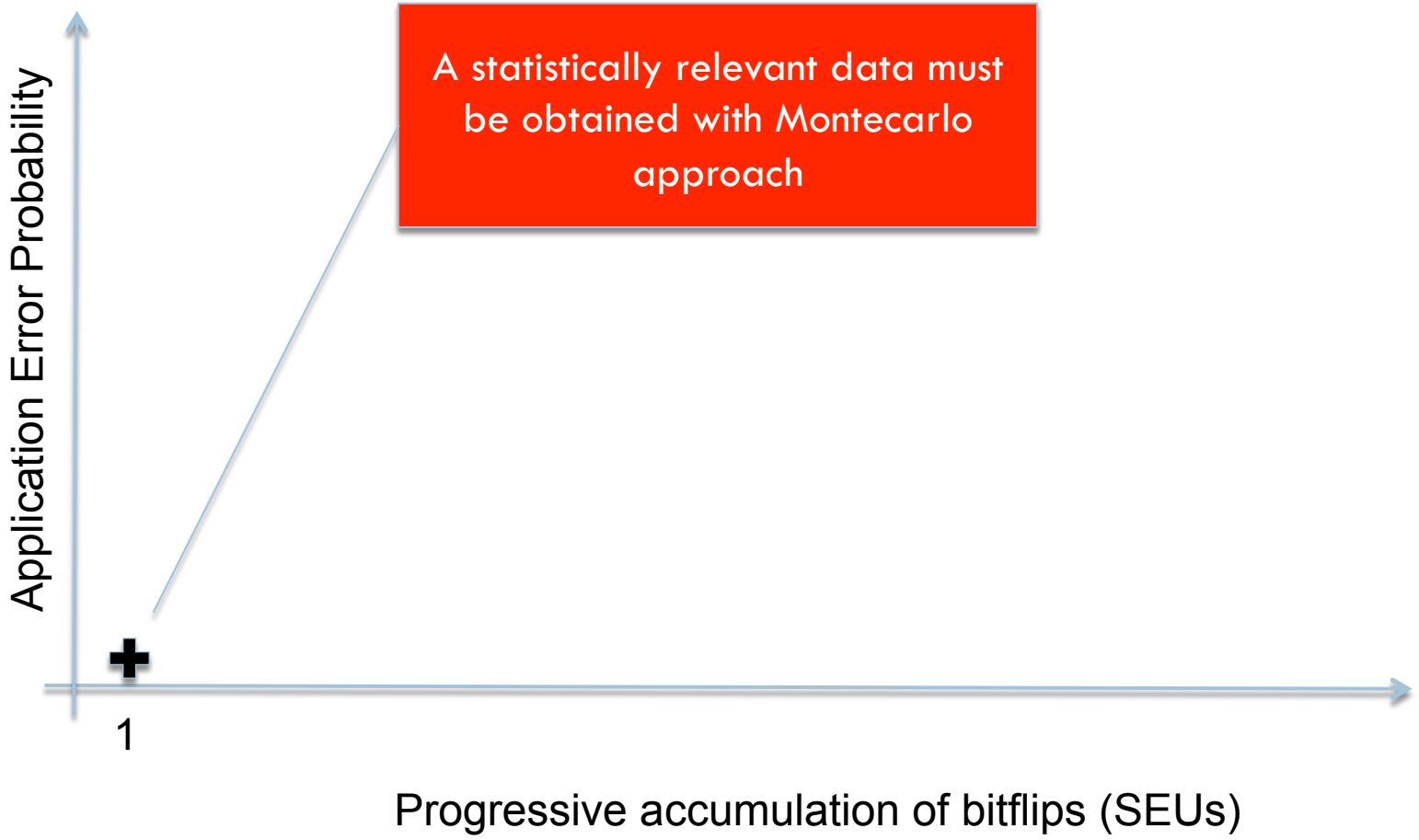
- Calculation of the Application Error Probability



# Results and Classification



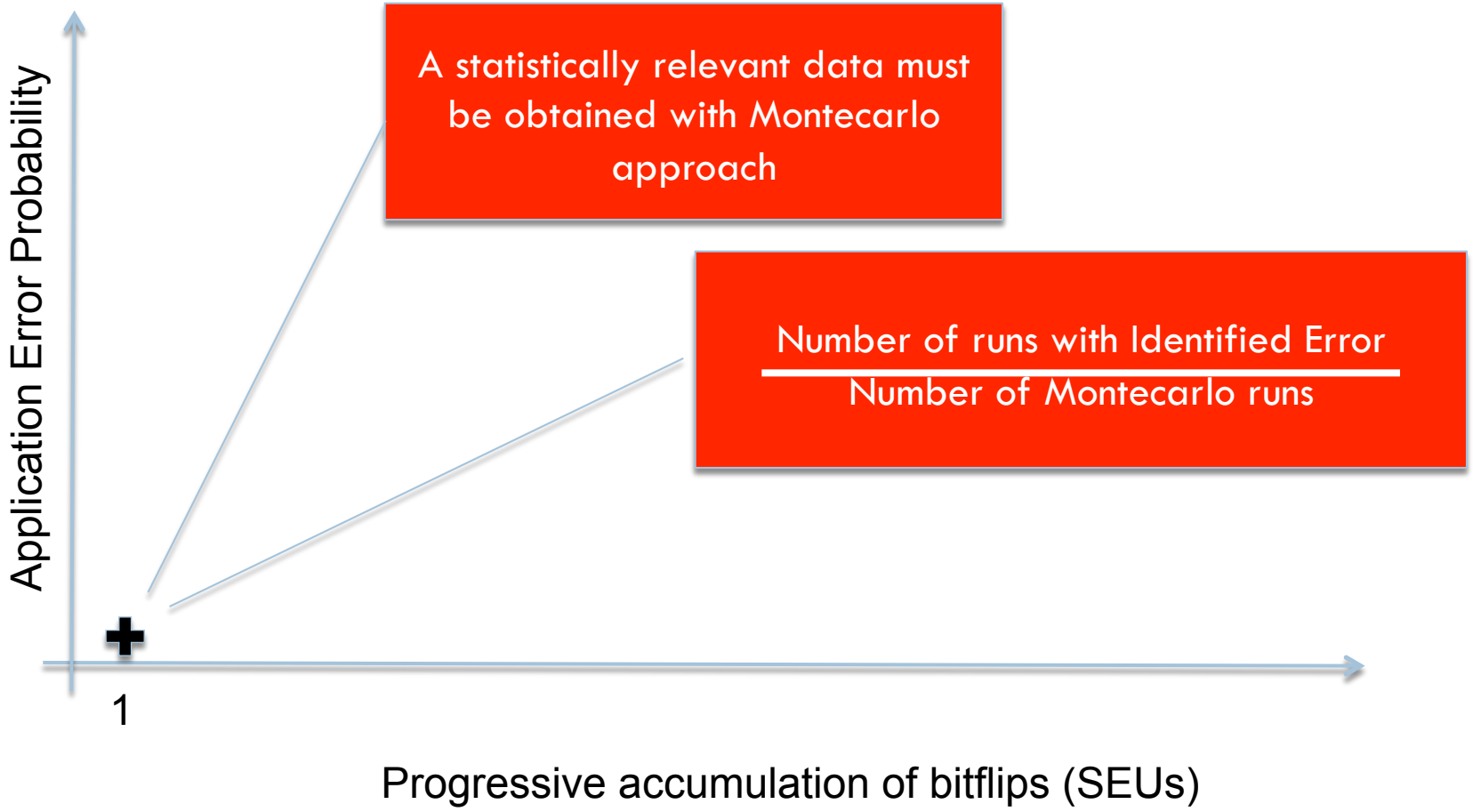
- Calculation of the Application Error Probability



# Results and Classification



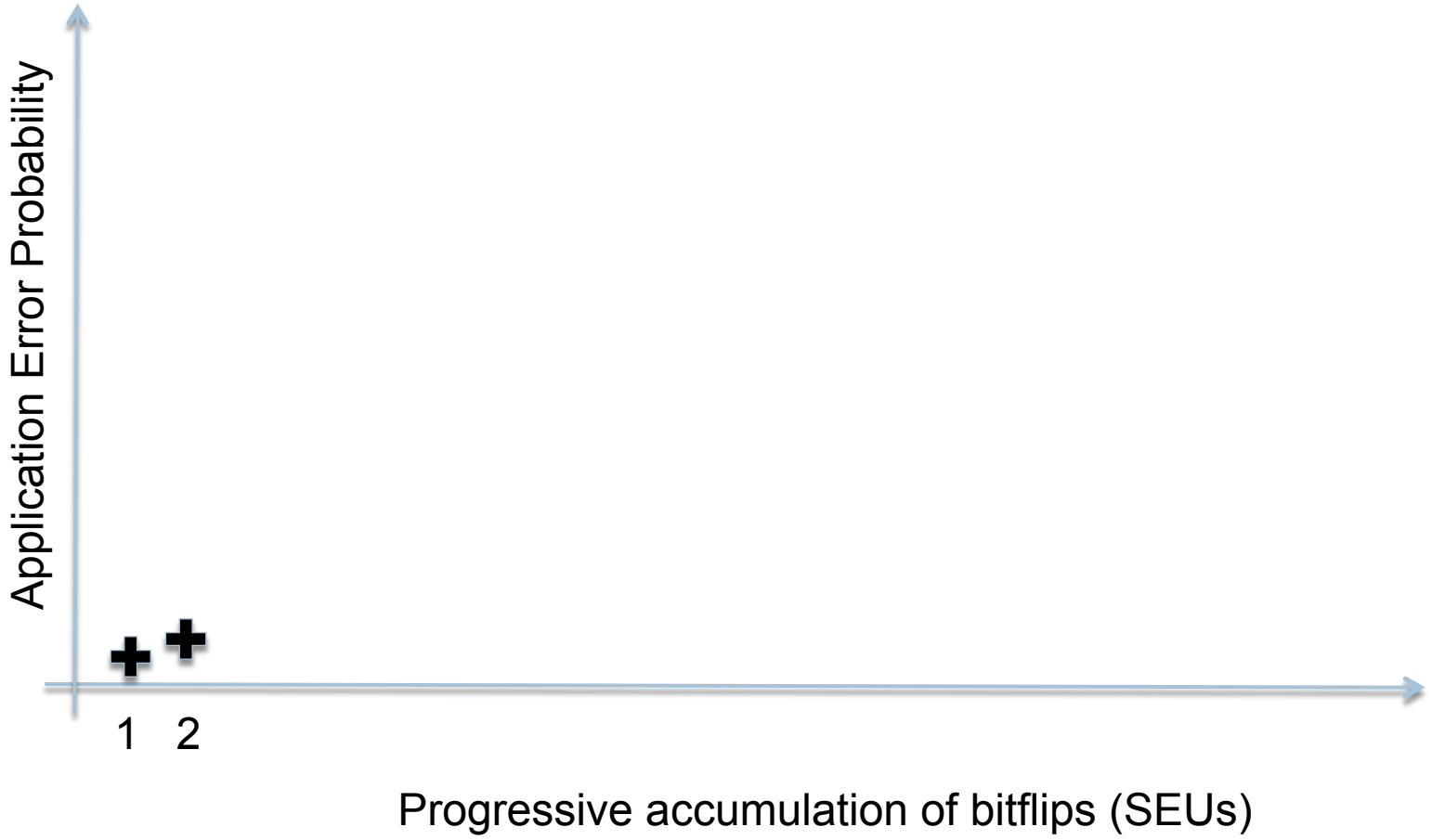
- Calculation of the Application Error Probability



# Results and Classification



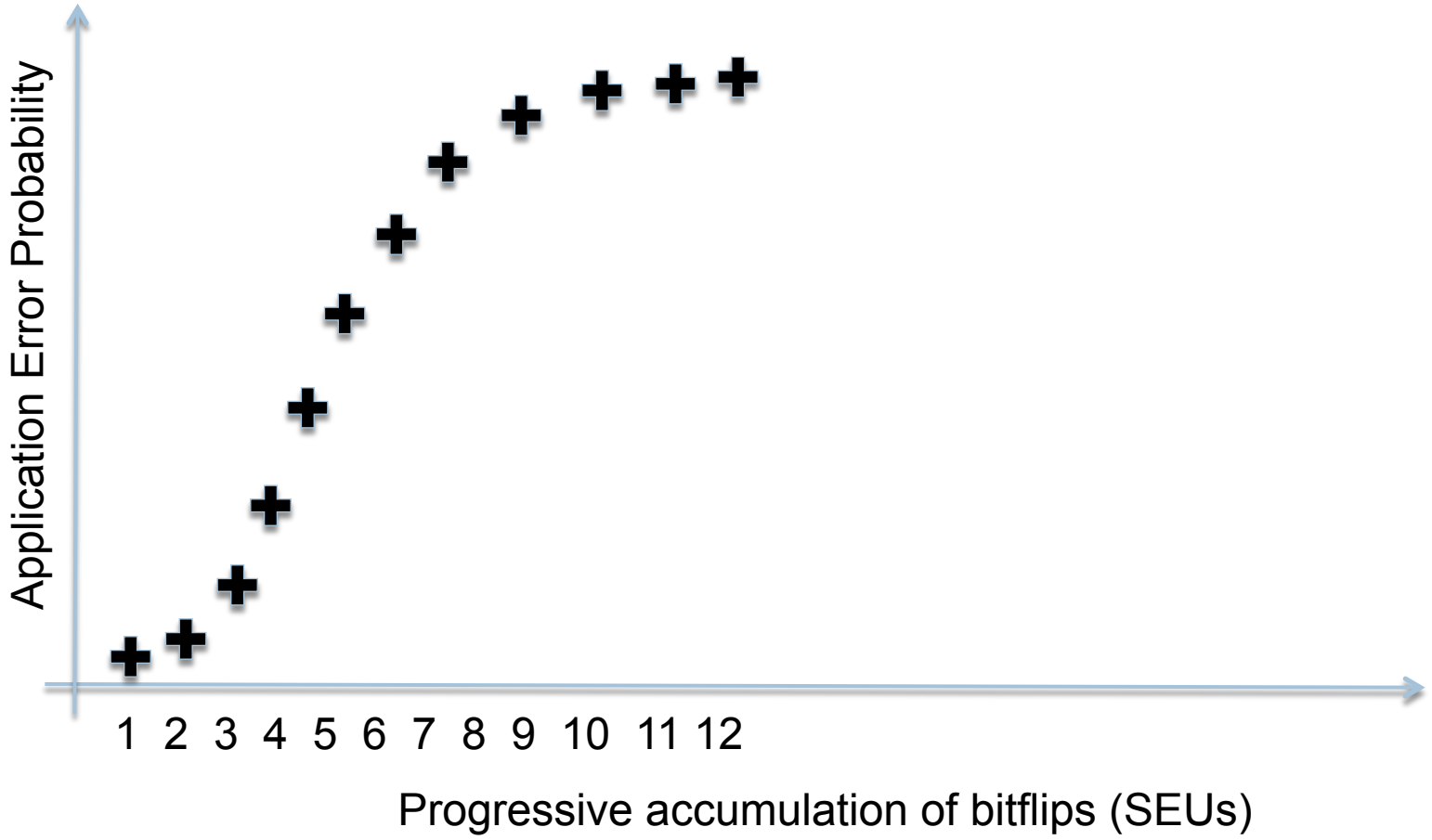
- Calculation of the Application Error Probability



# Results and Classification



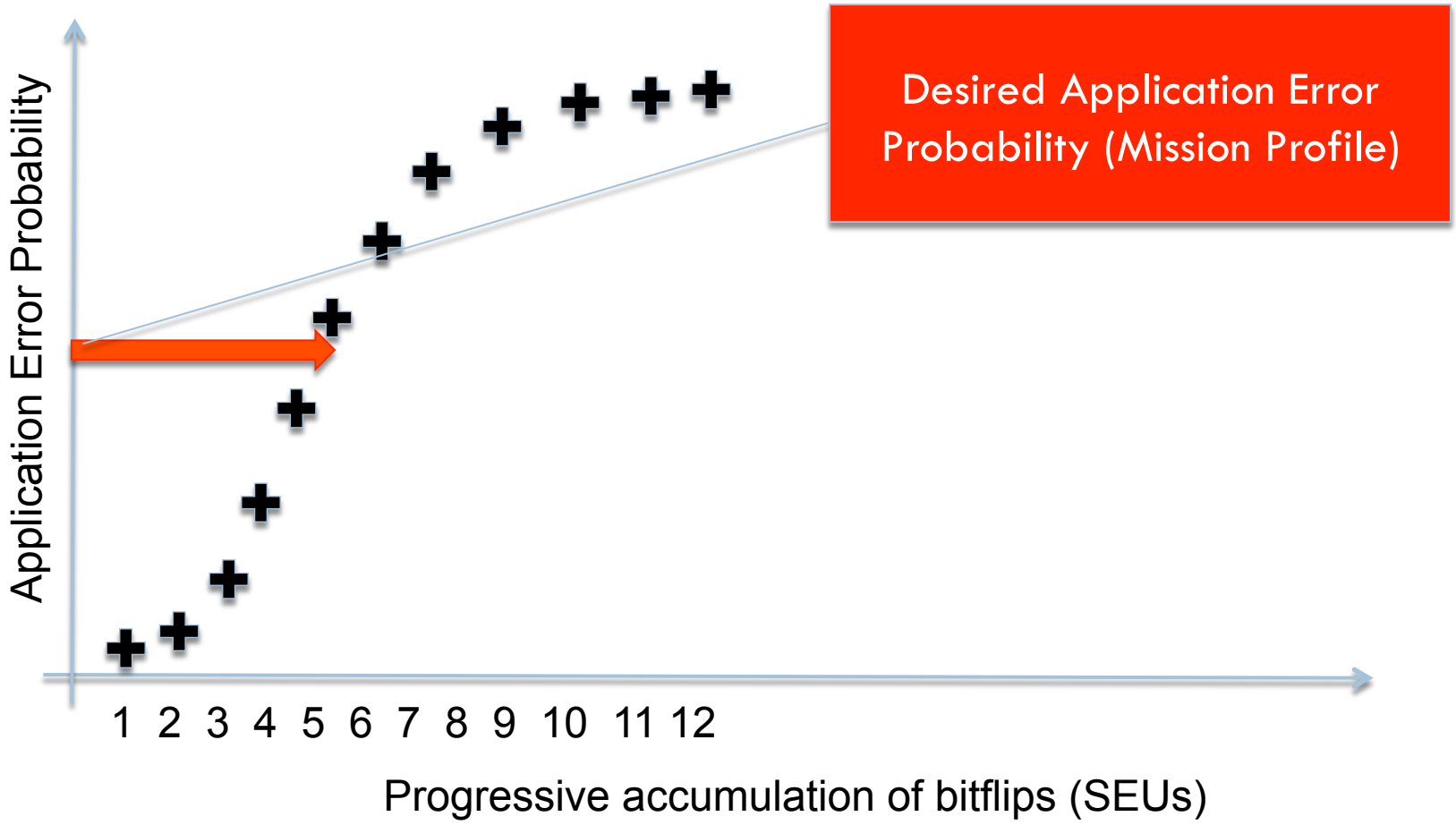
- Calculation of the Application Error Probability



# Results and Classification



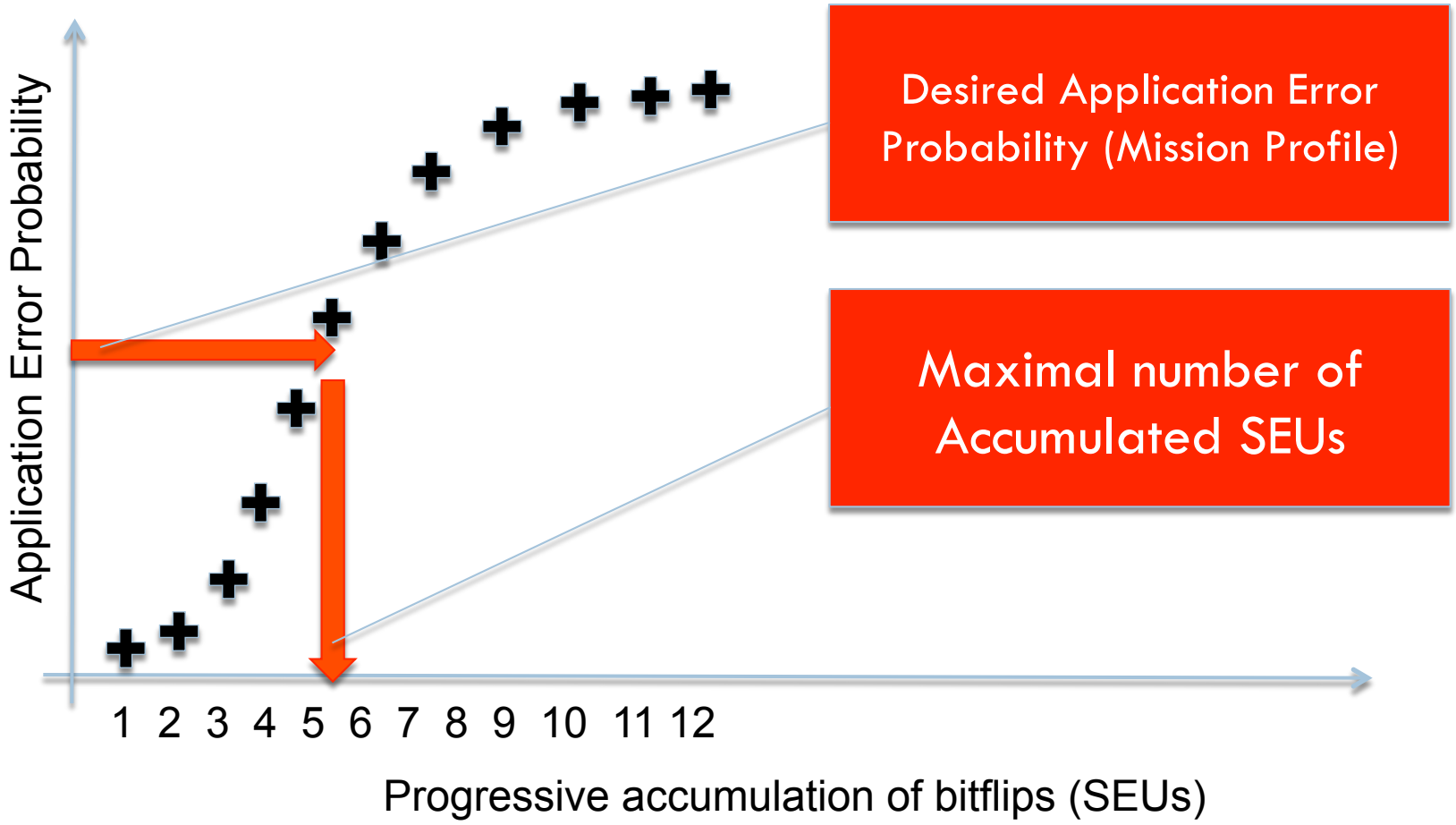
- Calculation of the Application Error Probability



# Results and Classification



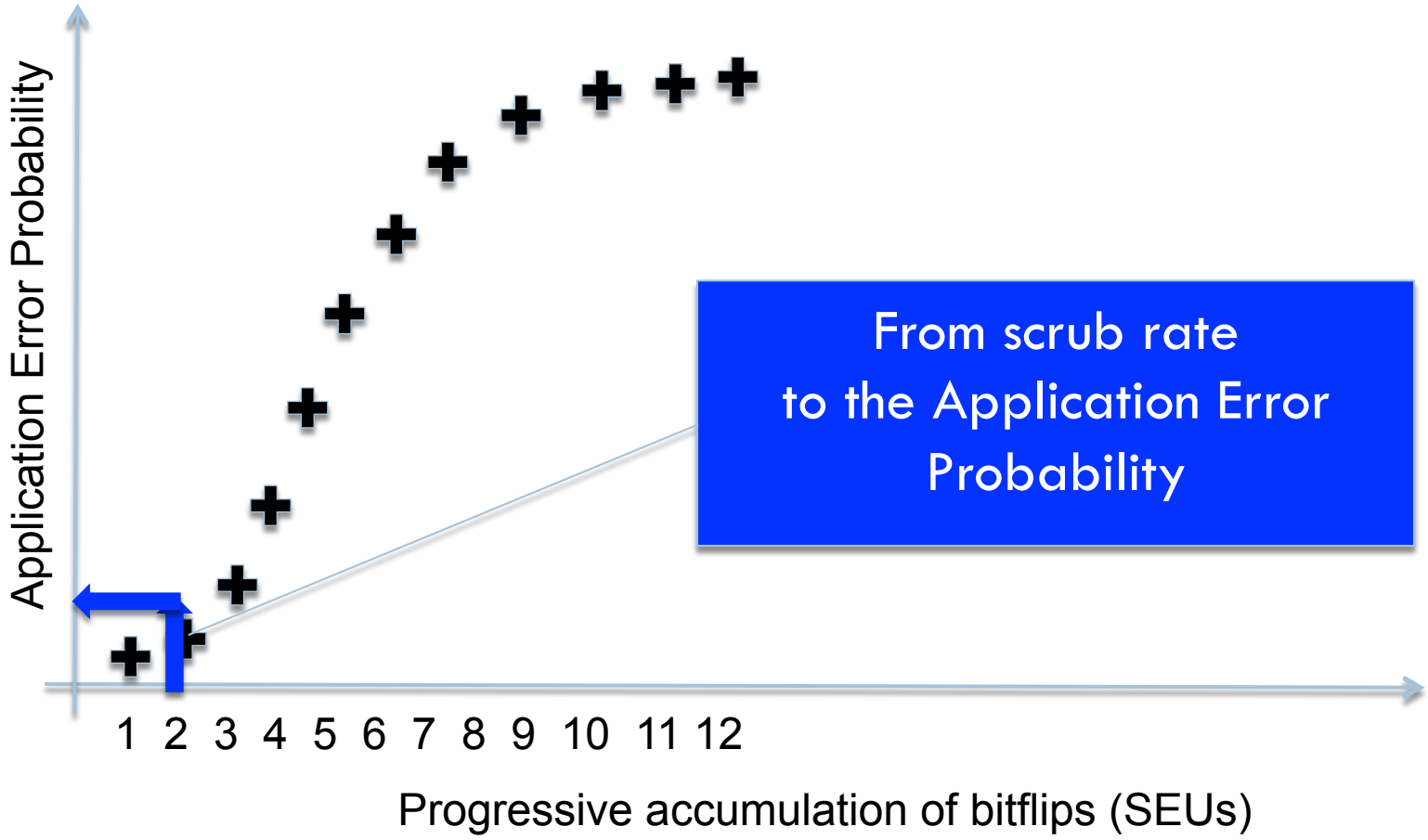
- Calculation of the Application Error Probability



# Results and Classification



- Calculation of the Application Error Probability



# Experimental Results



- B13 from ITC'99 an interface Meteo sensor

B13 circuit characteristics

| Name | VHDL | | | Gate level | | | | Fault list | |
|---|---|---|---|---|---|---|---|---|---|
| | # Line | # Process | Type | Gate | Pi | Po | FF | Complete | Collapse |
| B13 | 296 | 5 | std | 362 | 10 | 10 | 53 | 1,906 | 830 |
| | | | opt | 317 | 10 | 10 | 53 | 1,694 | 77 |

B13 Test Patterns details

| Circuit | # Sequences | # Vectors | Fault Coverage % | Fault detected | Fault Total |
|---|---|---|---|---|---|
| B13 | 5 | 7639 | 81.27 | 1341 | 1650 |

# Experimental Results



- Area occupation on Xilinx Virtex-5 LX50T FPGA

| Circuit | Design Topology | PLAIN | XTMR | VP-XTMR |
|---|---|---|---|---|
| B13 | Slice FF | 62/28800 - 1% | 147/28800 - 1% | 147/28800 - 1% |
| | Slice LUTs | 84/28800 - 1% | 369/28800 - 1% | 369/28800 - 1% |
| | Slices Distribution | 42/7200 - 1% | 177/7200 - 2% | 177/7200 - 2% |
| B13 x 30 | Slice FF | 1590/28800 - **5%** | 4770/28800 - **16%** | 4770/28800 - **16%** |
| | Slice LUTs | 1830/28800 - **6%** | 10,841/28800 - **37%** | 10,841/28800 - **37%** |
| | Slice Distribution | 827/7200 - **11%** | 4791/7200 - **66%** | 4791/7200 - **66%** |

# Experimental Results

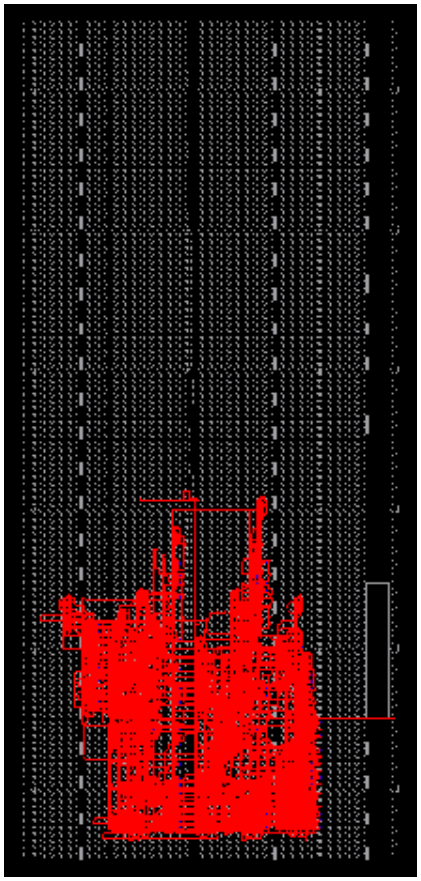


- 3 different design topologies have been tested at Los Alamos
  - **PLAIN** : b13x30 without any type of hardening
  - **XTMR**: Triple Modular Redundancy version with converge option of outputs pins using Xilinx TMRTool 2.1.76
  - **VP-XTMR**: Hardening version of XTMR with re-placement constraints generated byVERI-Place tool.

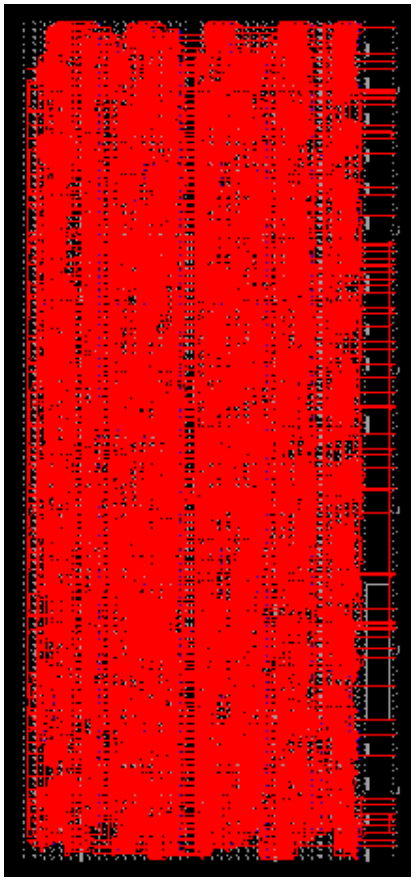
# Experimental Results



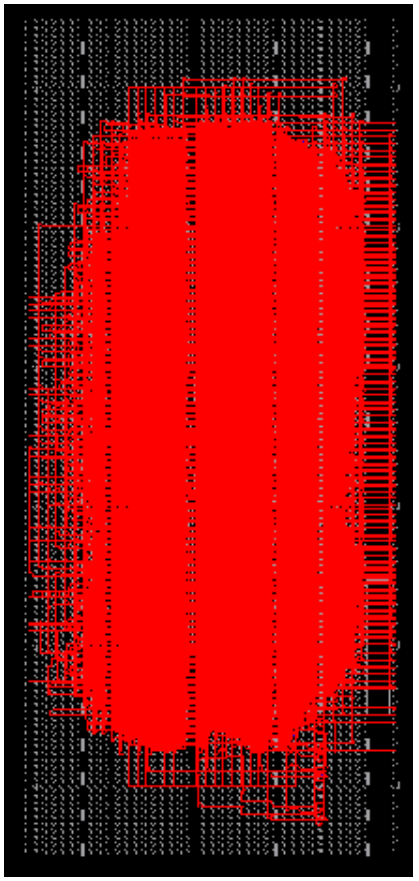
**B13x30 - PLAIN**



**B13x30 - XTMR**



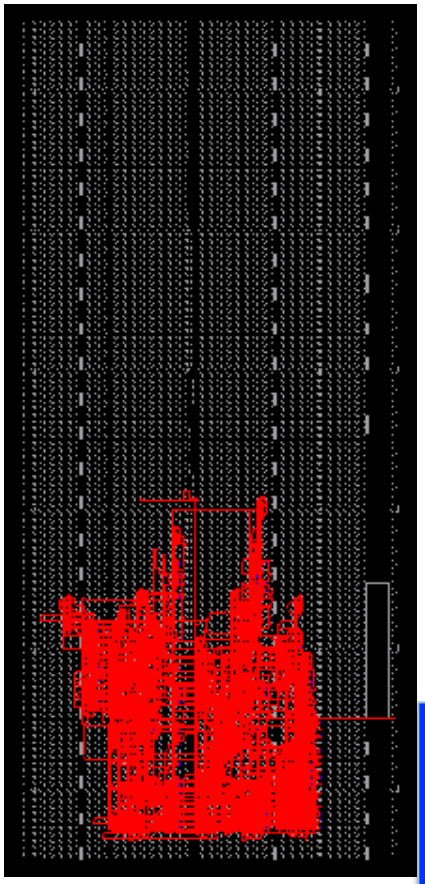
**B13x30 – VP-XTMR**



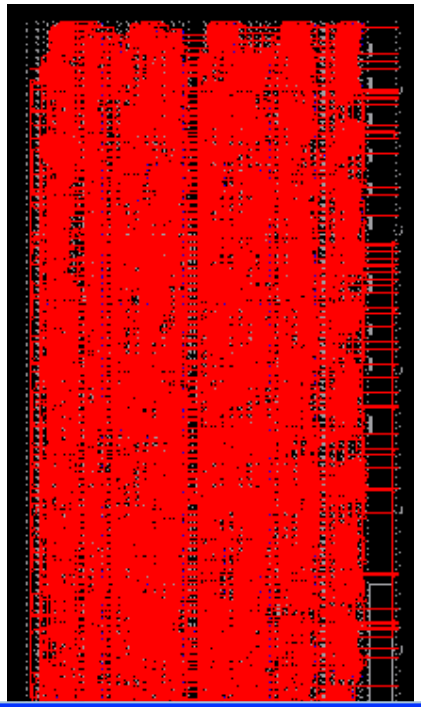
# Experimental Results



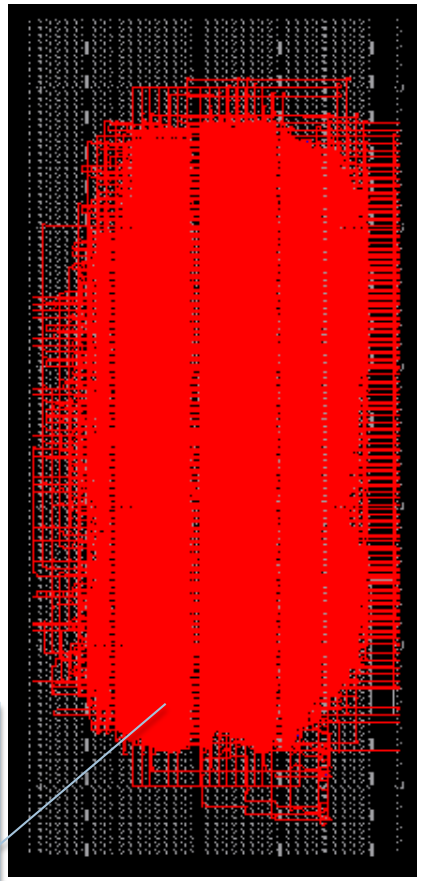
B13x30 - PLAIN



B13x30 - XTMR



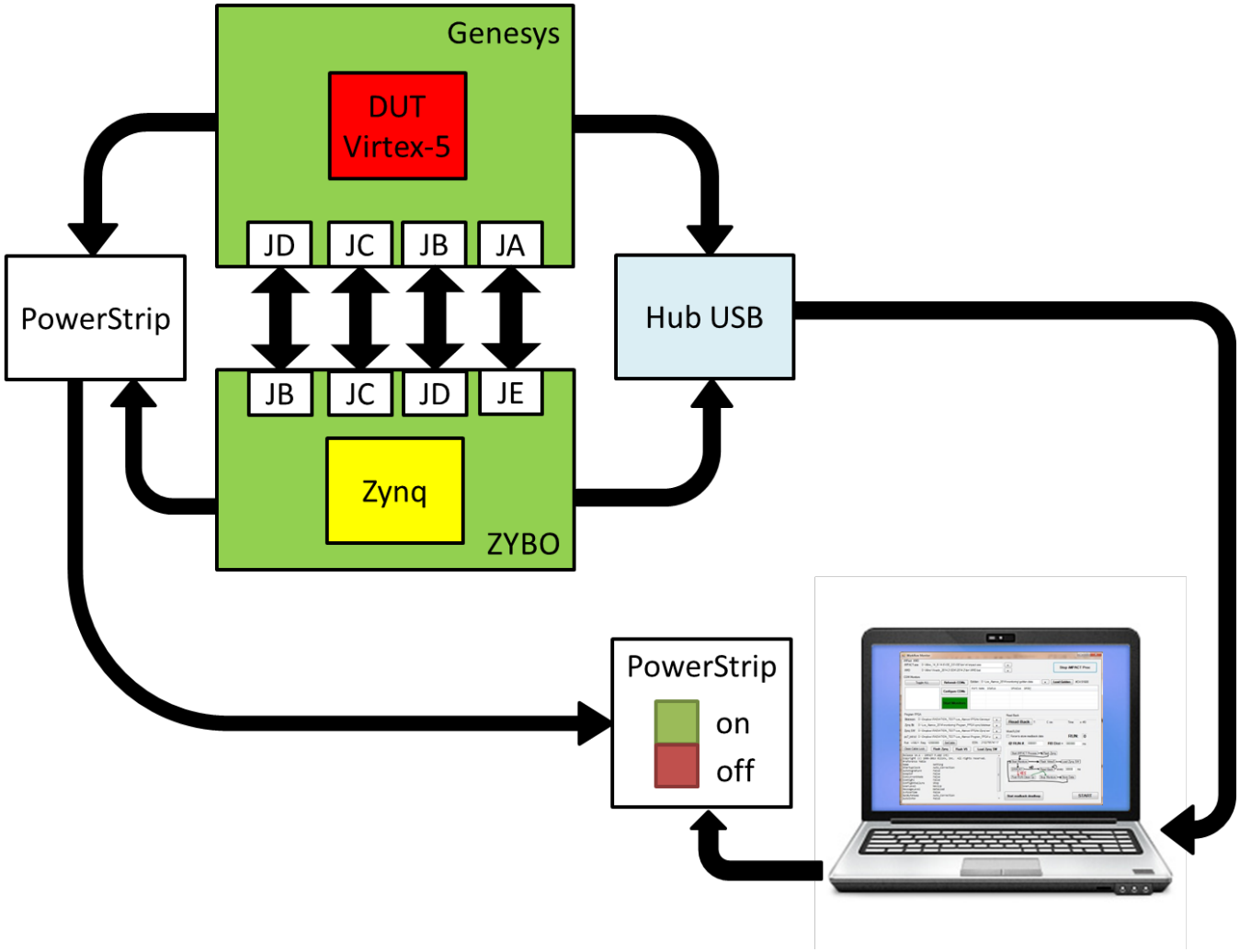
B13x30 – VP-XTMR



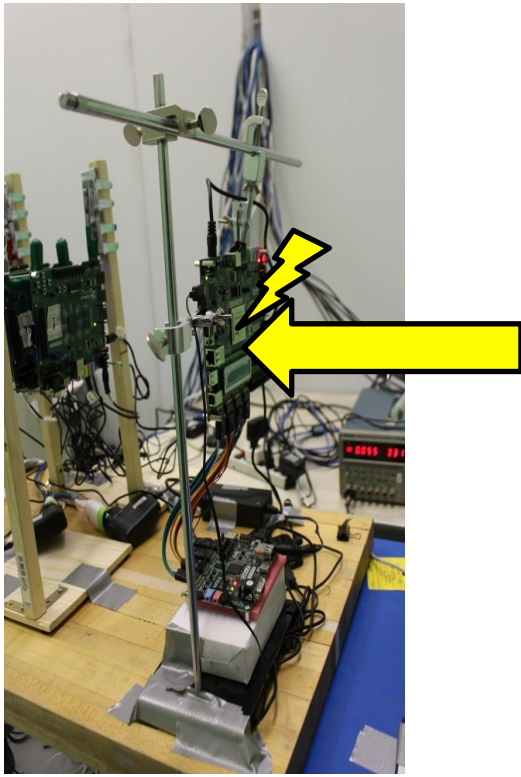
The Layout is complementary with Isolation Design Flow

# Experimental Results



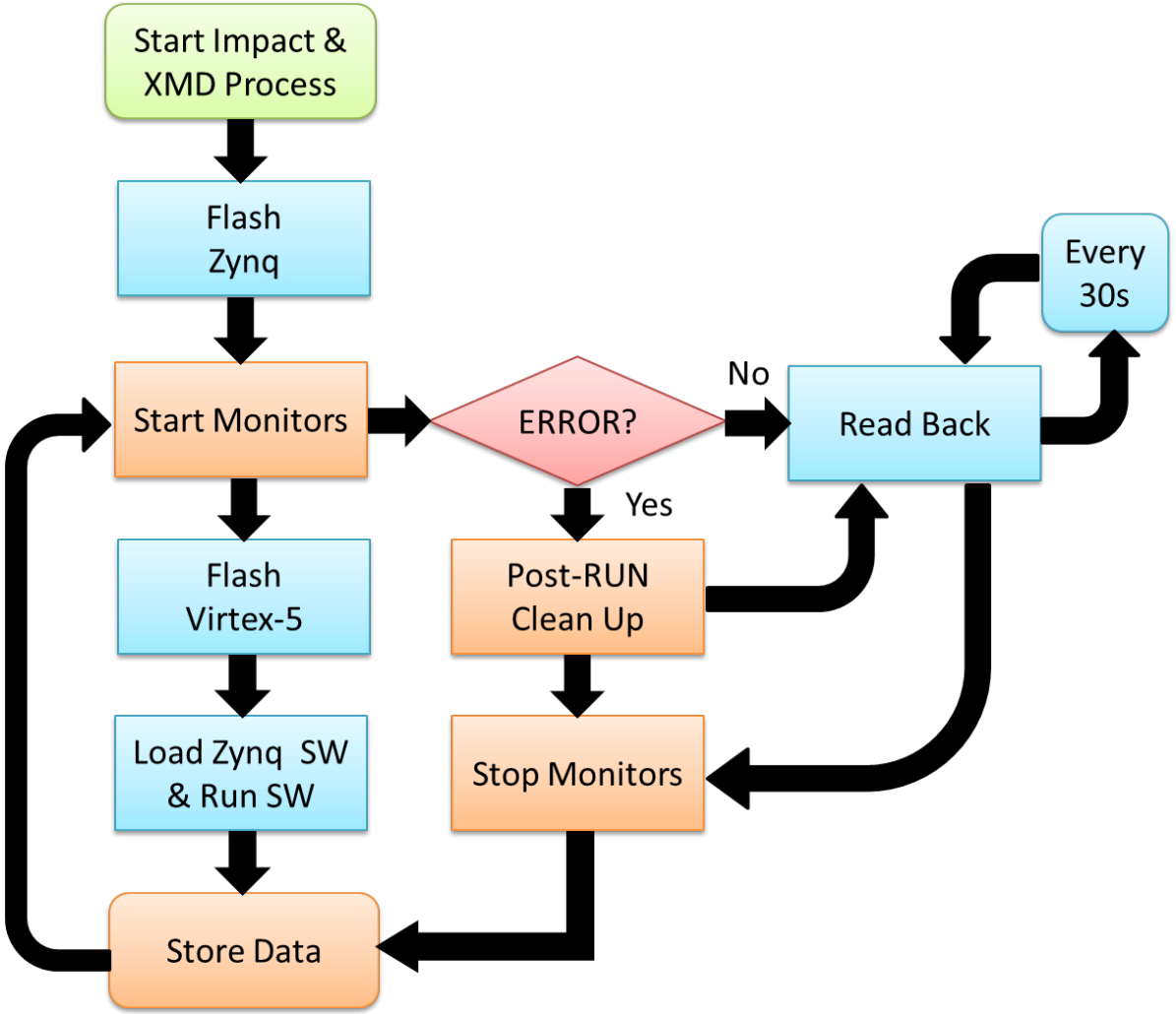



Neutron Beam



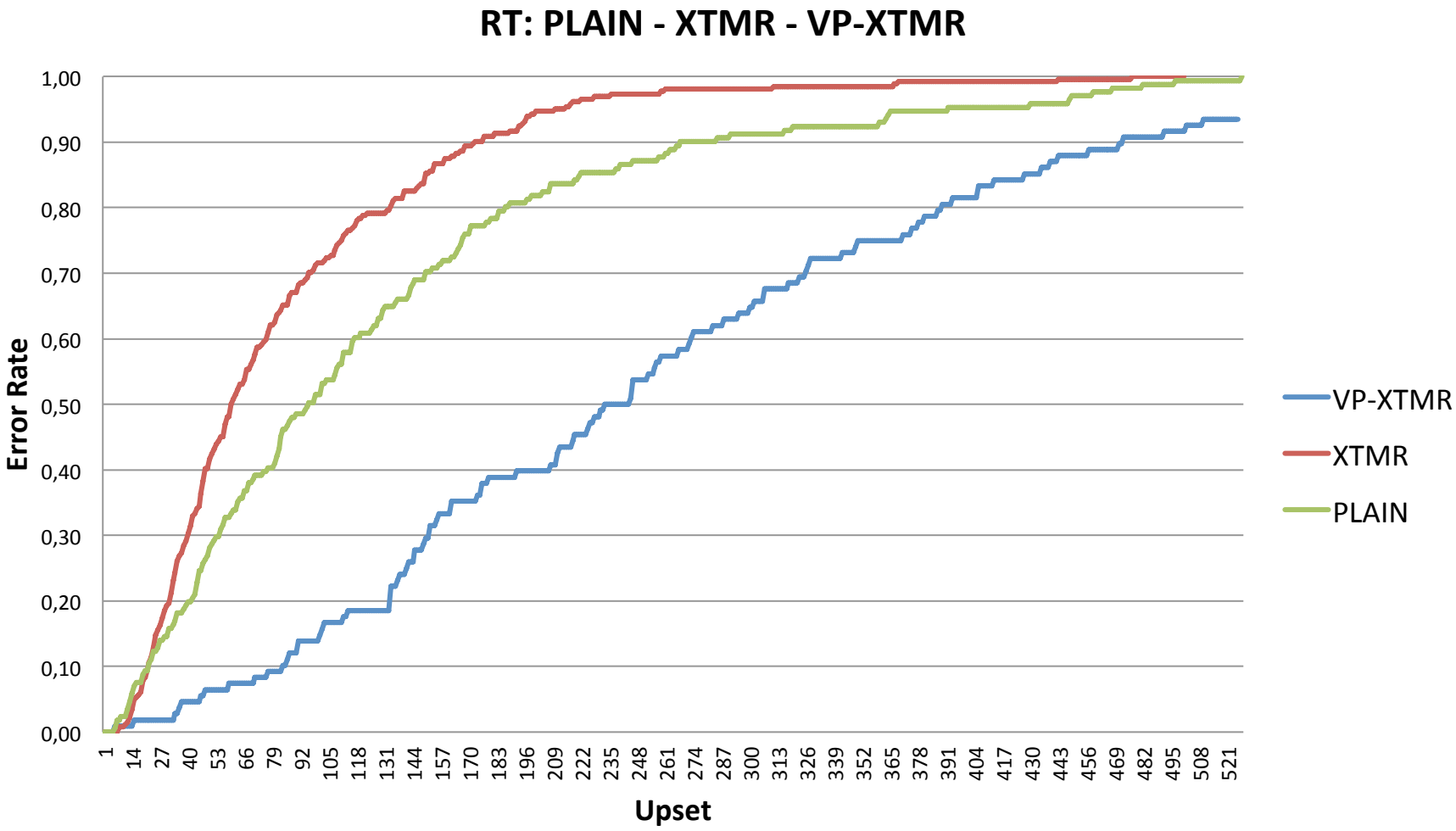
# Test Methodology





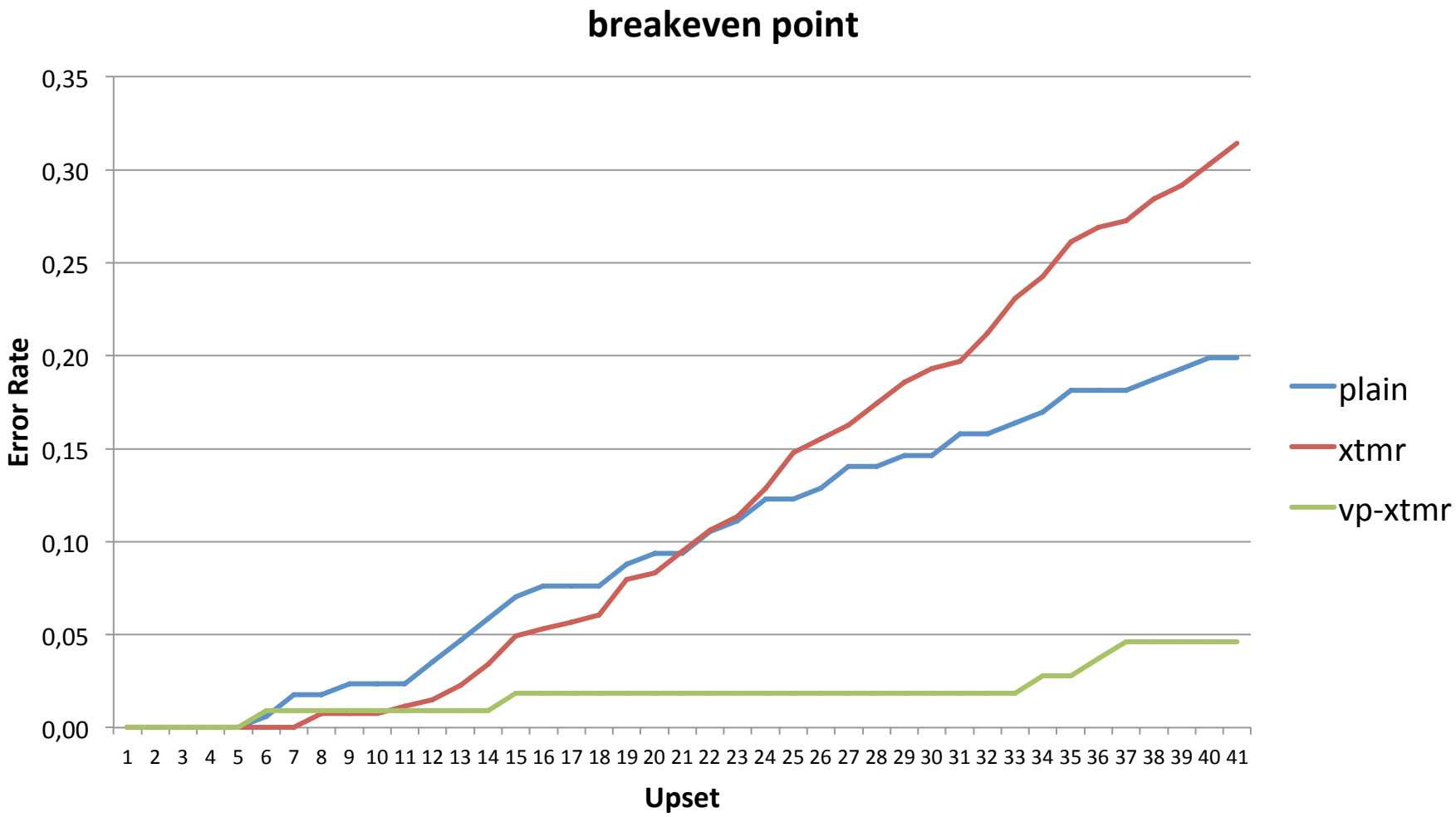
# Experimental results





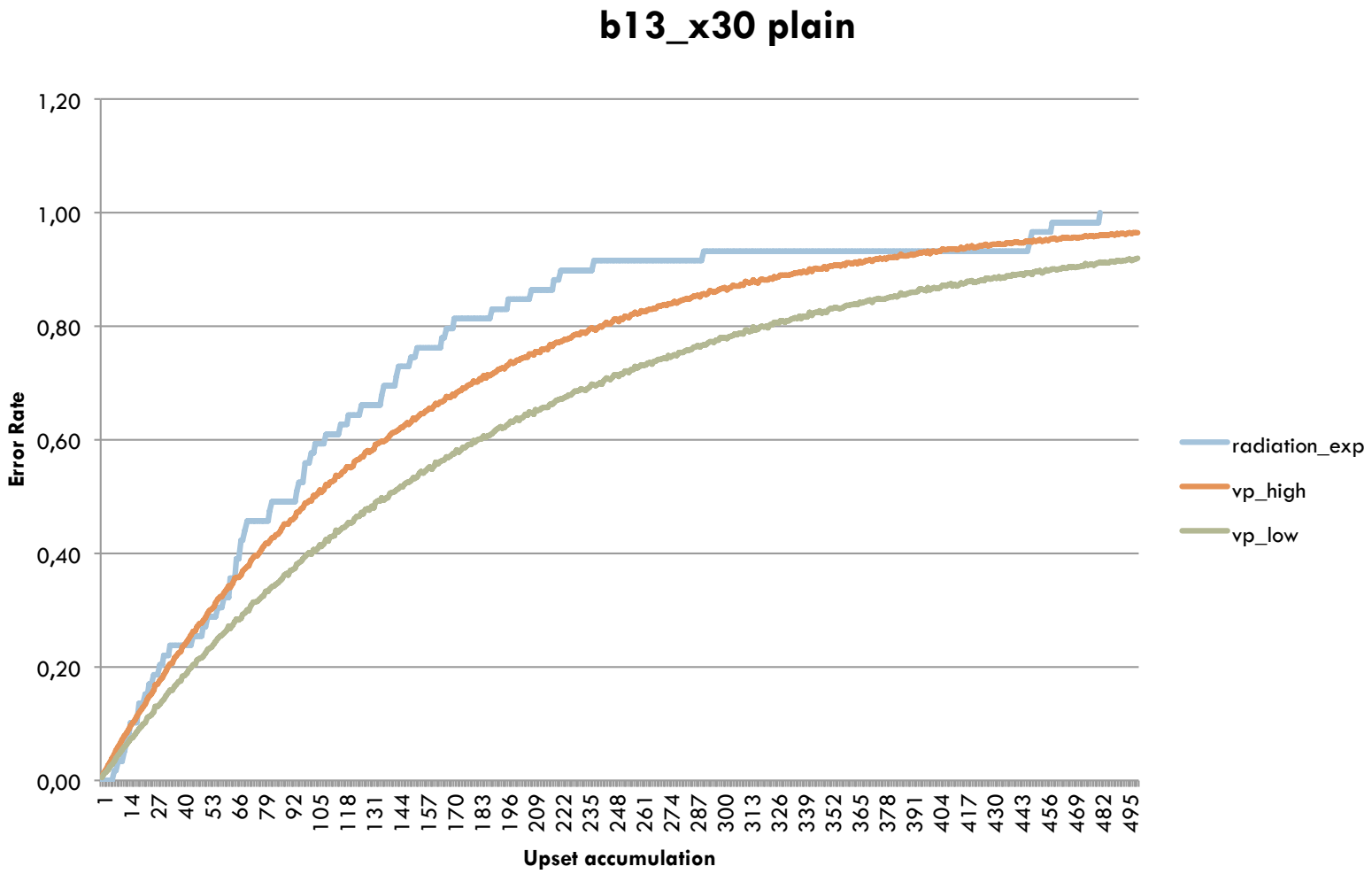
# Experimental results





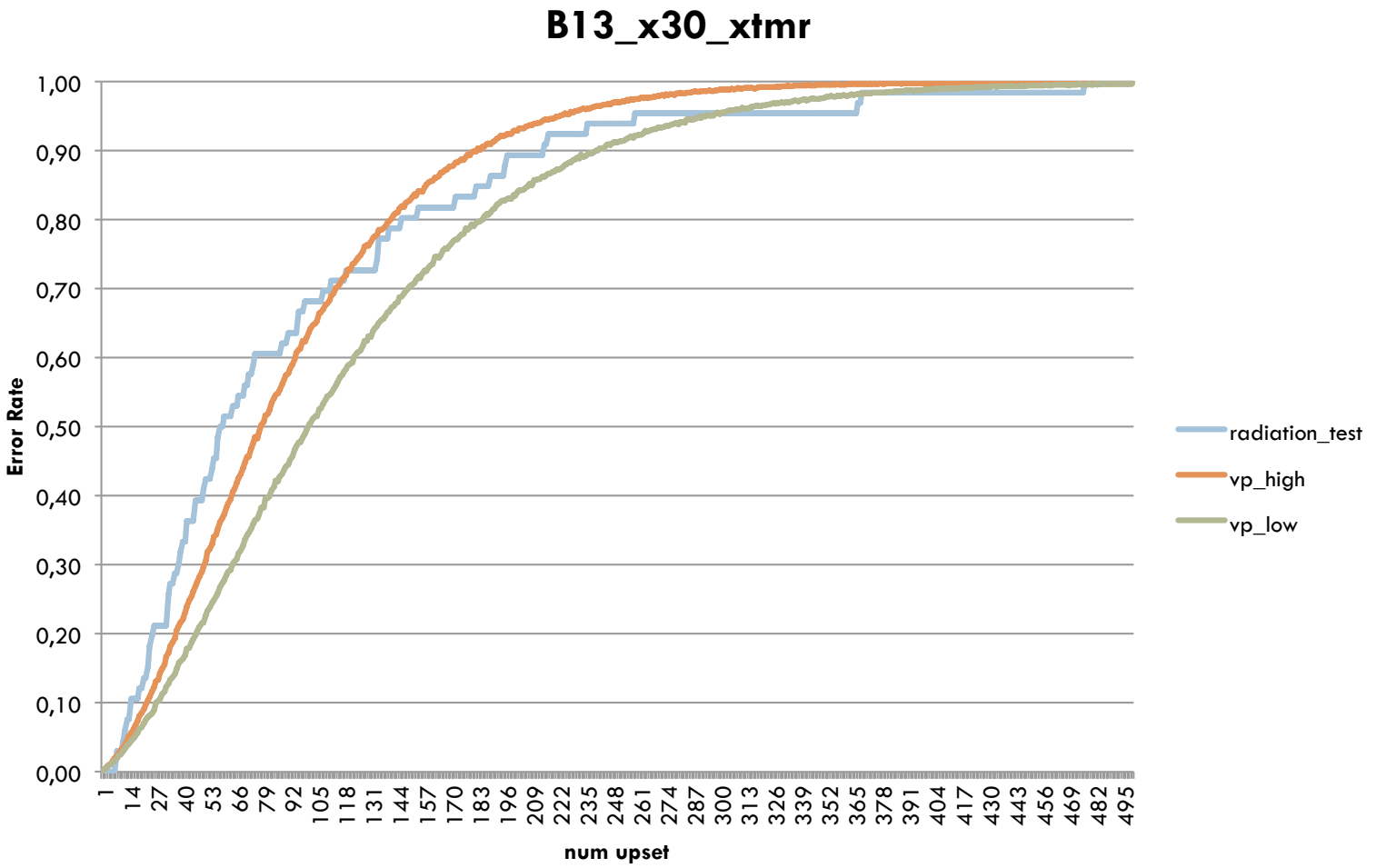
# Experimental results – Plain Prediction





# Experimental results – XTMR Prediction





# Experimental results – ARM-M0

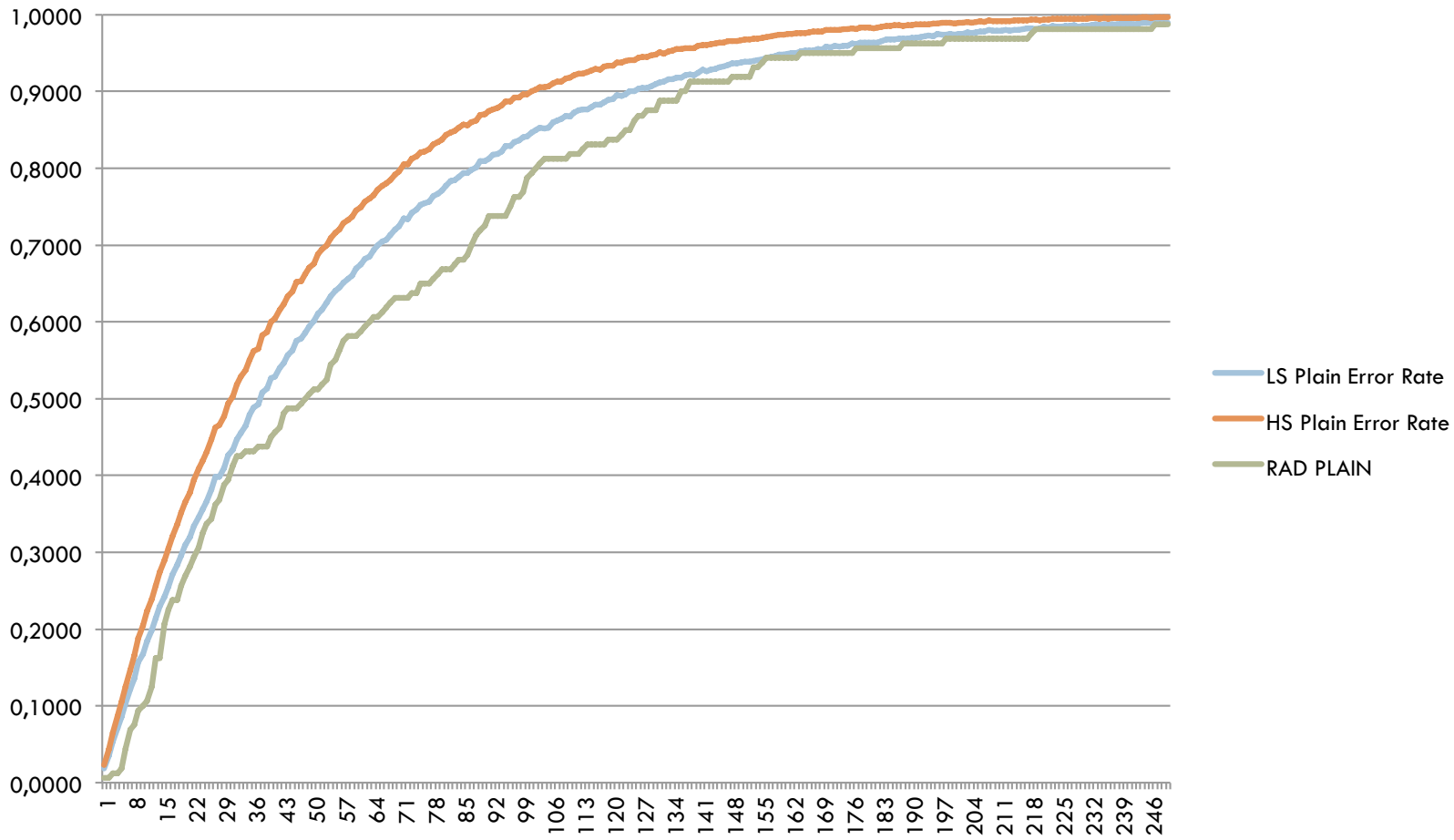


- ARM-M0 processor has been tested at PSI
  - Available flux of proton: 7.22E6 [p/(cm$^2$s)]
  - Working frequency of 50 Mhz
  - Software: Bubble sort

| Design Version | LUTs[#] | FFs[#] | BRAM[#] |
|---|---|---|---|
| *Plain* | 3563 (12%) | 961 (3%) | 4 (6%) |
| *XTMR* | 13,229 (45%) | 2887 (10%) | 12 (20%) |
| *XTMR-VP* | 13,229 (45%) | 2887 (10%) | 12 (20%) |

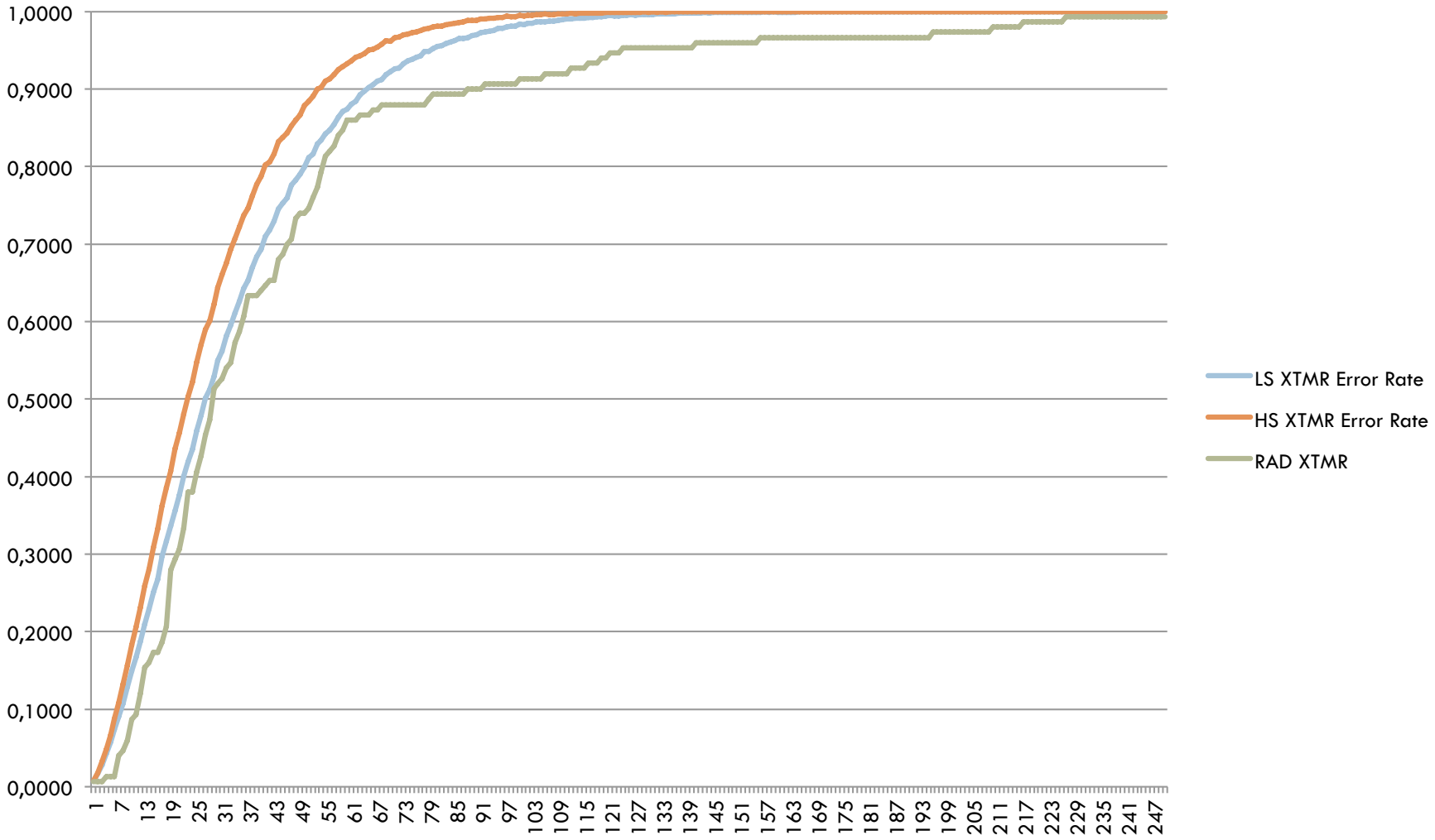
# Experimental results – ARM Plain prediction





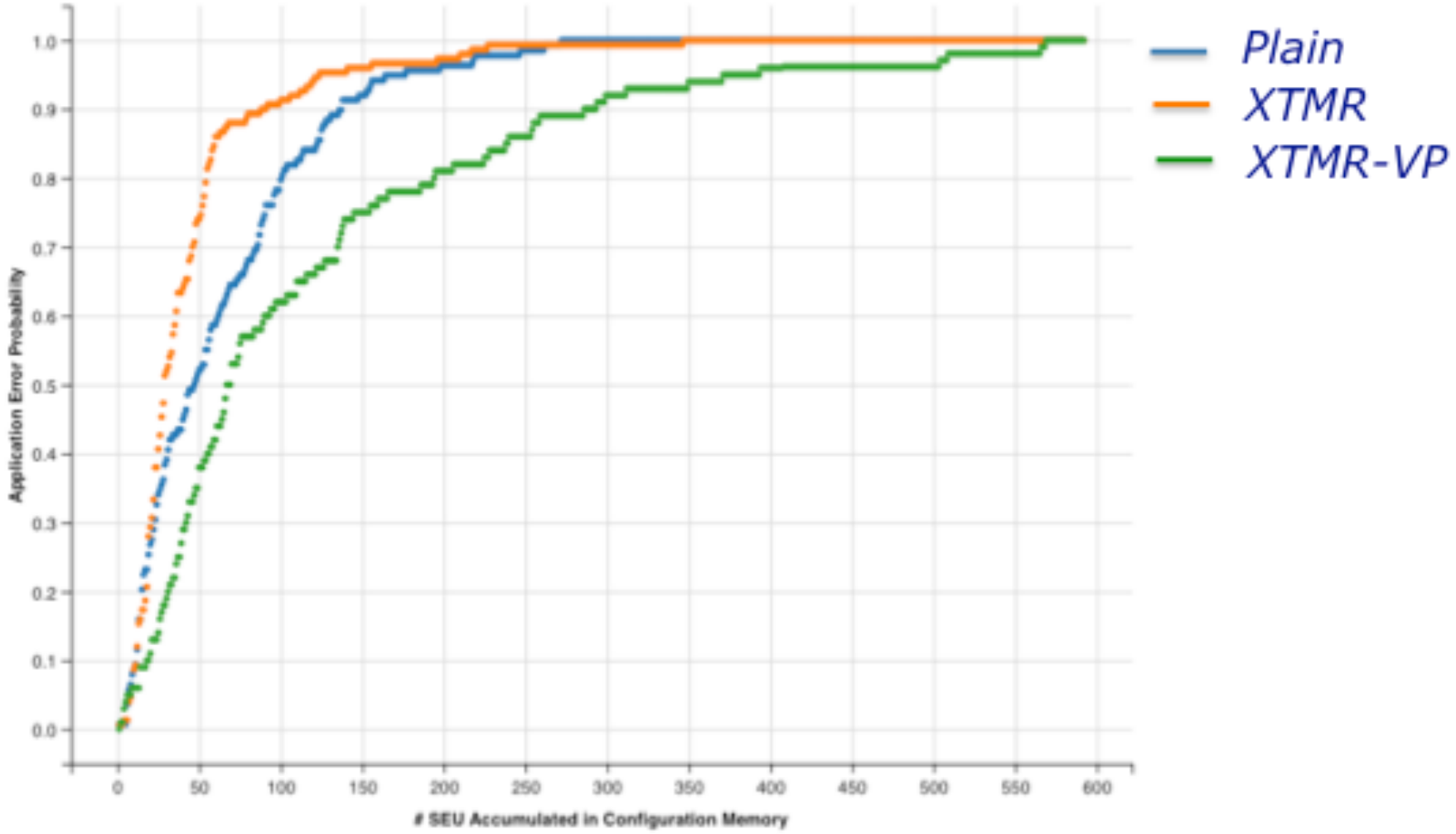
# Experimental results – ARM XTMR Prediction





# Experimental results – ARM overall results





# Conclusions and future works



- VERI-Place for Virtex-5LX50T is available online
  - Fault injection tests executed
  - Radiation test validate VERI-Place
  - Specific versions released to some users
- VERI-Place is available for Zynq family
- VERI-Place for Kintex7-X7K325T is available upon request
  - Fault injection is ongoing
  - Radiation test is planned

# Thank you!

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