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European Space Agency

Using Dynamic Circuit Specialization to enable Microreconfigurations for Space Applications

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Outline

- Introduction to Dynamic Circuit Specialization (DCS)
- FIR as a Parameterized Design
- Microreconfiguration process
- Space applications

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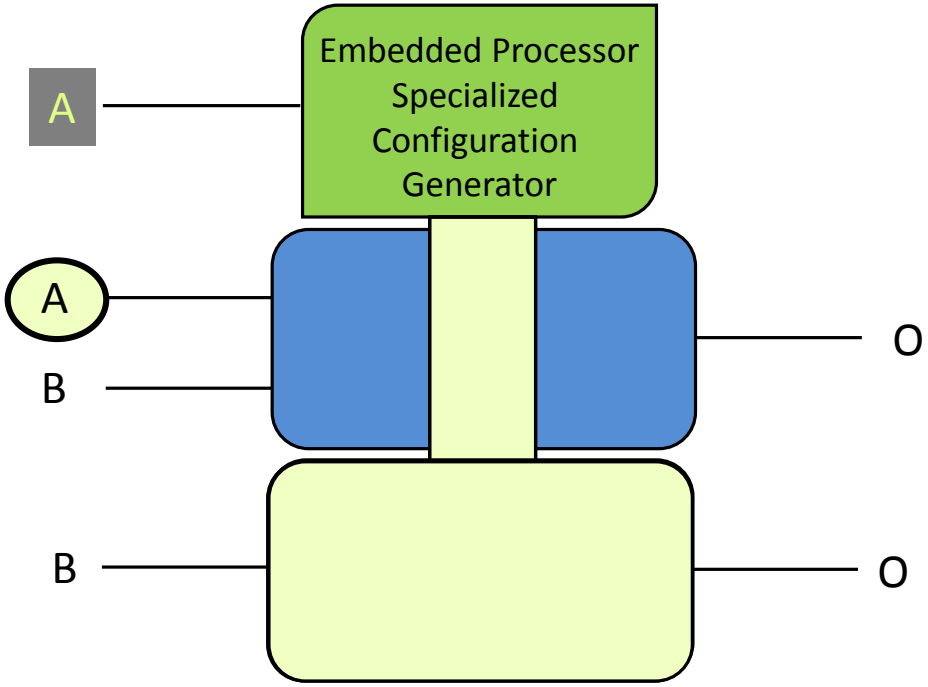
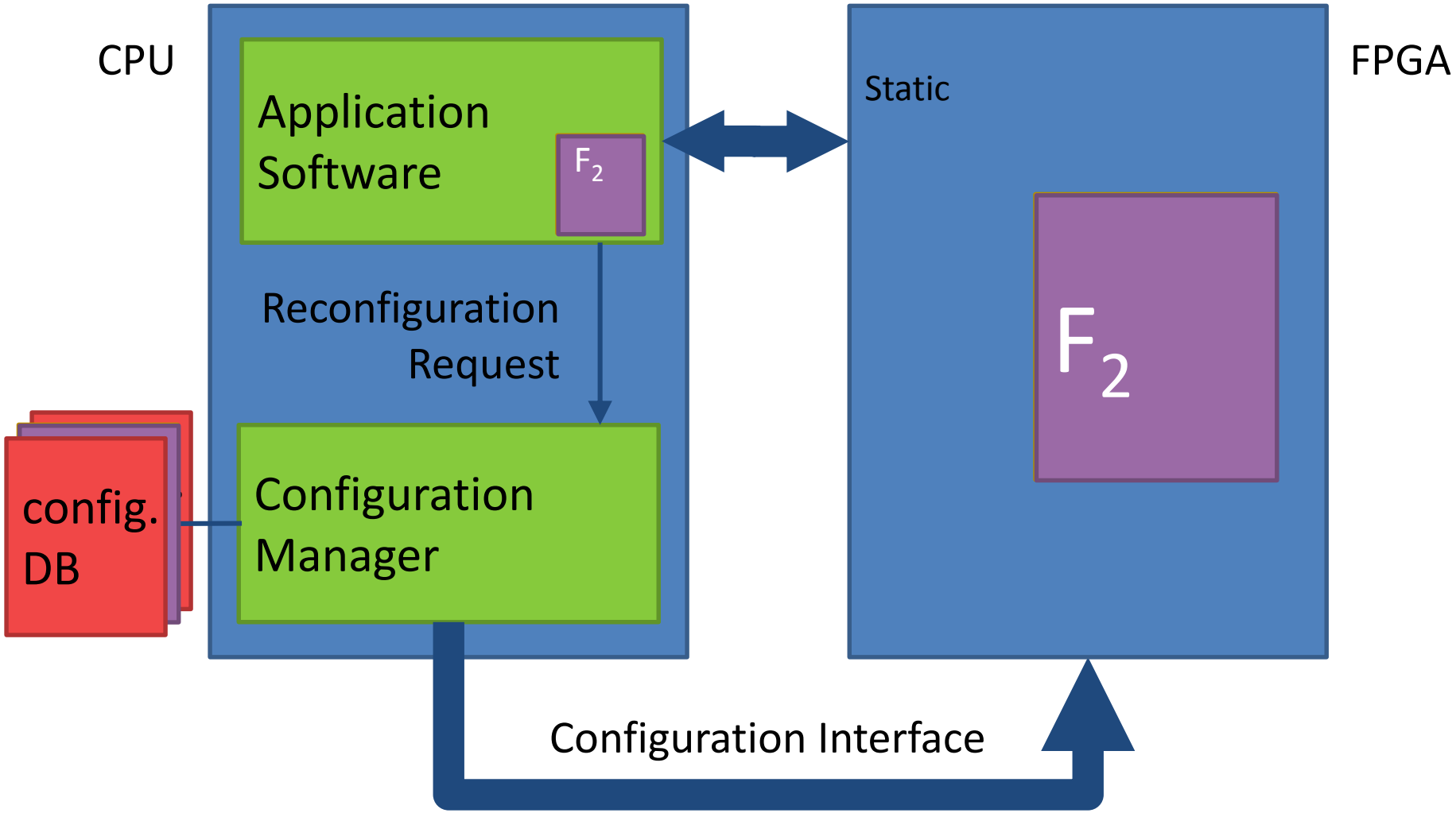
Introduction

- What is Dynamic Circuit Specialization (DCS)?
  - An Optimized FPGA implementation technique
- What kind of applications are suitable?
  - Parameterized Application
- How Beneficial is the DCS?
  - Reduction in FPGA resource (LUTs) utilization by the design
- A novel tool flow from HES research group – UGent

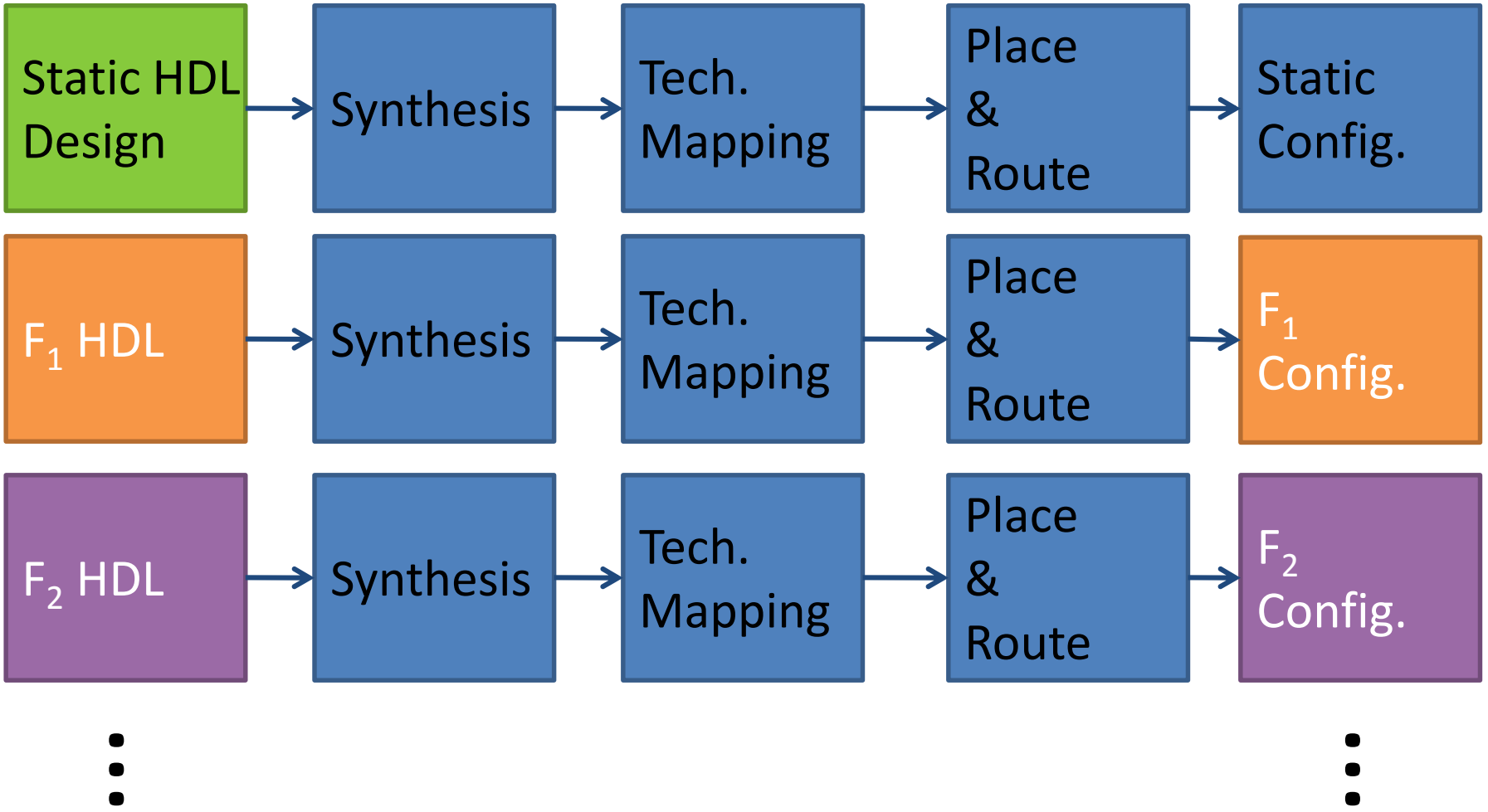
Parameterized Configuration



Conventional Dynamic Reconfiguration (PR)



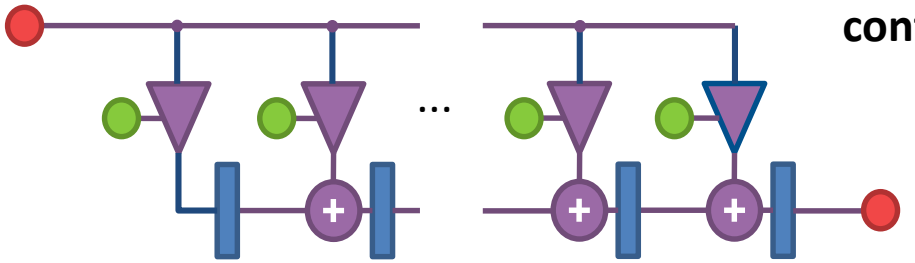
Conventional Tool Flow



Dynamic Circuit Specialization not feasible using conventional PR!

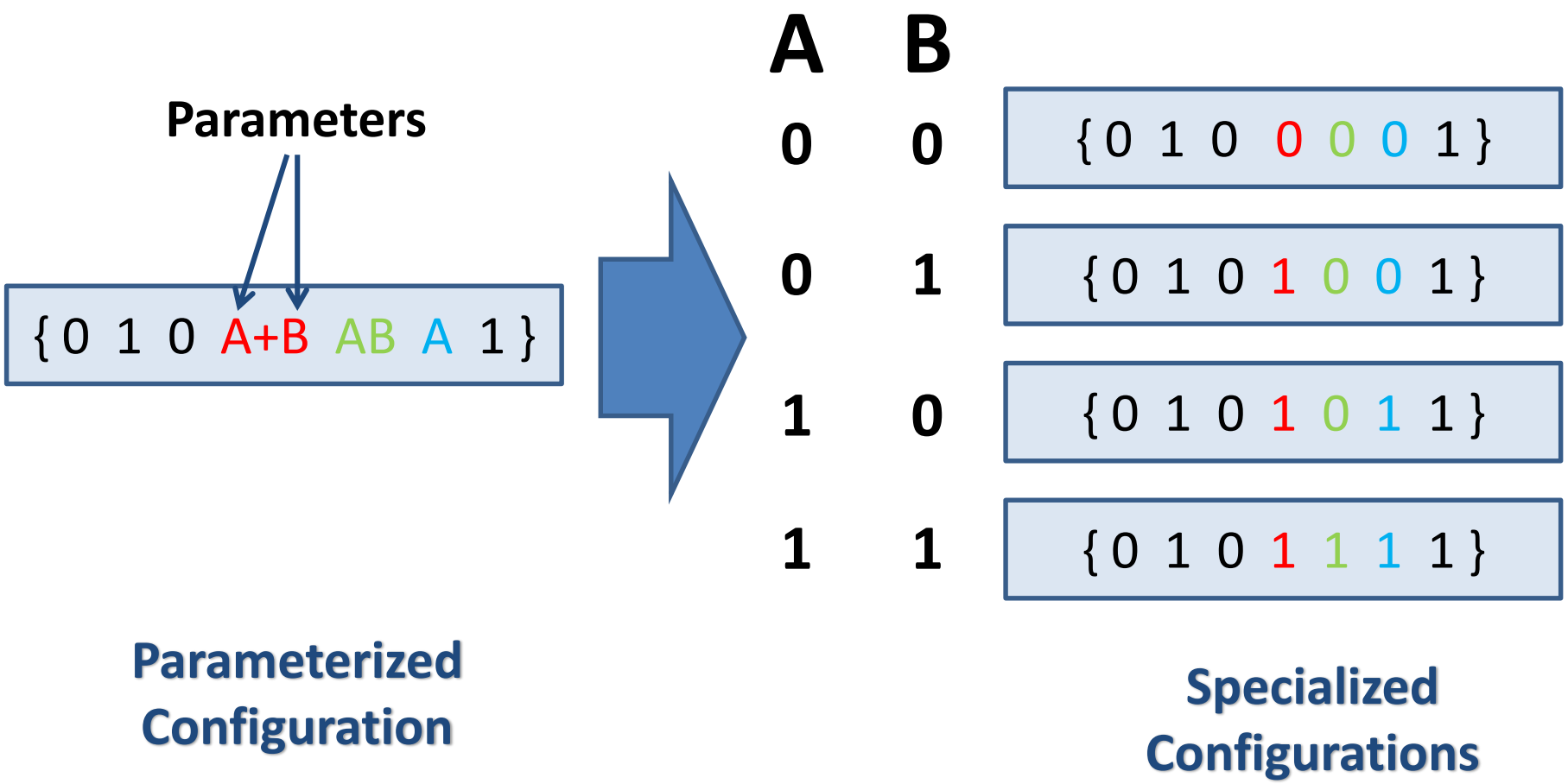
- Application where part of the input data changes infrequently
  - Conventional implementation (no reconfiguration):

    Generic circuit, Store data in memory, Overwrite memory
  - Dynamic circuit specialization:
    Reconfigure with configuration specialized for the data
- Example: Adaptive FIR filter (16-tap, 8-bit coefficients)



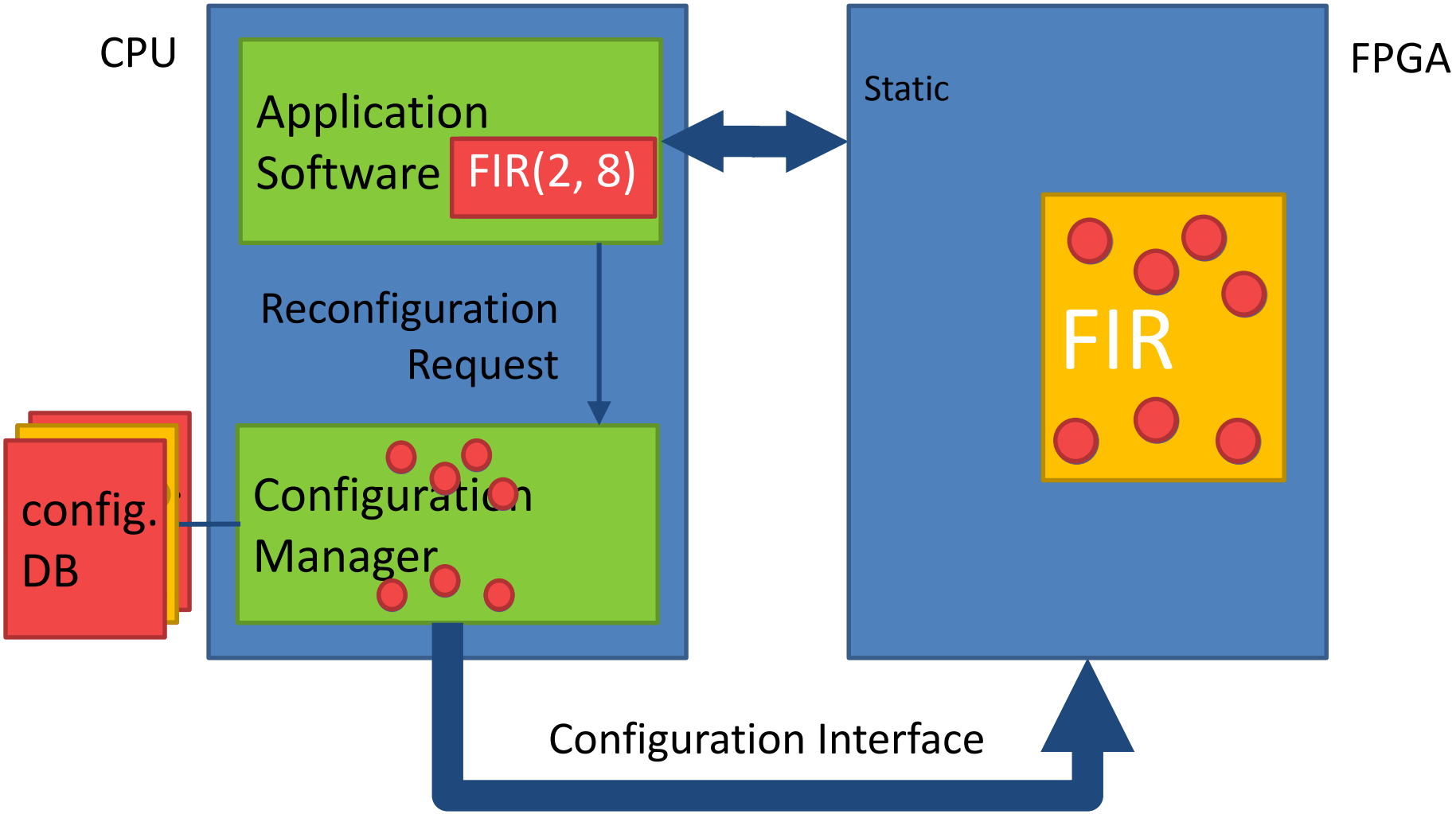
2^{128} possible configurations!

Our solution: Parameterized Configuration

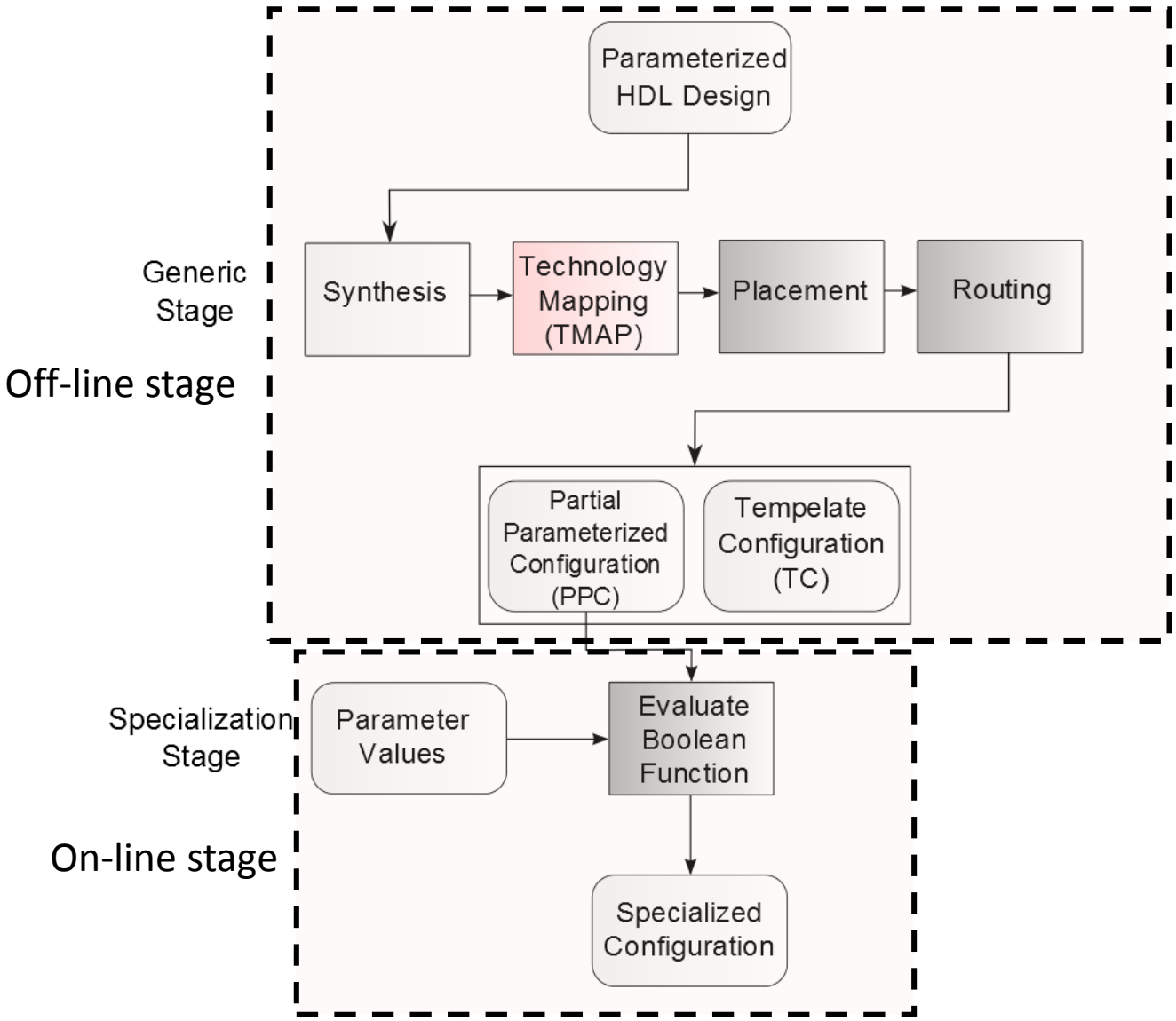


* K. Bruneel and D. Stroobandt, "Automatic Generation of Run-time Parameterizable Configurations," FPL 2008.

Dynamic Circuit Specialization (micro-reconfiguration)

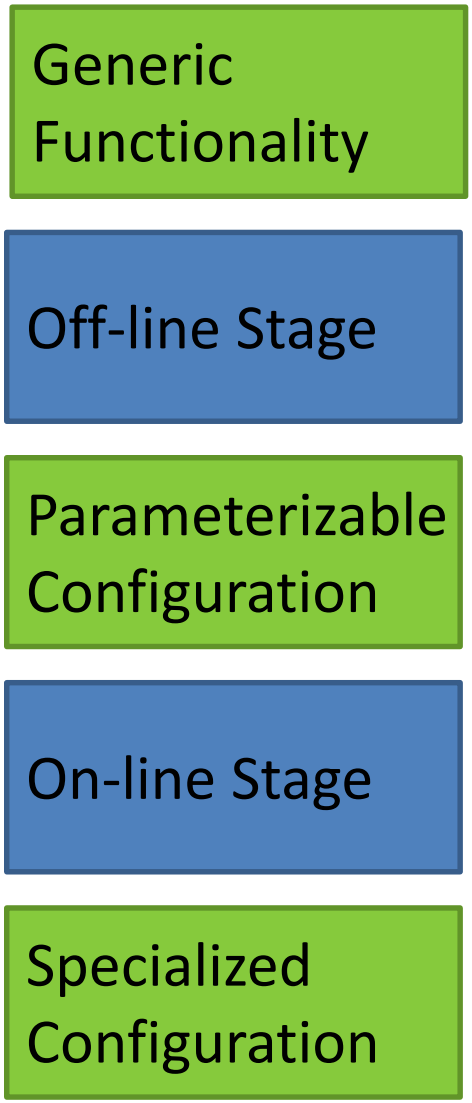


Tool flow

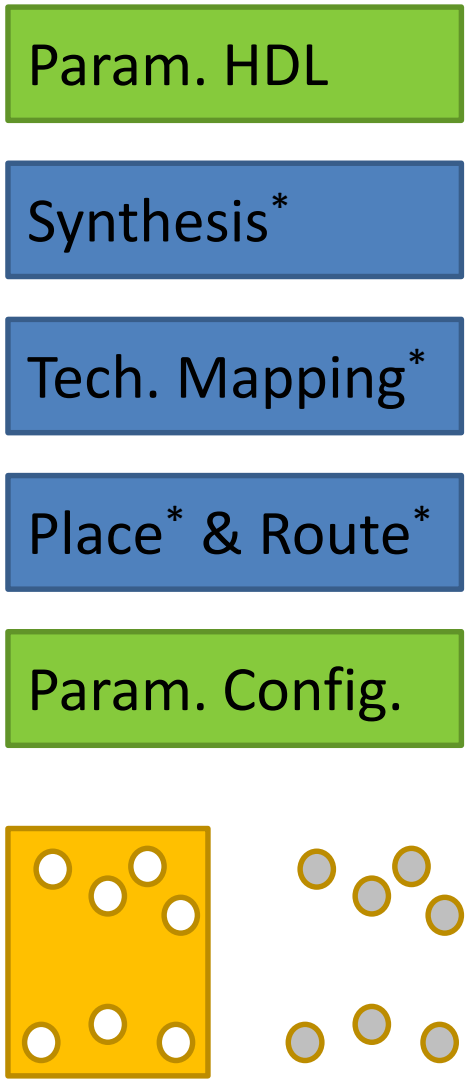

Parameterized HDL Design
Generic Stage
Synthesis
Technology Mapping (TMAP)
Placement
Routing
Off-line stage
Partial Parameterized Configuration (PPC)
Tempelate Configuration (TC)
Specialization Stage
Parameter Values
Evaluate Boolean Function
On-line stage
Specialized Configuration

Two stage approach

- Off-line stage:
  - In: **Generic functionality**
    - Specification of the generic functionality
    - Distinction regular and parameter inputs
  - Out: **Parameterizable Configuration**
    - Software function
    - outputs specialized configurations for given parameter values
- On-line stage:
  - Evaluate parameterizable configuration
  - Out: **Specialized Configuration**
  - **Repeat** every time parameters change



Param. Configuration Tool Flow



- **Tunable truth table** bits
  - Adapted Tech. Mapper: TMAP
  - Map to Tunable LUTs (TLUTs)
  - [FPL2008], [ReConFig2008], [DATE2009]
- Tunable routing bits
  - Adapted Tech. Mapper
  - Adapted Placer
  - Adapted Router

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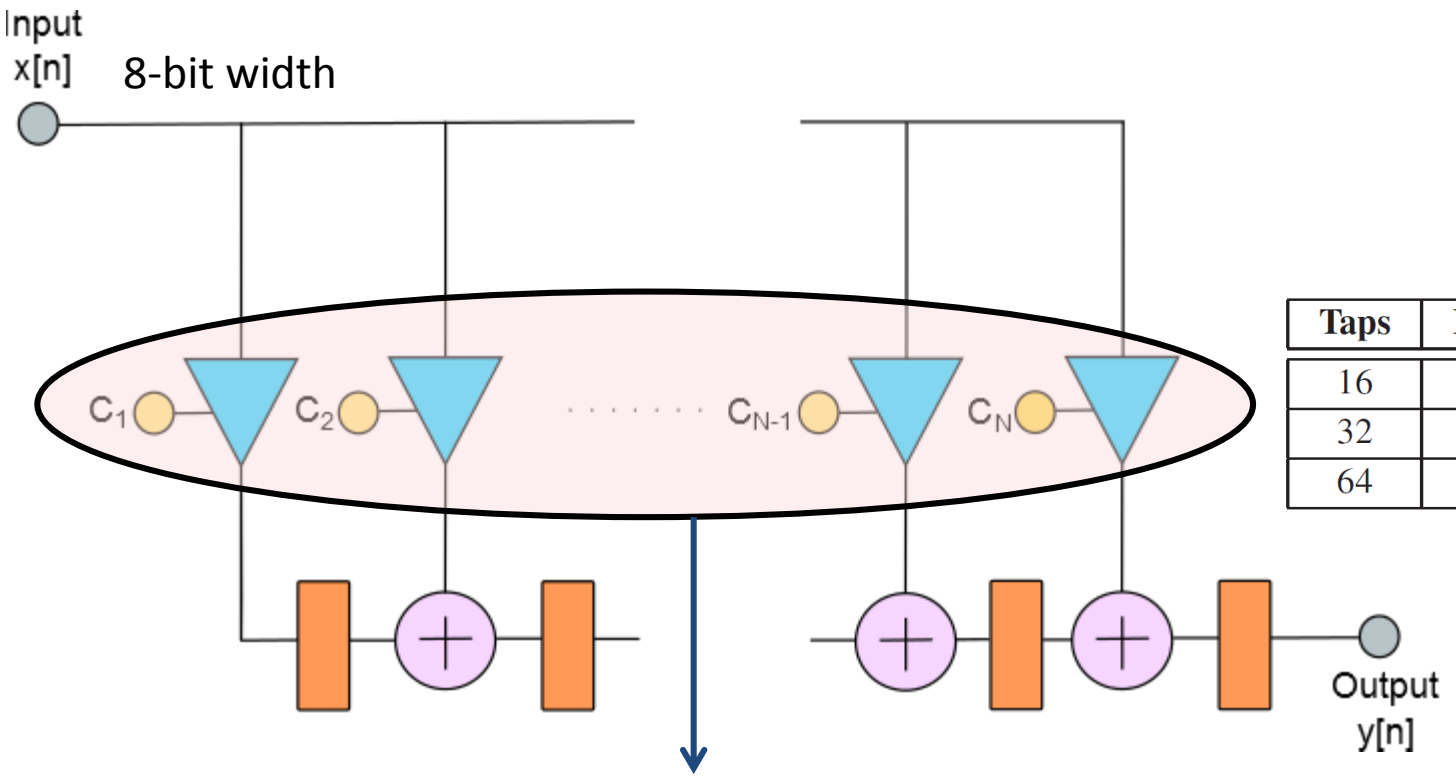
FIR filter as a Parameterized design



Taps	Multipliers	TLUTs
16	32	384
32	64	768
64	128	1536

Multipliers of each TAP are parameterized
Each tap has two 4-input multipliers

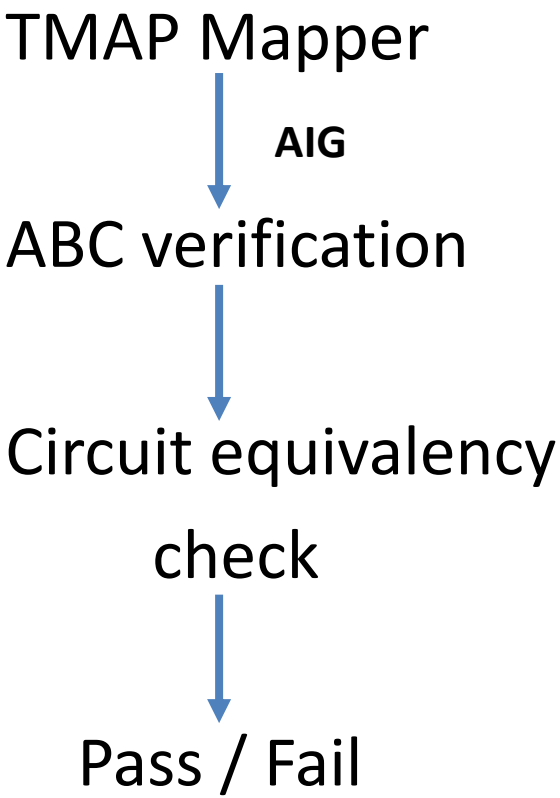
Experiment: 16-tap FIR, 8-bit coefficients

	Generic	**Parameterizable configuration**	**Specialized**
area (LUTs)	2999	**1301 (-56%)**	1146
clock freq. (MHz)	84	**115 (+37%)**	119
gen. time (ms)	0	**0.166**	35634
memory (kB)	0	**29**	2^{128} conf.

[illegible] (5 orders)

- [illegible]
- [illegible]

Formal verification



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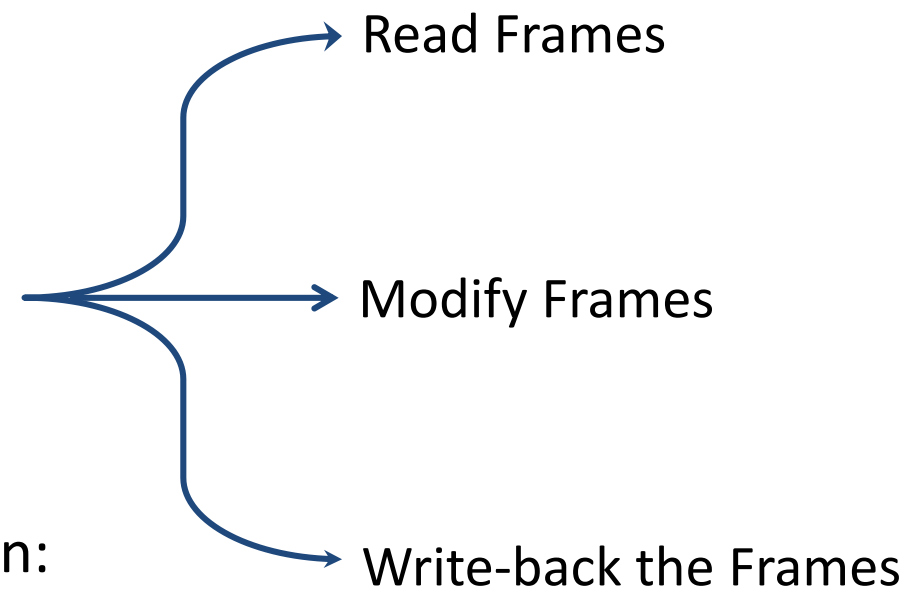
Microreconfiguration Process

Custom HWICAP driver function

XhwIcap_Custom_setClb_bits ( );



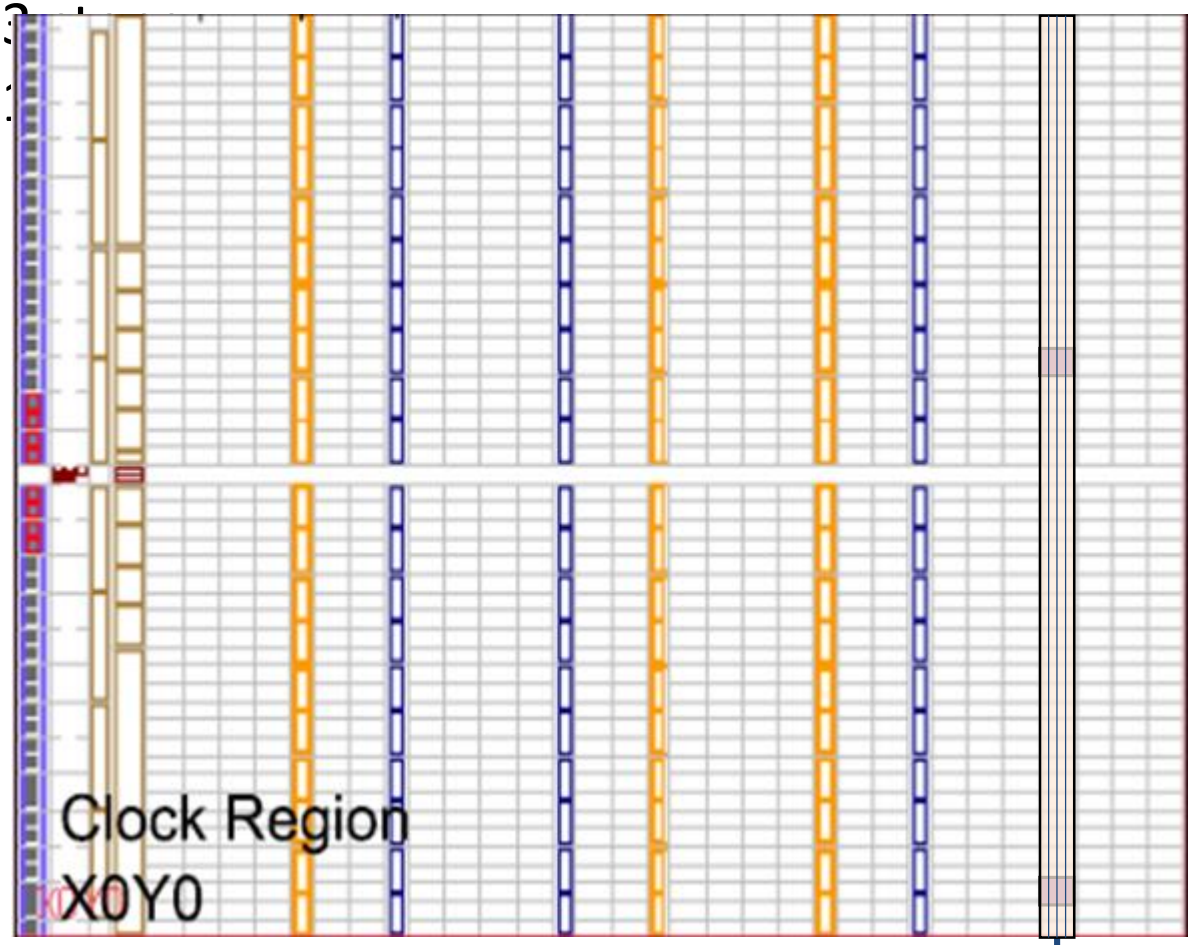
Crucial inputs to the function:

1) Location co-ordinates of a LUT

2) Truth table entries of the LUT

Reconfiguration Process

Read frames



Write-back the Frames

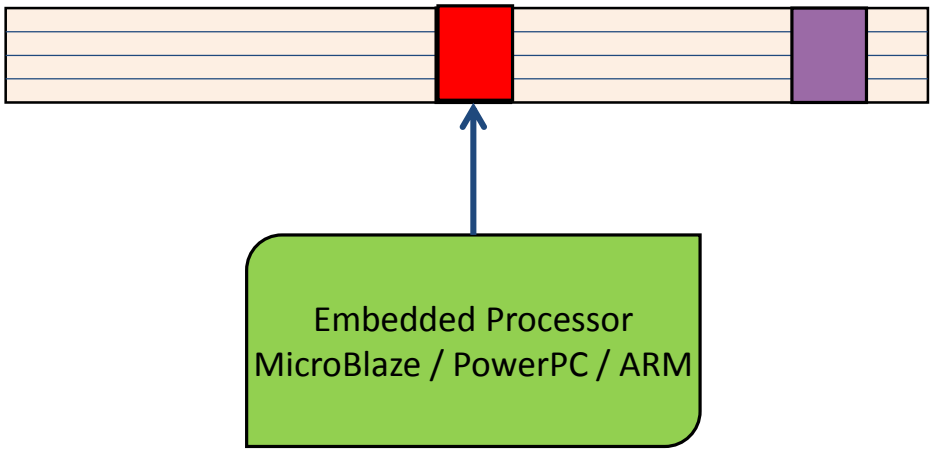
Embedded Processor
MicroBlaze / PowerPC / ARM

HWICAP

Reconfiguration Process

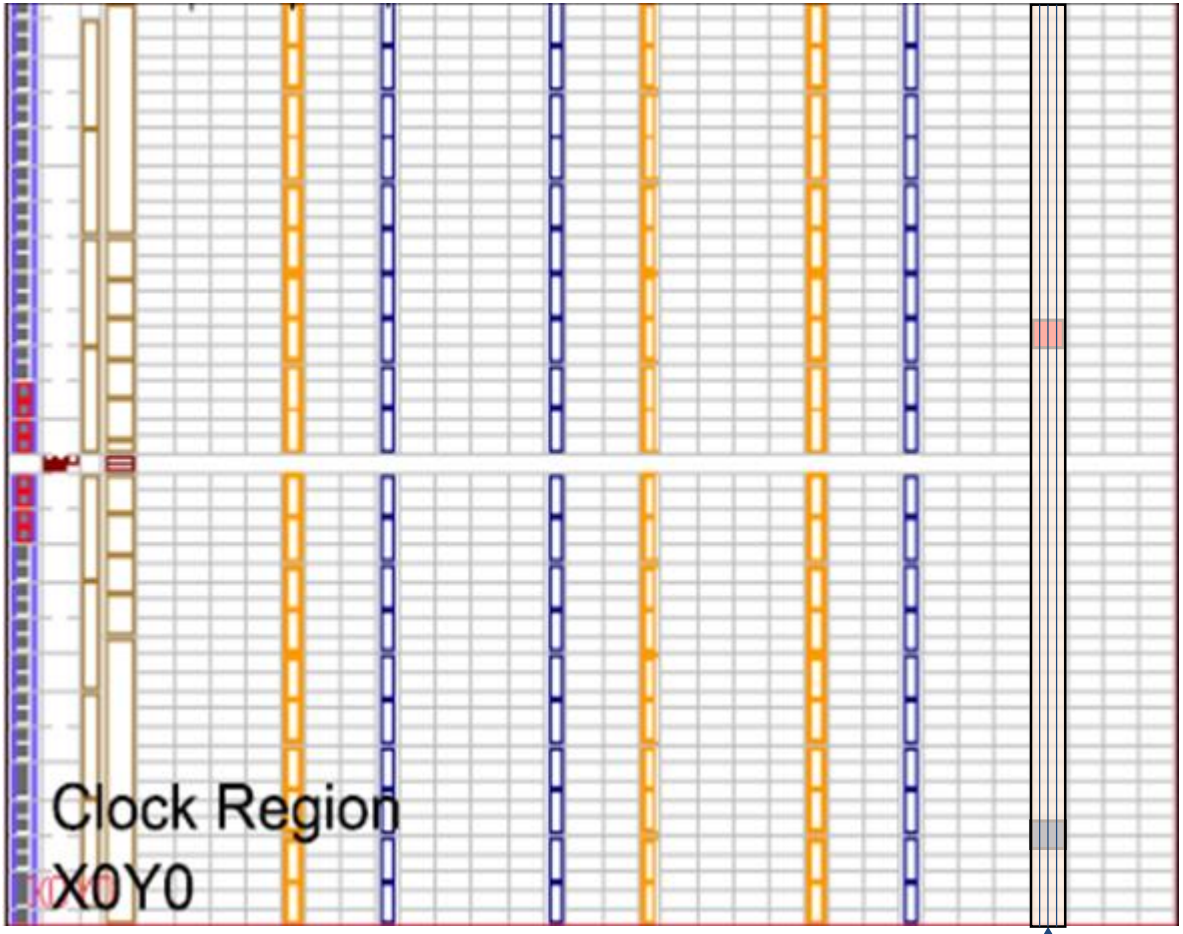
Modify frames

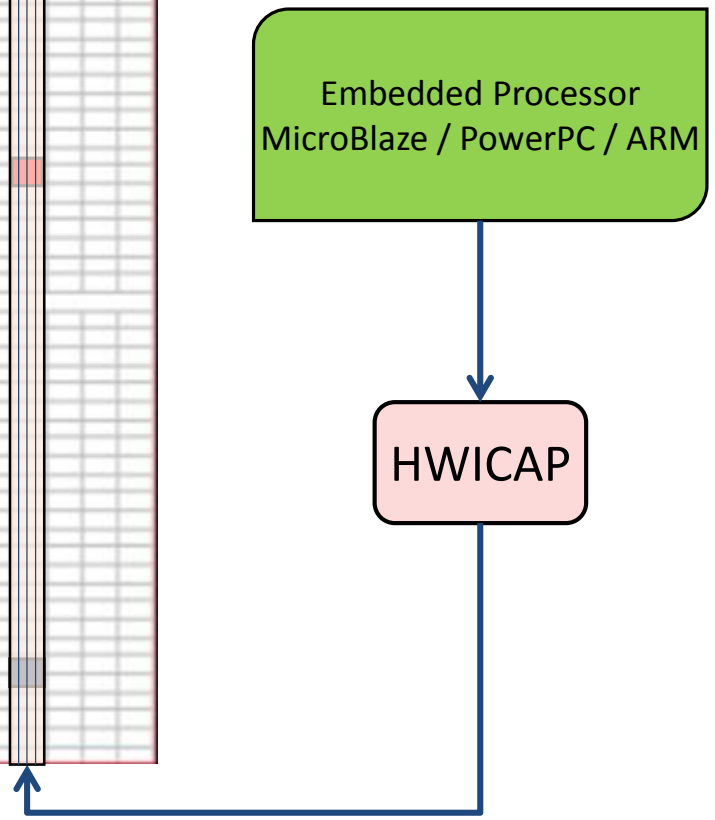
Reconfigure single TLUT



Reconfiguration Process

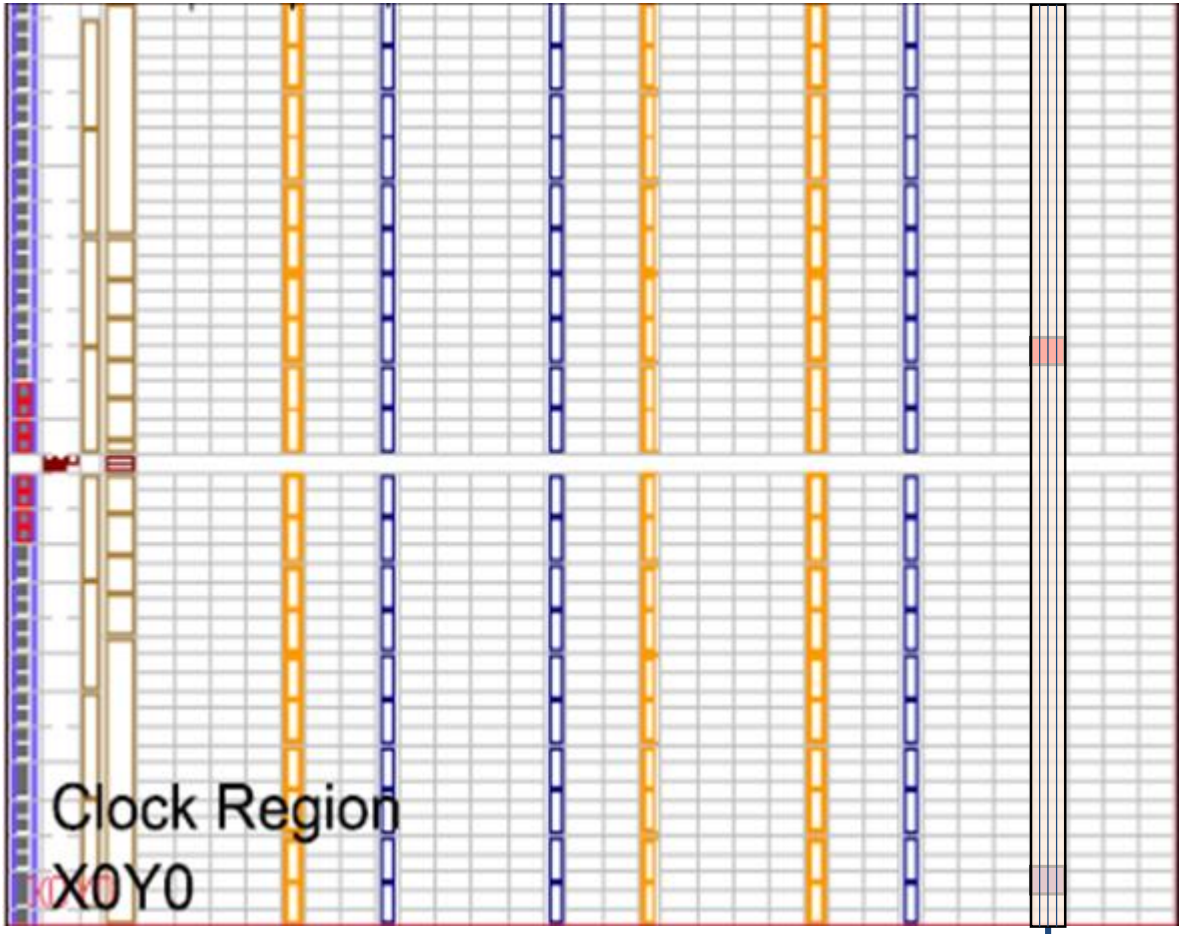
Write back the frames

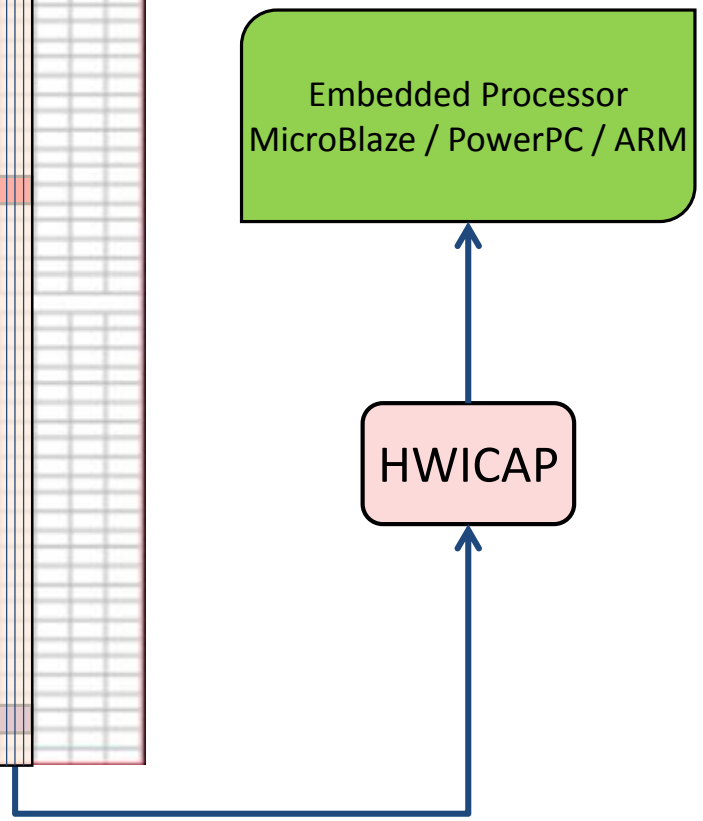




Reconfiguration Process

Read frames

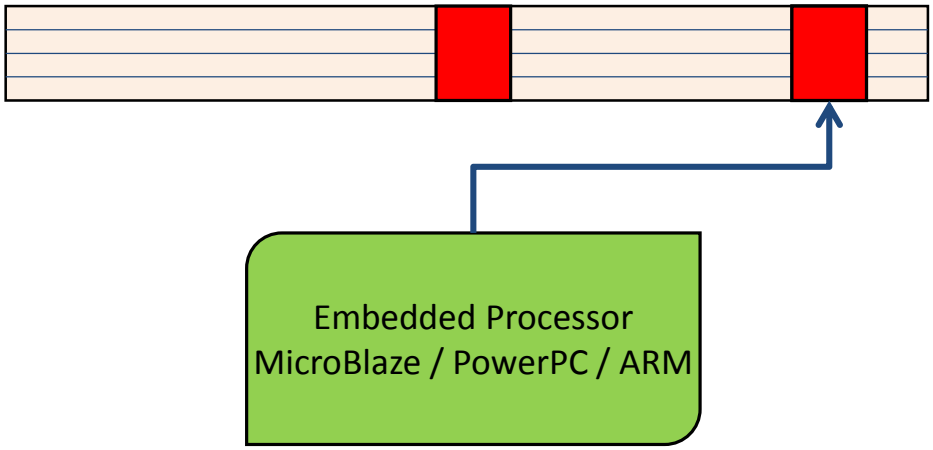




Reconfiguration Process

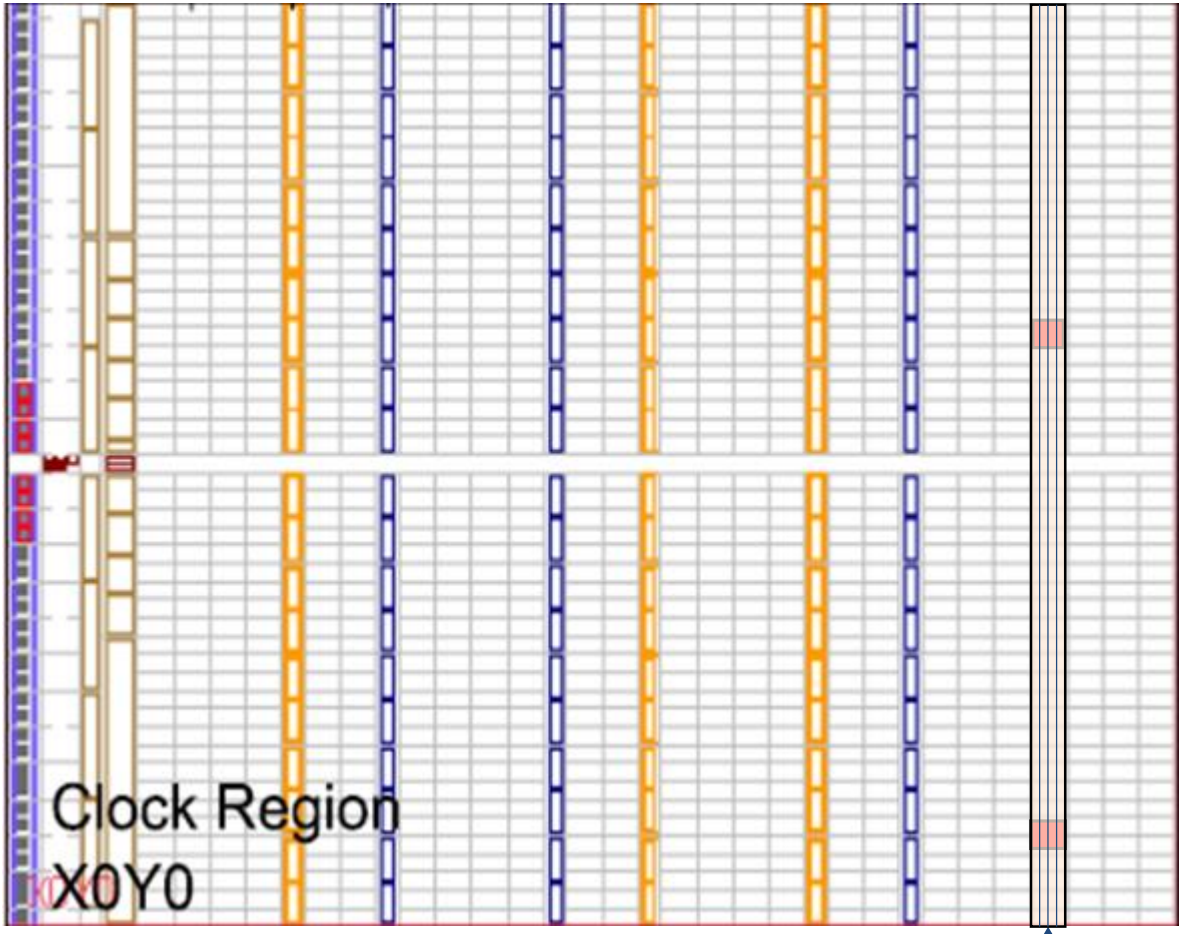
Modify frames

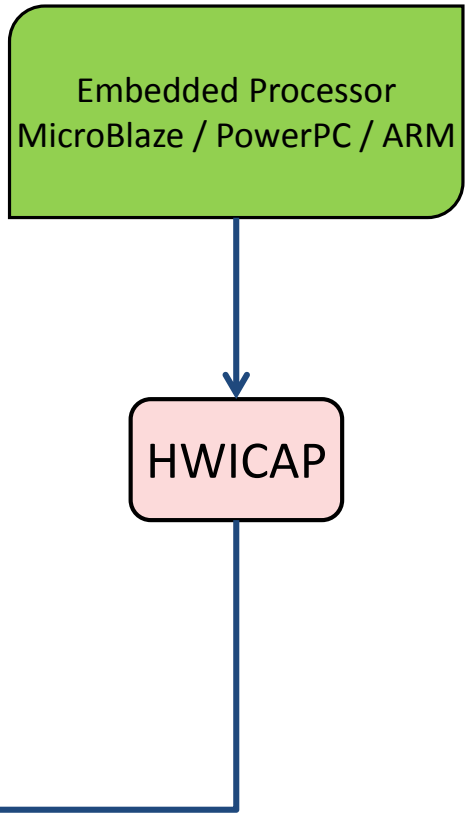
Reconfigure single TLUT



Reconfiguration Process

Write back the frames





Call **XhwIcap_Custom_setClb_bits ( );** to reconfigure every TLUT

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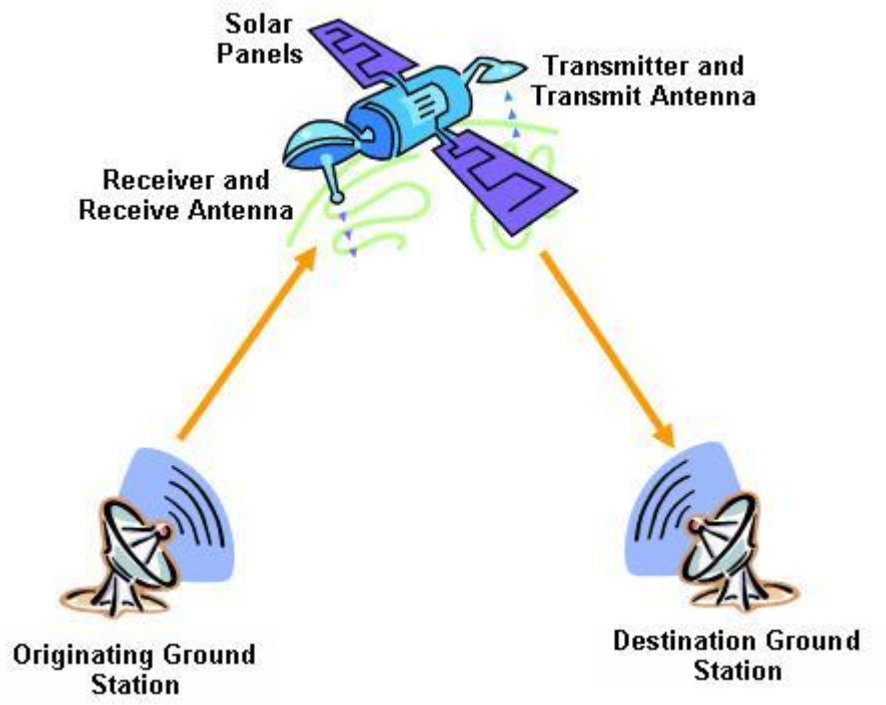
Microreconfiguration for a Satellite

- Tune the filters according to the conditions
  - Microreconfigure the satellite filters (if tuning is needed)
- Micro-Scrubbing
  - Microreconfiguration for minimal frame scrub
  - Adv: less memory to store the golden bits and faster reconfiguration

Surface to Air transmission



- Minimal data Tx from the surface
- Minimal encryption and decryption cost
- Faster Tx due to small amount of data bits

Last slide

- Much of this work was done in the framework of the EU-FP7 project FASTER and is now continued in the EU-H2020 project (FETHPC) EXTRA

- Tools at https://github.com/UGent-HES/tlut_flow

- More information: http://hes.elis.ugent.be/

- Questions?

- THANK YOU