RESOURCE-EFFICIENT DEBUGGING CORE

TO EVALUATE FPGA DESIGNS IN ON-BOARD PROCESSORS

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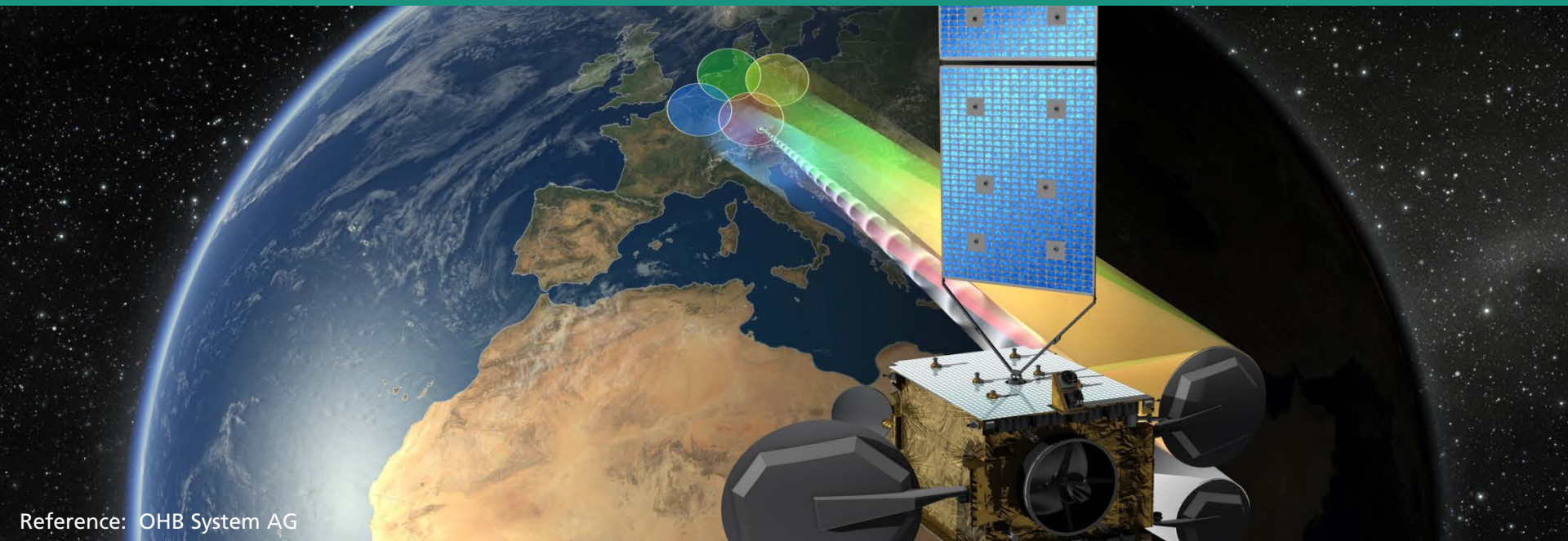

Reference: OHB System AG

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Abstract

Modern SRAM-based FPGAs improve on-board processing (OBP) in space applications through dynamic reconfiguration of the firmware. This provides flexibility and adaptability for new communication experiments. An example for such a novel signal processing platform is the *Fraunhofer On-Board Processor* (FOBP), located in the scientific payload part of the *Heinrich Hertz* satellite mission, with two space-grade *Virtex-5QV*. Nevertheless, in-orbit verification (IOV) of new firmware experiments comes with the price of reduced debugging possibilities. While on-ground debugging enables to use different tools and methods to access the FPGA, in-space debugging (ISD) restricts this direct access. To solve this problem, we present an ISD core which acts as an interface inside the FPGA to debug firmware signals by an user on earth. The result is a wireless remote access of the FPGA with the possibility of tracing signals and controlling the firmware. We use a virutal telemetrie/telecommand (vTM/TC) link within the user-band to transmit or receive debugging data.

We focus a resource-efficient approach based on a VHDL concept and consider flexibility for adaptions and improvements. The concept contains a trigger unit, a read-in module for user data sampling, a memory block for the data storage and a read-out module to connect the ISD core with the vTM/TC. For the first proof of concept, the implementation is reduced to the TX part (capture debug data of a user logic module).

We use a typical setup (8 bit data width, 4096 sampling depth) to verify the functionality of the ISD core. The resource consumption results in less than a half percent flip-flops (FFs), look-up tables (LUTs) and BRAM compared to all usable *Virtex-5QV* resources. If we choose a setup with higher data width or sampling depth, the BRAM consumptions appropriately increases while the increase of FFs and LUTs are negligible. We analyzes the essential bits of the ISD core and the mentioned setup uses only 0.1 % essential bits.

The presented resource-efficient ISD core is able to improve the IOV of new firmware-experiments in FPGA-based OBPs. A debug-unit on the ground is necessary to depacketize, visualize and analyze the debug data. Furthermore, a combination with an BRAM radiation sensor provides additional information about the space whether and allows a categorization of the debug data.