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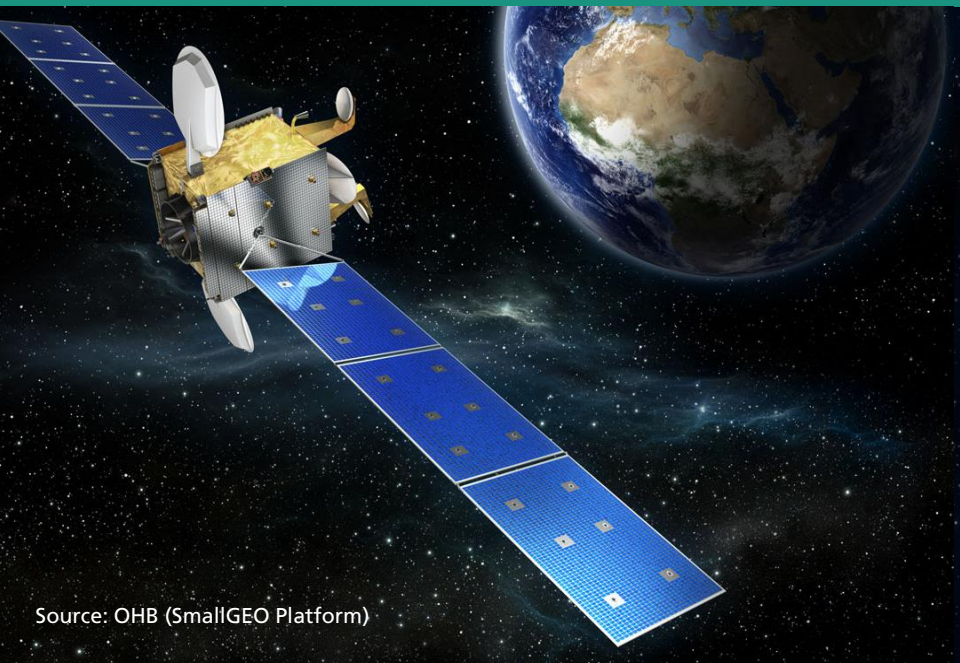
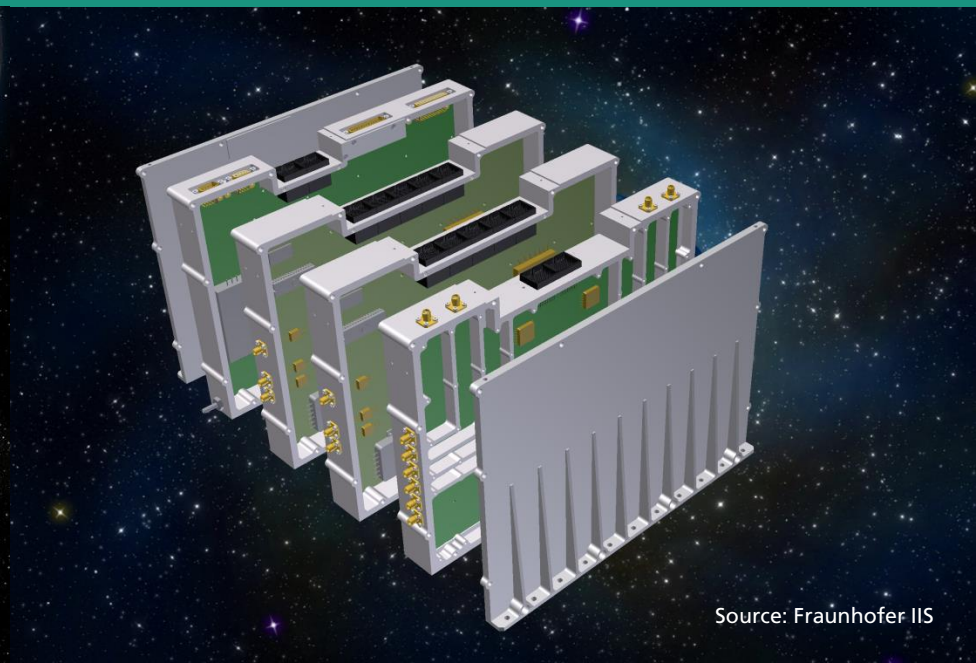
Fast In-Orbit FPGA Reconfiguration via In-Band TM/TC

Christopher Stender, March 17th, 2016

SpacE FPGA Users Workshop, 3rd Edition, Noordwijk



Source: OHB (SmallGEO Platform)



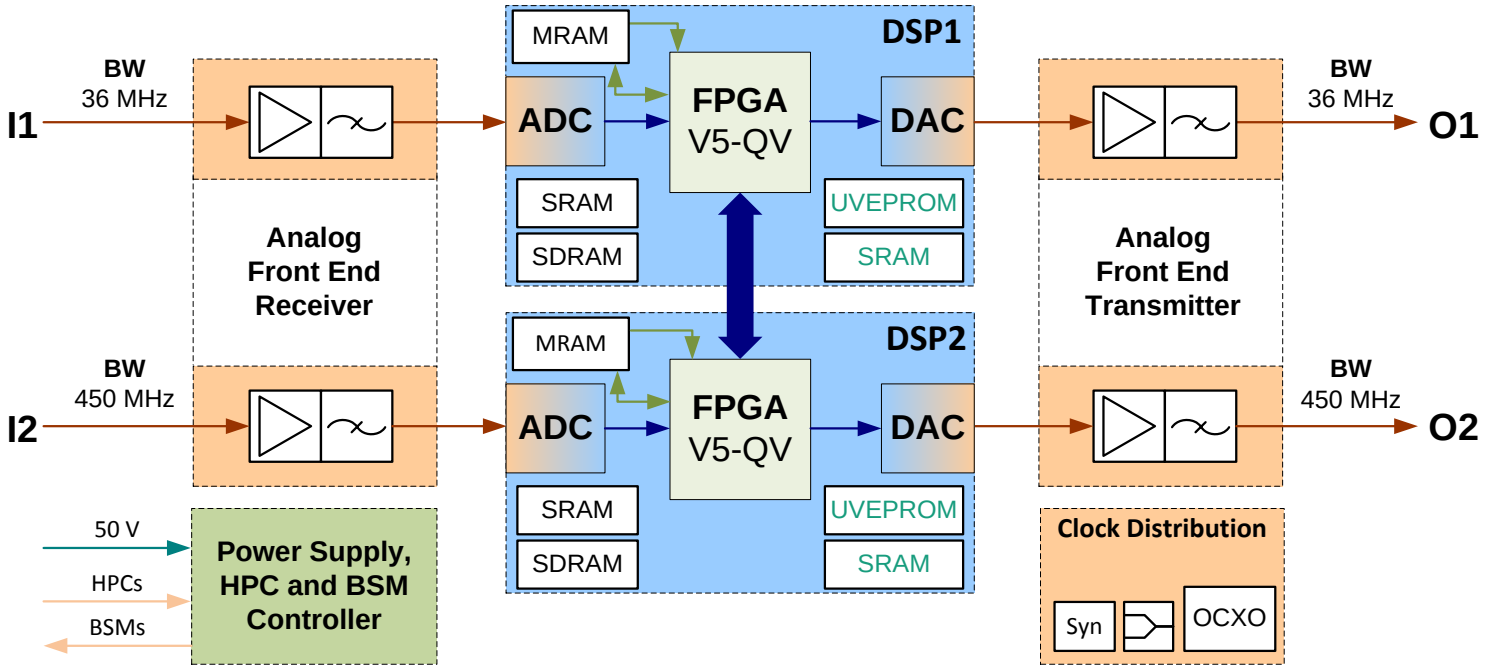
Source: Fraunhofer IIS

AGENDA

- Motivation
- In-Band TM/TC Communication Link
  - Features
  - Layer Overview
- FPGA Reconfiguration
  - Design Overview
  - Bootstrapping
- Implementation Results
  - Performance
  - Resources
- Conclusion & Outlook

Motivation
Fraunhofer On-Board Processor (FOBP)

- FOBP on the Heinrich Hertz-Satellite is part of the scientific IOV payload
- Regenerative transponder with two reconfigurable Virtex-5QV FPGAs
- Variable component for performing in-orbit experiments



[1] *In-Orbit Verification (IOV)*

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Motivation
Limitations when using the Satellite's TM/TC[1] Link

- Time-consuming upload of new FPGA designs
  - Virtex-5QV bit file size is about 6 MiB
  - Several design uploads per day
  - FOBP is not powered permanently → FPGA designs need to be uploaded again after a power cycle
- Strict implementation & verification requirements regarding the payload interface to the flight computer
- Inflexible → fixed or at least limited data rates
- No real-time link access

[1)] *Telemetry/Telecommand (TM/TC)*

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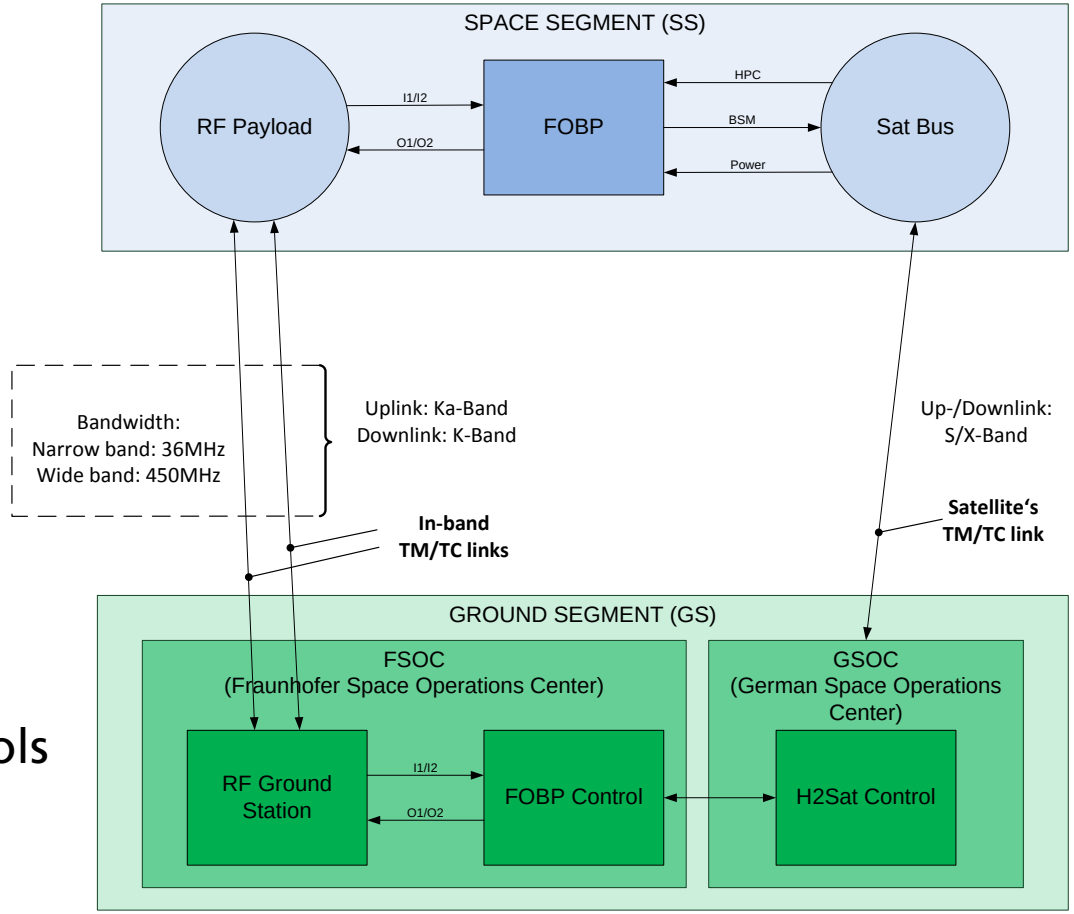
In-Band TM/TC Communication Link
Introduction

- **Goal: Establish an in-band TM/TC communication link**

- Requirements
  - ~1 Mbit/s data rate
  - Reliable transmission
  - Virtual channels with different priority
  - Based on established communication protocols
  - Easy to use in software



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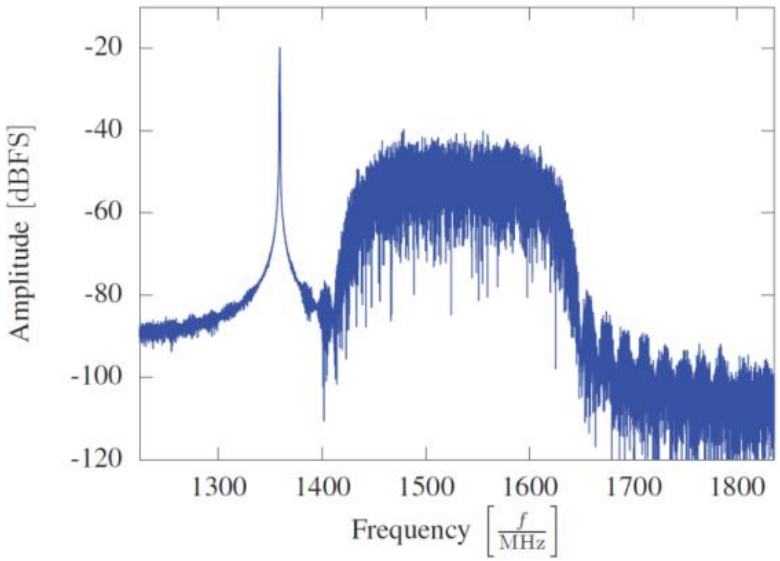
In-Band TM/TC Communication Link
Implementation Overview

- Requirements
  - ~1 Mbit/s data rate
  - Reliable transmission
  - Virtual channels with different priority
  - Based on established communication protocols
  - Easy to use in software

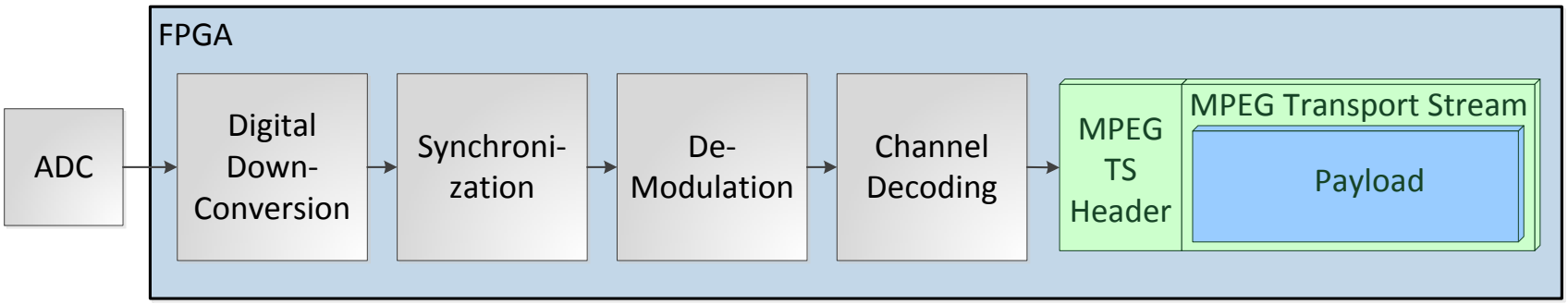
- 2 MHz bandwidth
- DQPSK[1] modulation
- Root-raised-cosine roll-off 1.0
- Code rate 0.46
- Link budget → 99.9% availability
- Channel coding
- MPEG Transport Stream
- TCP/IP
- Ethernet (IEEE 802.3)
- Unidirectional Lightweight Encapsulation (ULE)

[1)] *Differential Quadrature Phase-Shift Keying (DQPSK)*

In-Band TM/TC Communication Link
Physical Layer



- 2 MHz bandwidth
- DQPSK modulation
- Channel coding
  - Reed-Solomon
  - Convolutional coding
- Interface to the data link layer: MPEG Transport Stream



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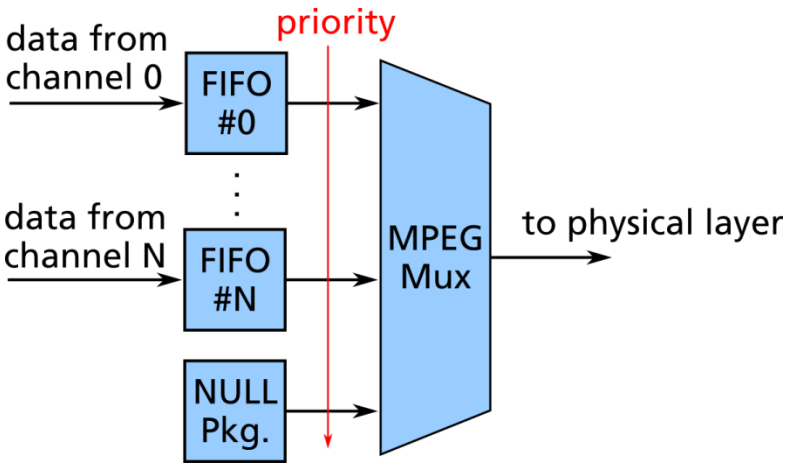
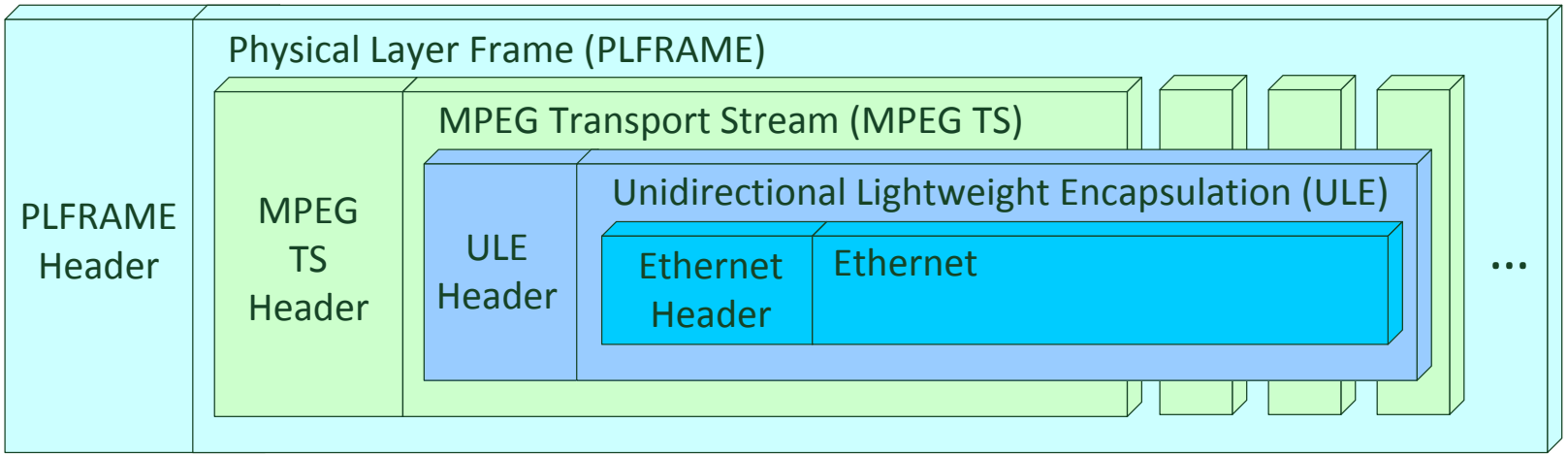
In-Band TM/TC Communication Link
Data Link Layer

- Ethernet frames are encapsulated into MPEG-TS packets using Unidirectional Lightweight Encapsulation (ULE)
- Priorization in hardware (VHDL)
- Encapsulation in software (C)





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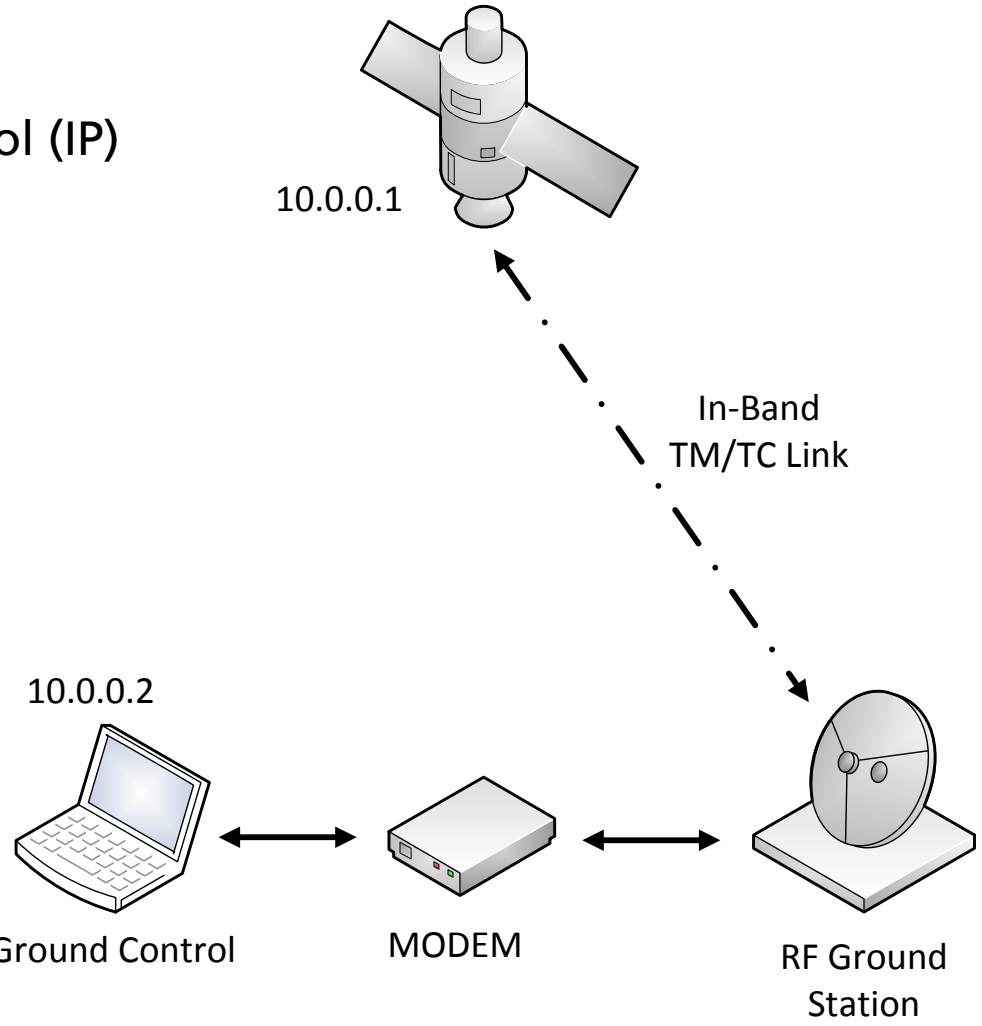
In-Band TM/TC Communication Link
Network, Transport and Application Layer

- Network Layer: Internet Protocol (IP)
- Transport Layer
  - Periodic updates: UDP
  - Reliable transfers: TCP
- Application Layer
  - FTP[1] for bit file uploads
  - SNMP[2] for monitoring
  - Telnet for telecommands
  - …



[1] File Transfer Protocol (FTP) [2] Simple Network Monitoring Protocol (SNMP)

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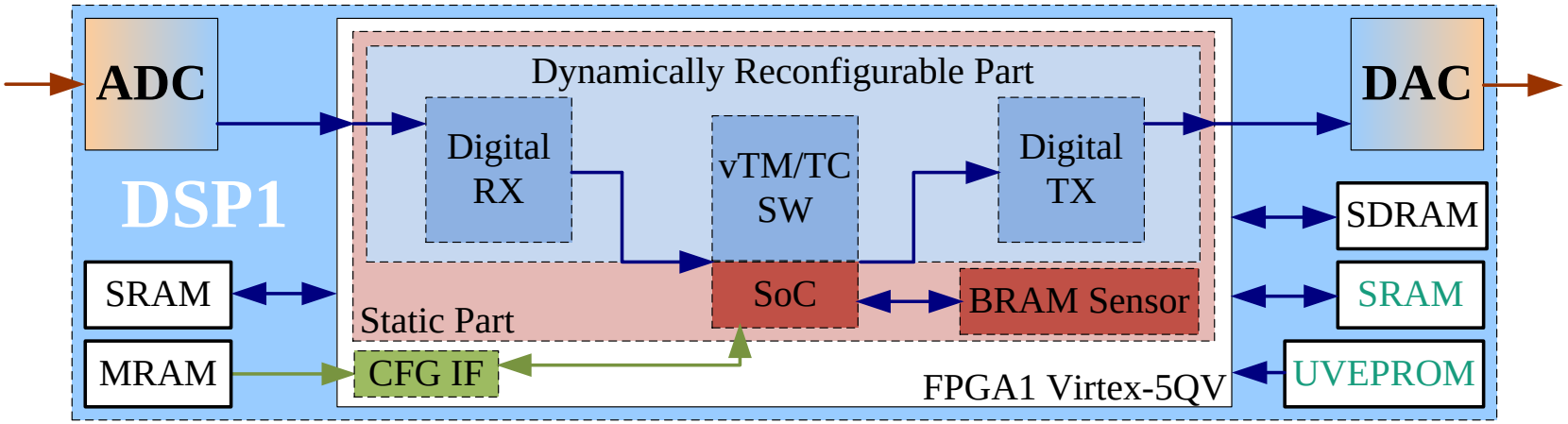
FPGA Reconfiguration
Design Overview

- TM/TC communication link is completely implemented in a Virtex-5QV
  - Lower layers are realized in the FPGA fabric
  - Higher layers are realized as software running on a LEON3FT-SoC[1]
- FPGAs can reconfigure themselves / each other via the LEON3FT-SoC
  → no external configuration controller required



[1] *System-on-Chip (SoC)*

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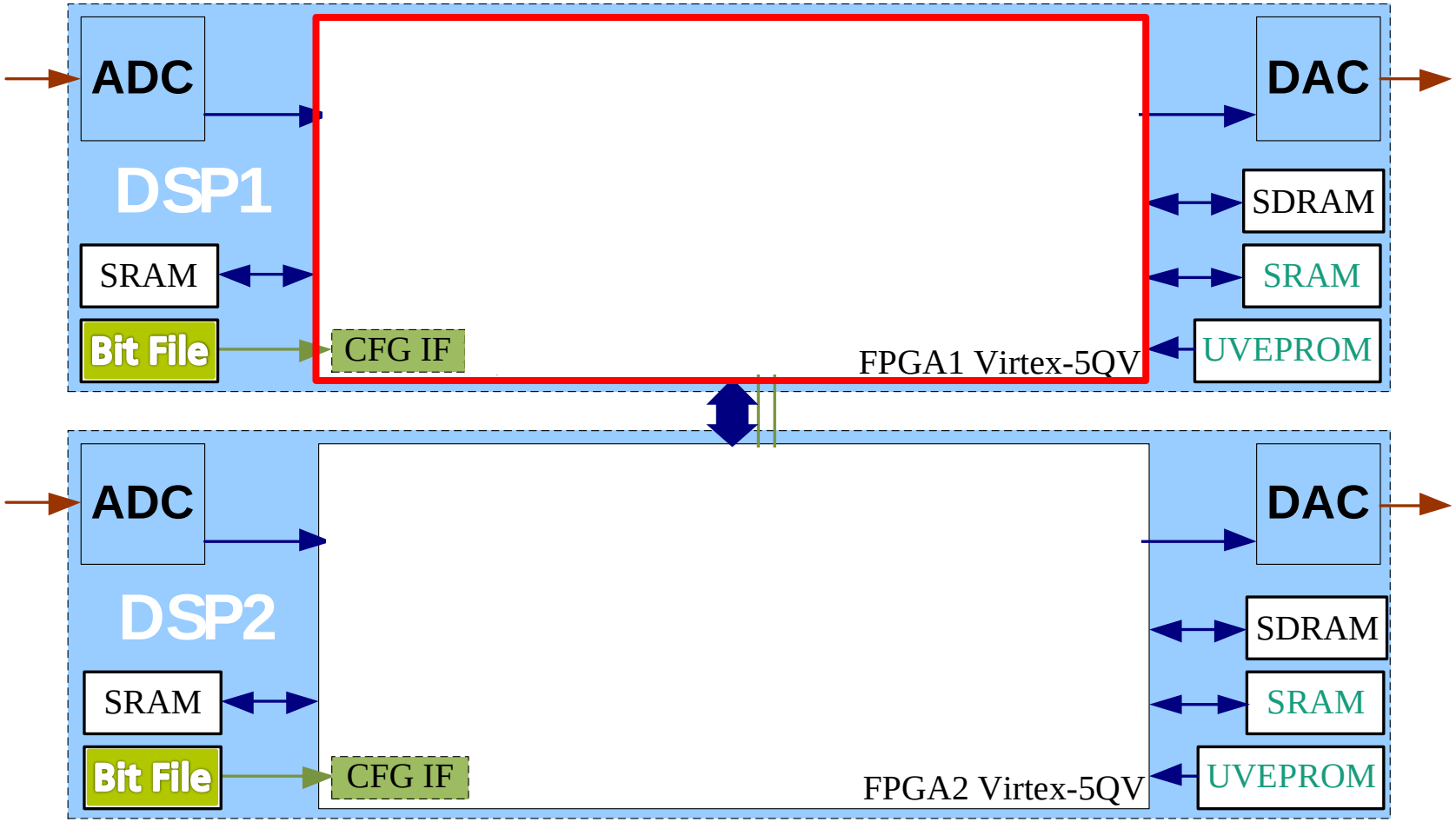
FPGA Reconfiguration
LEON3FT-SoC

- LEON3FT-SoC
  - Fault-tolerant 32-bit SPARC V8 microprocessor (51 MHz clock)
  - 256 MiB SDRAM
  - I/O memory interface to the
    - Internal Configuration Access Port (ICAP)
    - SelectMAP configuration interface of the other FPGA
- Software stack
  - RTEMS 4.11 with a TCP/IP stack
  - Network driver with support for ULE and MPEG-TS
  - Bit file manager (can store and manage multiple bit files)

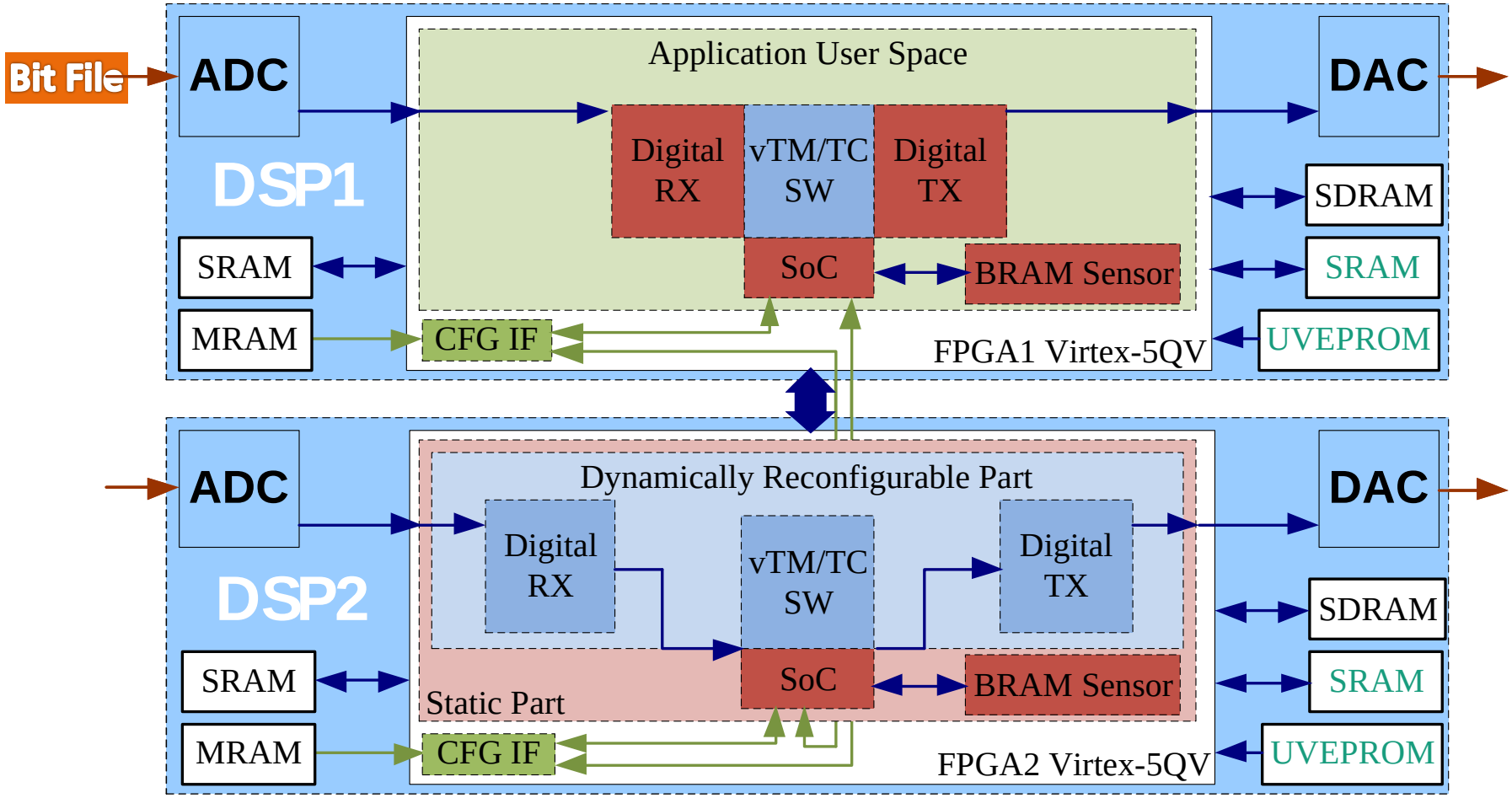
FPGA Reconfiguration

Initial Configuration and Master Determination



FPGA Reconfiguration

Master FPGA Reconfiguration (Bootstrapping)



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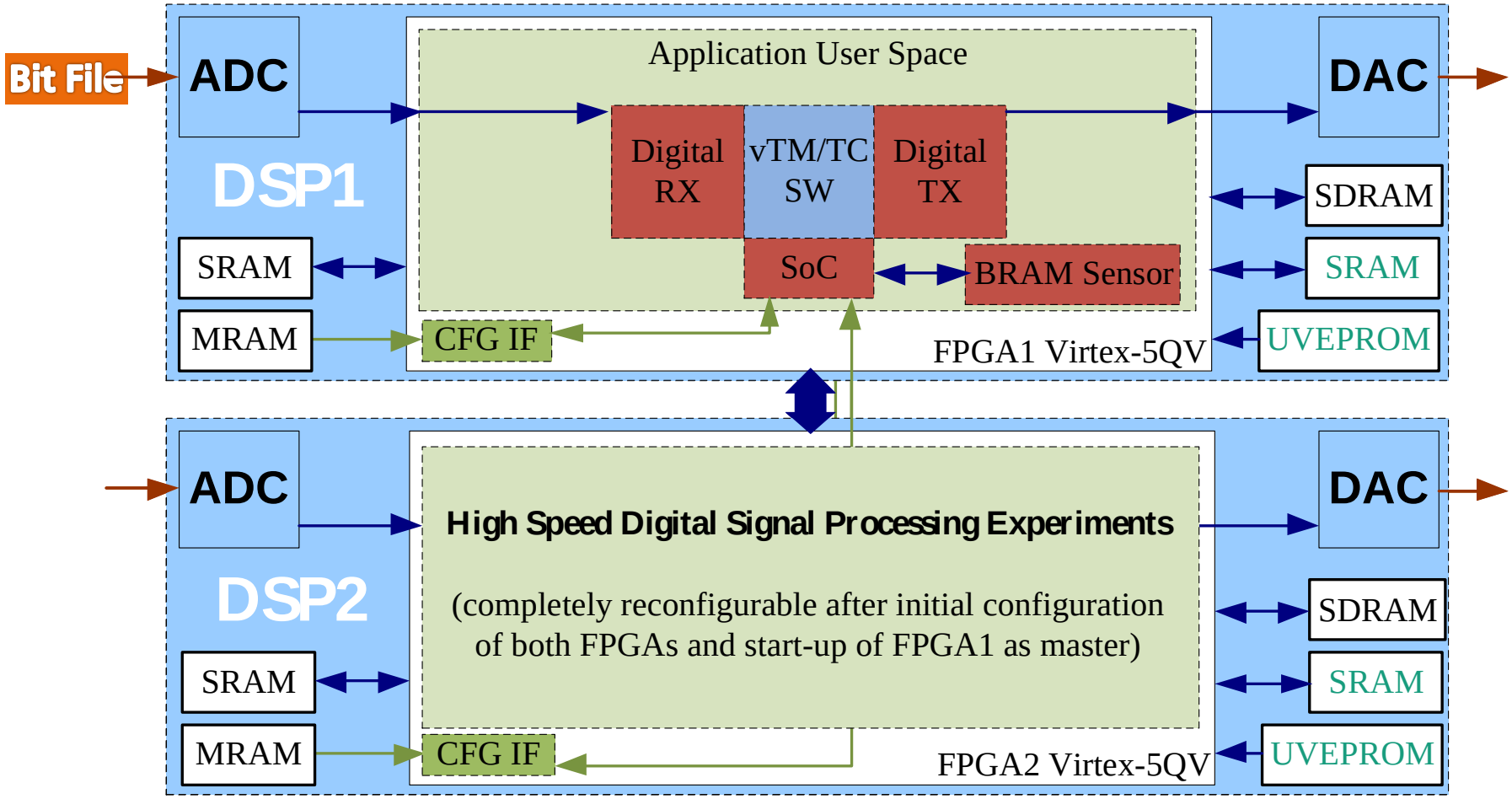
FPGA Reconfiguration

Slave FPGA Reconfiguration (Experiment Loading)



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Implementation Results
Link Performance and FPGA Reconfiguration Time

- Link performance
  - Bandwidth: 2 MHz
  - Availability: 99.9 %
  - TCP throughput: ~0.85 Mbit/s
  - Round-trip time (RTT): 265 ms[1]

- FPGA reconfiguration time
  - Bit file upload (6 MiB): ~57 s
  - Bit file upload (3.5 MiB): ~33 s
  - Reconfiguration: < 1 s

[1] *incl. 250 ms emulated GEO round-trip delay*

Implementation Results
FPGA Resource Utilization and Memory Usage

- FPGA Design

Module	LUT		FF		BRAM		DSP	
Available	81920		81920		298		320	
LEON3FT	15301	19 %	5378	7 %	14	5 %	4	1 %
TM/TC	11731	14 %	11382	14 %	6	2 %	111	35 %
Monitoring	1064	1 %	498	1 %	4	1 %	0	0 %
CRM[1]	139	0 %	104	0 %	0	0 %	0	0 %
CAM[2]	504	1 %	386	0 %	4	1 %	0	0 %
Sum	**28739**	**35 %**	**17748**	**22 %**	**28**	**9 %**	**115**	**36 %**

- Memory usage for the LEON3FT-SoC software
  - Binary size: 480 KiB
  - Working memory: 8 MiB (without bit file manager)

[1] Clock and Reset Management (CRM) *[2] Configuration Access Module (CAM)*

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Conclusion & Outlook

- **Problem:** Satellite's TM/TC link is limited in terms of data rate and real-time access → Drawback when dealing with large FPGA bit file uploads.
- **Solution:** In-band TM/TC link for fast FPGA reconfiguration based on IP
  - High throughput and real-time access
  - Scalable
  - Reliable
  - Easy to use
- **Result:** Upload and configuration of an entire new FPGA design in less than a minute
- **Outlook:** Next-Generation Xilinx RT-FPGA provides ~6 times more resources than the Virtex-5QV and include an MPSoC by default → resource utilization for the in-band TM/TC will be less than 3 percent!