Heavy Ion SEE Testing of XC7K70T, Kintex7 family FPGA from Xilinx

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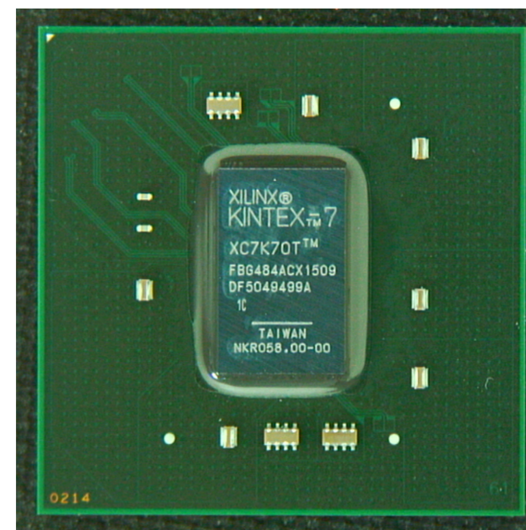
TRAD Tests & radiations

Outline

- Part description
- SEE test constraints
- Test methodology
- Conclusions

Part tested – XC7K70T – Xilinx

PART IDENTIFICATION	
Type :	XC7K70T
Manufacturer :	Xilinx
Process:	28nm
Function :	FPGA
PARTS PROCUREMENT INFORMATIONS	
Packaging :	BGA484 ➔ Flip-chip !



Device	Logic Cells	Configurable Logic Blocks (CLBs)		DSP Slices	Block RAM Blocks			CMT	PCIe	GTXs	XADC Block	I/O Bank	Max User I/O
		Slices	Max Distributed RAM (Kb)		18 Kb	36Kb	Max(Kb)						
XC7K70T	65600	10250	838	240	270	135	4860	6	1	8	1	6	300

SEE constraints

- **SEE testing, what are the constraints ?**
  - **De-capping component**
  - **Facility**
    - Range of ions, LET
  - **Device in functioning**
  - **Type of event**
    - SEL, SEU and SEFI
  - **Dedicated test board (size and compatibility) and test bench**

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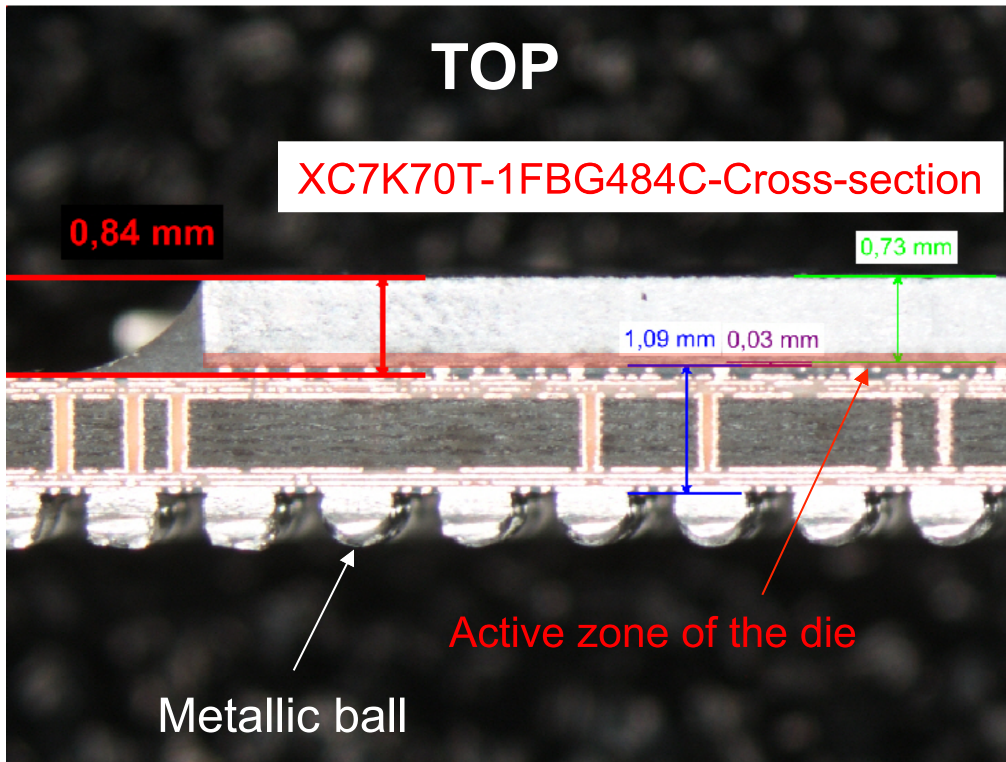
De-capping operation



- Flip chip die
- Die directly interfaced on the PCB package
- Reduce thickness of the die
- High beam range ➔ UCL (73µm)

Tests & radiations

UCL facility

Ion	Energie (MeV)	Range (µm(Si))	LET ($MeV.cm^2.mg^{-1}$)
$^{13}C^{4+}$	131	269.3	1.3
$^{14}N^{4+}$	122	170.8	1.9
$^{22}Ne^{7+}$	238	202	3.3
$^{40}Ar^{12+}$	379	120.5	10
$^{58}Ni^{18+}$	582	100.5	20.4
$^{84}Kr^{25+}$	769	94.2	32.4
$^{124}Xe^{35+}$	995	73.1	62.5

- **The lowest ions range will determine the maximum thickness of the die**
- **25h of beam is plan to be used**

Maximum thickness allowed for this test → 50µm

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TRAD Tests & radiations

Test Bench - Hardware

FPGA Board

USB

PC for storage and visualisation

configuration and output signals

DUT

Power Supply Signals

GUARD SYSTEM

high end modular power supply

Power Supply Signals

GPIB IEEE488

SEL Curves

Current Consumption

SEE constraints

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Single Event Latchup

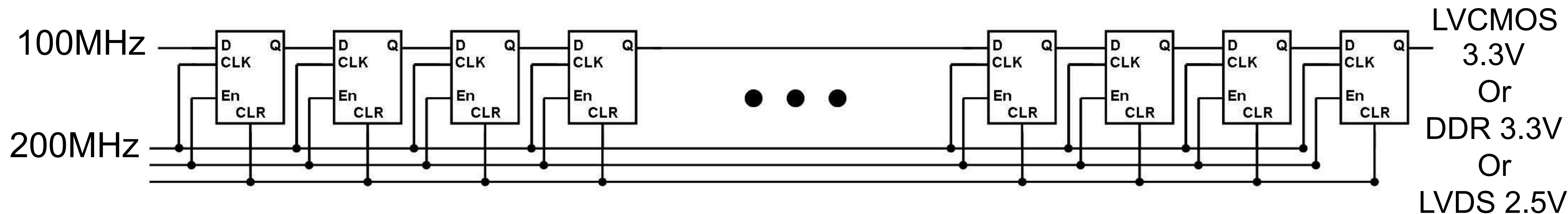
- Temperature will be set at 85°C
  - Monitored with PT1000 and XADC integrated in the DUT
- Each power supplies will be monitored separately with the GUARD Systems and set at maximum voltage if possible (15 power supplies with 3 GUARD systems)
- Dedicated power supply for each power input of the DUT with ramp power-up in order to avoid current peak if Latch-up is observed.
- Flash Memory is used to program the DUT in Byte-wide Peripheral Interface (BPI) configuration mode, in case of latchup or hard reset

Tests & radiations

SEU and SEFI

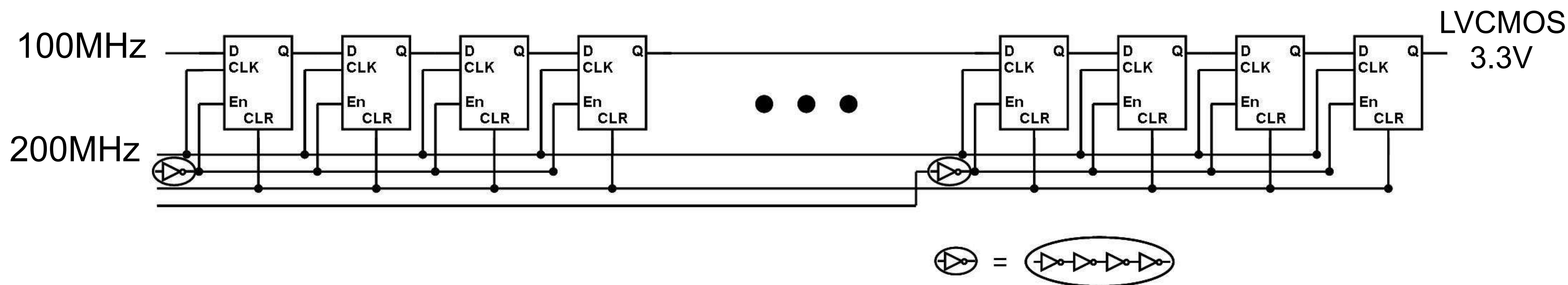
- **Two different designs :**
  - **Shift registers and block memory**
  - **Typical space application :**
    - Interest for spacecraft payload or platform
    - Must present a sufficient complexity to necessitate a Kintex 7 FPGA
    - Failures linked to soft errors must be easy to interpret

Shift Register chain



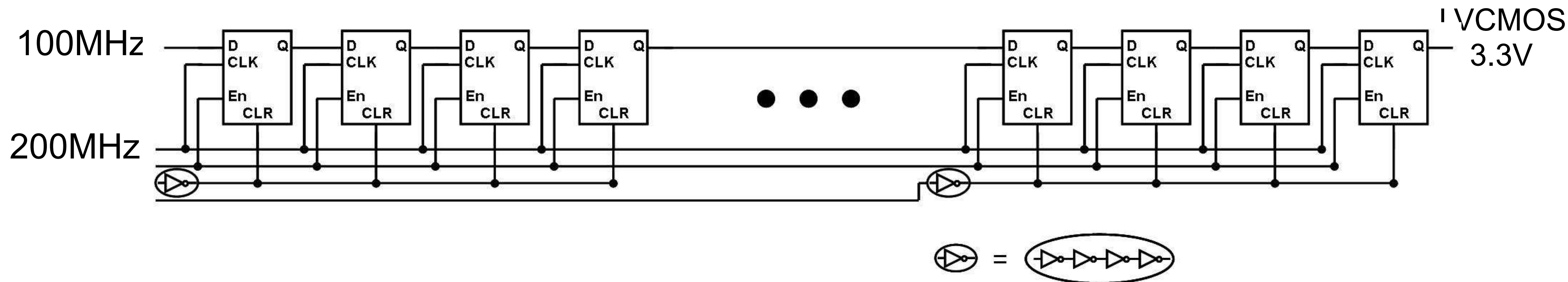
- Input clock 200MHz
- Input Data 100MHz
- 3 different Output chains, LVCMOS, DDR and LVDS

Shift Register chain



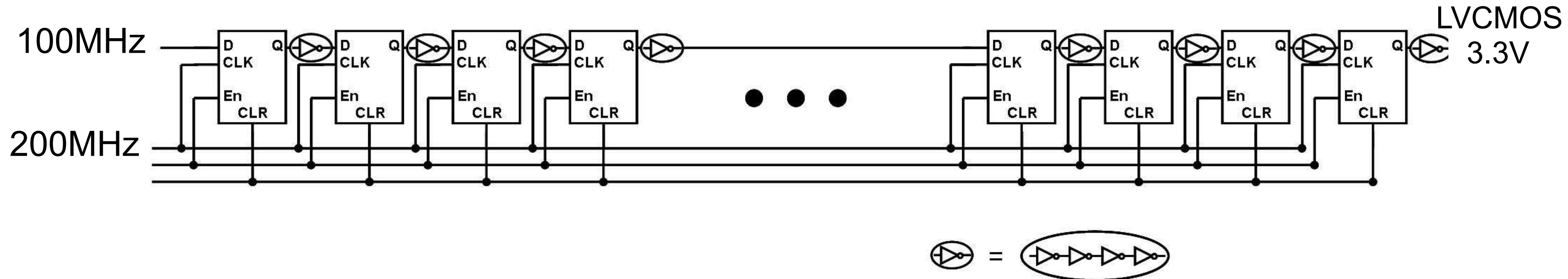
- Input clock 200MHz
- Input Data 100MHz
- Layers of combinational logic made of 4 inverters on the Enable path

Shift Register chain



- Input clock 200MHz
- Input Data 100MHz
- Layers of combinational logic made of 4 inverters on the Clear pin path

Shift Register chain



- Input clock 200MHz
- Input Data 100MHz
- 4 inverters between the output and the next input

TRAD Tests & radiations

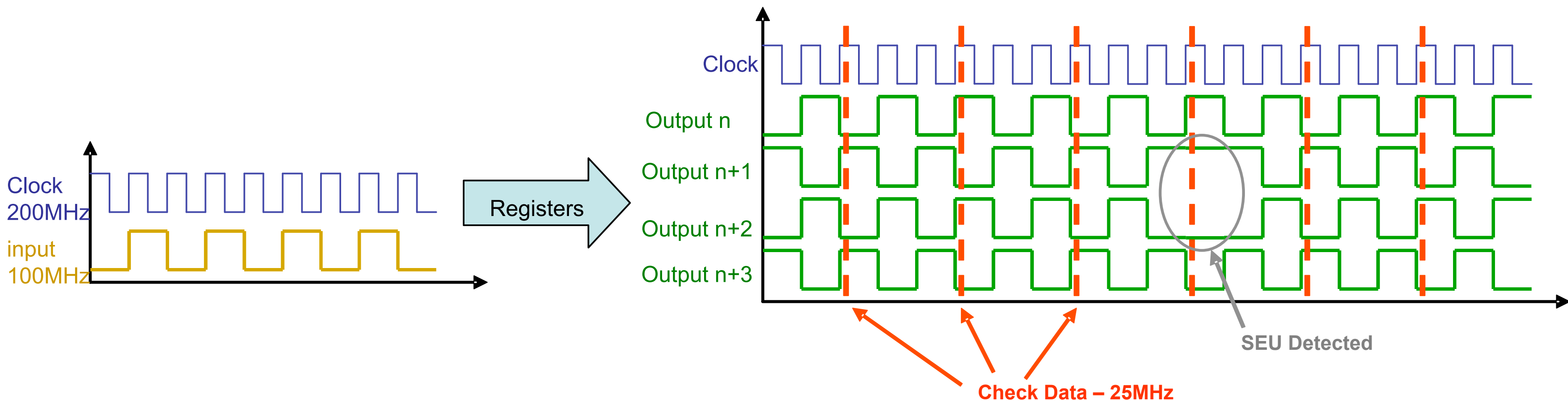
Shift Register chain

100MHz
20MHz
Internal PLL 200MHz
D CLK En CLR Q
LVCMOS 3.3V

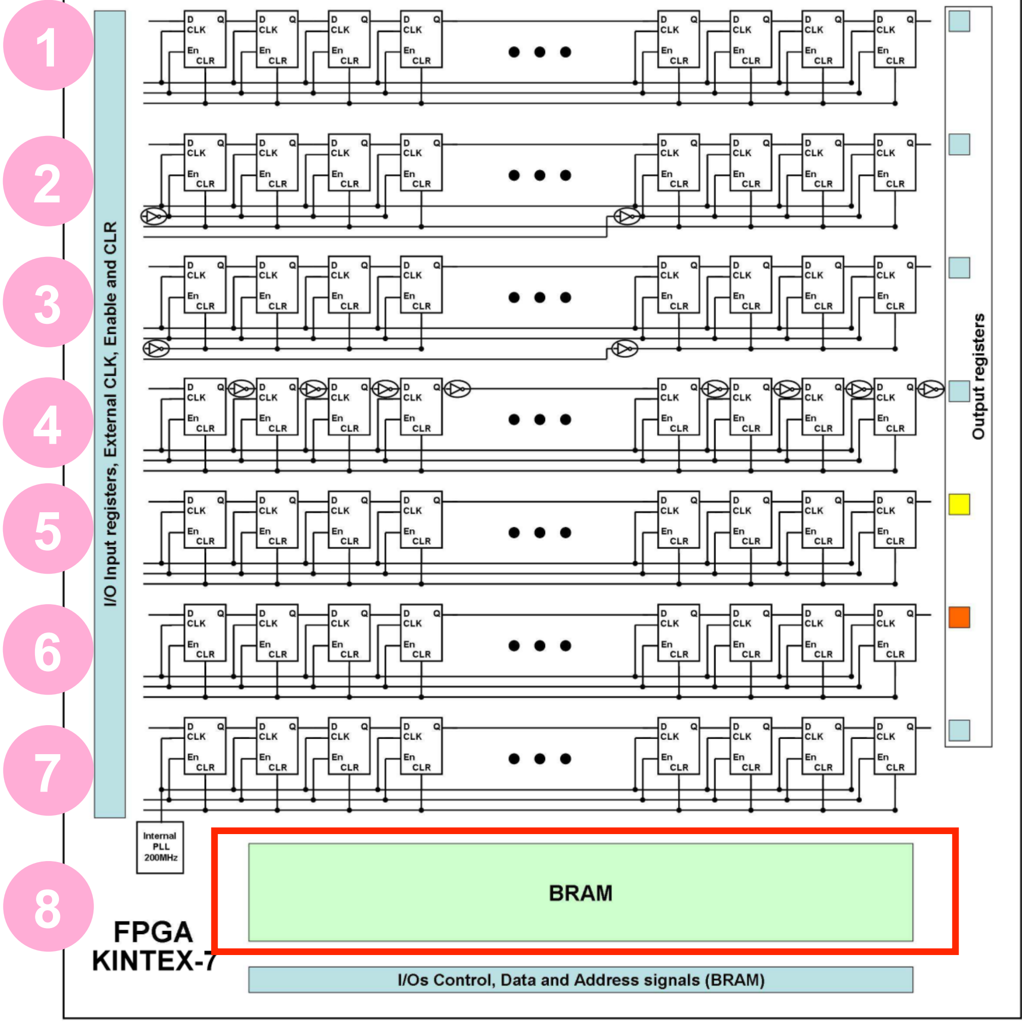
- **Input clock 20MHz on PLL x 10**
- **Input Data 100MHz**

SEU, MBU and SEFI analysis

- The virtex4 board will generate for each chain, a common external clock of 200 MHz + input square signal of 100MHz
- The output of each shift register chain is bufferized 4 bits by 4 in the Virtex4 board
- If 500 consecutives SEU are observed, an SEFI will be counted



Shift registers and BRAM



- ***Filling at least 50 - 90% of the reconfigurable blocks***

Chain	Clock	Logic Between registers	Logic to Enable pins registers	Logic to CLR pins registers	I/O type
1	200 Mhz	no	no	no	LVCMOS 3.3V
2	200 Mhz	no	yes	no	LVCMOS 3.3V
3	200 Mhz	no	no	yes	LVCMOS 3.3V
4	200 Mhz	yes	no	no	LVCMOS 3.3V
5	200 Mhz	no	no	no	LVDS 2.5V
6	200 Mhz	no	no	no	DDR 3.3V
7	20Mhz x PLLx10	no	no	no	LVCMOS 3.3V
8	BRAM of 36 Kbits				

BRAM: SEU, MBU and SEFI

- 36 Kbits Block RAM – 4096 address bits and 9 data bits
- All memory will be written with two patterns 0xAA for odd address and 0x55 for even address

	Step 1: Read	Step 2: Readback	Step 3: write	Step 4: Read
No error	Good data ✓	-	-	-
ERR. Type 1	Bad data ✗	Good data ✓	-	-
ERR. Type 2	Bad data ✗	Bad data ✗	Expected data	Good data ✓
ERR. Type 3	Bad data ✗	Bad data ✗	Expected data	Bad data ✗

- Event classification:
  - Transient (error type 1)
  - Upset (error type 2)
  - Stuck bit (error type 3)

Tests & radiations

Conclusion

- **The test is still on development**
- **The final space application is on discussion**
- **The final heavy ions test will be performed before the end of the year.**

- Thank you for your attention

- Any question ?