ESA - SpacE FPGA Users Workshop, 3rd Edition

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WE LOOK AFTER THE EARTH BEAT

Feedback on Xilinx Virtex-5QV

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Agenda

- Features of the FPGA
- Design flow
- Performances
- Power consumption
- Recommendations

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XILINX VIRTEX XQR5VFX130

Also known as ... SIRF (**S**ingle event **I**mmune **R**econfigurable **F**PGA)

- CMOS Technology / 65 nm process
- Guaranteed operation over full military temperature range (-55°C to +125°C)
- Radiation Hardened By Design (RHBD) Technology
- SEU Hardened Configuration Memory Cells
- Embedded Error Detection And Correction (EDAC) and autonomous writeback for high-performance Block Memory SEU Mitigation

Reference : *DS192 (v1.4) Radiation-Hardened, Space-Grade Virtex-5QV Family Overview*

Xilinx Space-Grade FPGA Features – Radiations (2/5)

Fully characterized for space radiation effects (by the XRTC*)

- Total Dose
  - 1 Mrad(Si) total ionizing dose per method 1019
- **S**ingle **E**vent **L**atch Up (SEL)
  - Latch Up immunity to LET >100 MeV per mg-cm²
- **S**ingle **E**vent **F**unctional **I**nterrupt (SEFI)
  - Extremely low rates (e.g. less than once every 10,000 years for GEO orbit)
- **S**ingle **E**vent **U**pset (SEU)
  - Different resources have been tested (DSP, BRAM, Flip Flops, CFG memories)

*XRTC = Xilinx Radiation Test Consortium

Reference : *DS192 (v1.4) Radiation-Hardened, Space-Grade Virtex-5QV Family Overview*

Xilinx Space-Grade FPGA Features – Radiations (3/5)

- Example of radiation sensitivity for an altimeter orbit (873km, 78°)
  - No SEL
  - No SEFI (much less than one event per mission)
  - SEU rate

Type of resources	Event rate	Impacts
CFG memories	Around 2 events per mission	Bitstream re-load
DSP blocks	Less than 8 events per day	No impact
BRAM memories		
Without EDAC	Less than 10 events per day	No impact
With EDAC	Much less than 1 event per mission	No impact
Flip-Flop	Much less than 1 event per mission	No impact

Xilinx Space-Grade FPGA Features (4/5)

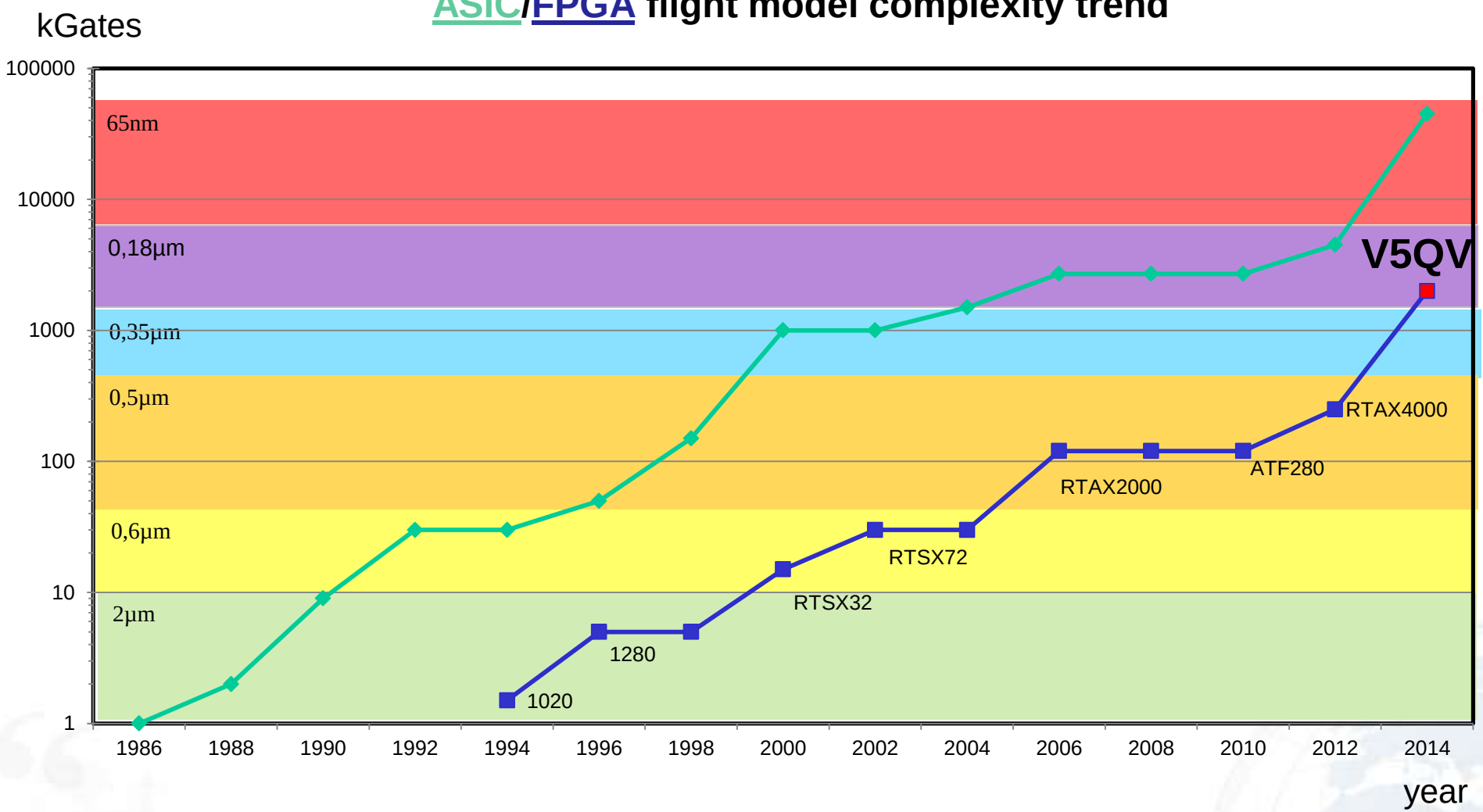
- FPGA resources
  - 81920 SEU Hardened Flip-Flops
  - 81920 x 6-inputs LUTs (Look-up Table)
  - 320 DSP slices
  - 298 x 36 Kb Block RAM
  - 836 User I/Os
  - 6 PLL / 12 DCM
  - …

About **2 Millions** of equivalent ASIC Gates (for logic only)
+
Up to **10.5 Mb** of embedded memory

Reference : *DS192 (v1.4) Radiation-Hardened, Space-Grade Virtex-5QV Family Overview*

Xilinx Space-Grade FPGA Features (5/5)

ASIC/FPGA flight model complexity trend



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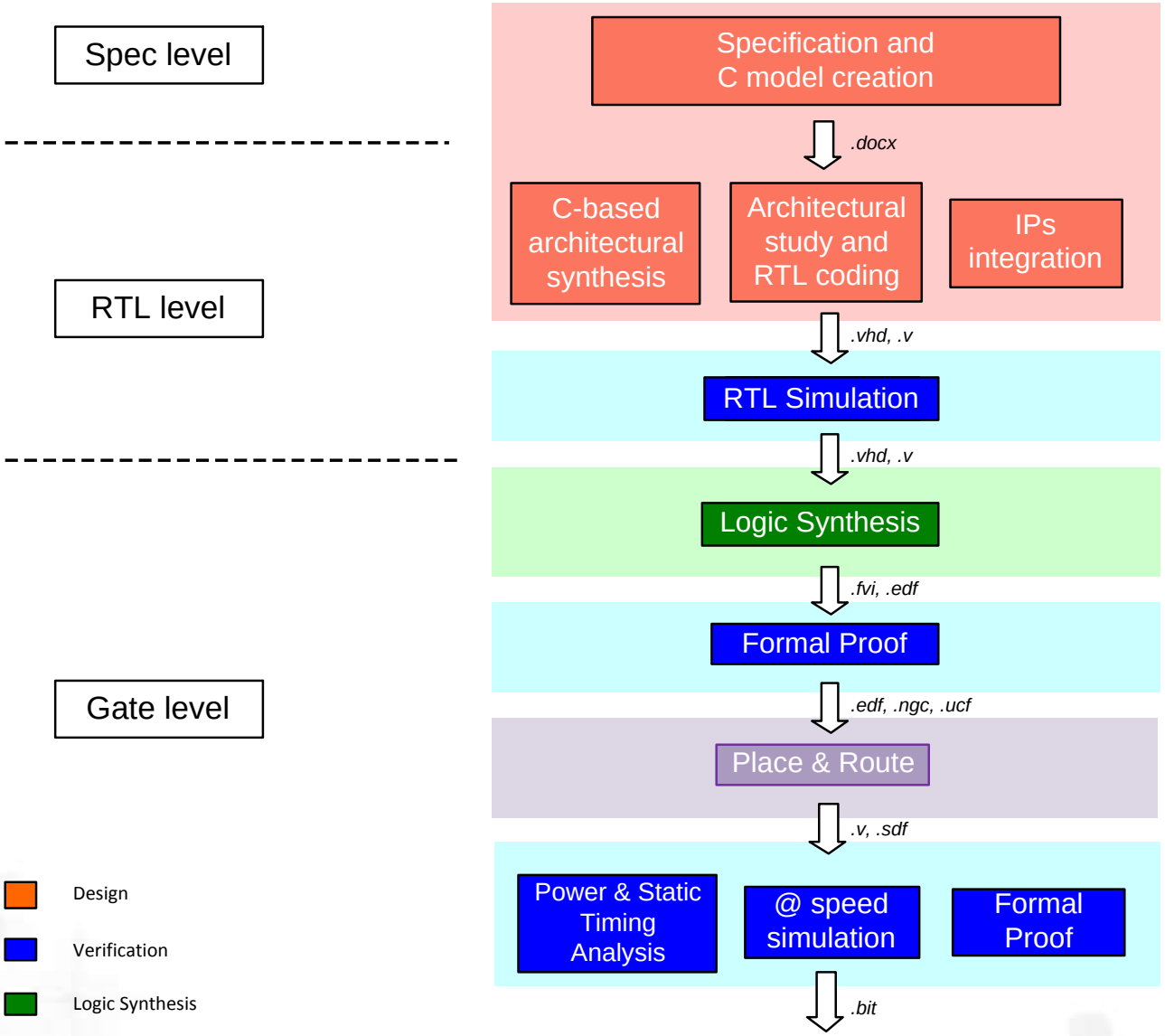
Design flow used for Xilinx Space-Grade FPGA (1/2)



PlanAhead

XPA, Timing Analyzer

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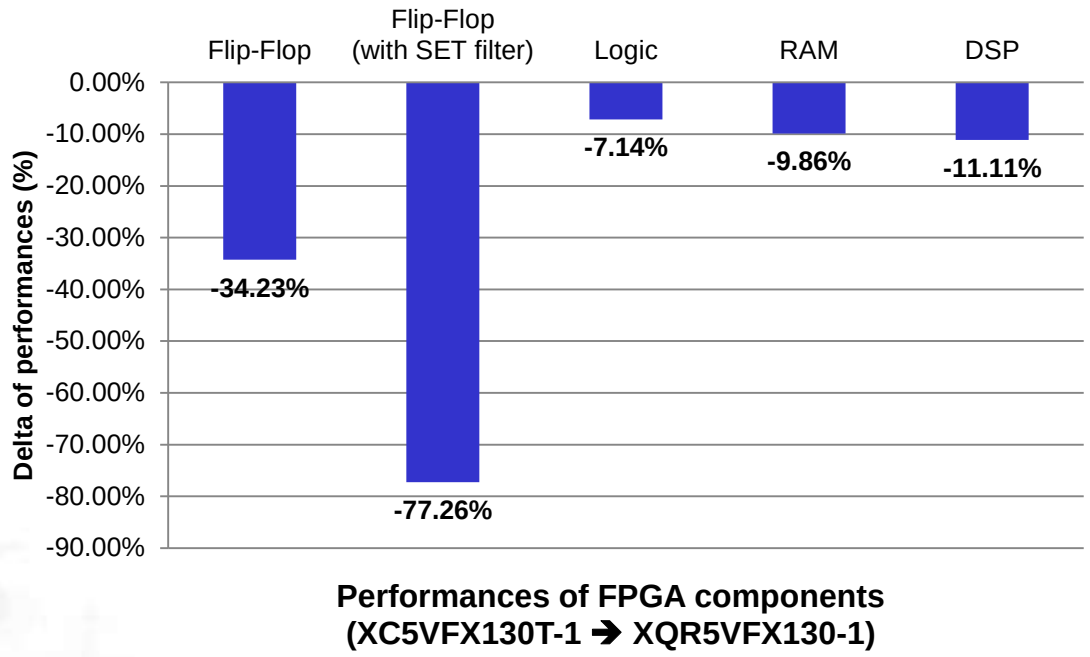
Design flow – Formal proof (2/2)

- Formal proof verifies RTL versus layout tool output netlist
- Why ?
  - RTL and gate simulations cannot be fully exhaustive
- How ?
  - Flow built with the help of tool suppliers
  - Declare DSP, memory blocks and specific macros as black boxes
- Results
  - 100% of the designs are equivalent (with exclusion constraints)

Performances of Xilinx Space-Grade FPGA (1/2)

- Delta of performances between:
  - Space-grade FPGA XQR5VFX130-1 (SIRF)
  - Commercial FPGA XC5VFX130T-1
- Comparison between datasheets:



Performances of FPGA components (XC5VFX130T-1 ➔ XQR5VFX130-1)

Concerns only basic elements and **not routing nets !**

Reference : *DS692 (v1.3.1) Radiation-Hardened, Space-Grade Virtex-5QV Data Sheet*

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Performances of Xilinx Space-Grade FPGA (2/2)

- Performances on a data processing design
  - Complexity

	Used	Available	% used on SIRF target
Flip-Flop	30506	81920	**37.2%**
Logic	22355	81920	**27.3%**
DSP	172	320	**53.8%**
RAM	181	298	**60.7%**
IO	432	836	**51.4%**

  - The best internal core frequency
    - $f_{CORE(XC5)}$ = **173** MHz
    - $f_{CORE(XQR5)}$ = **125** MHz

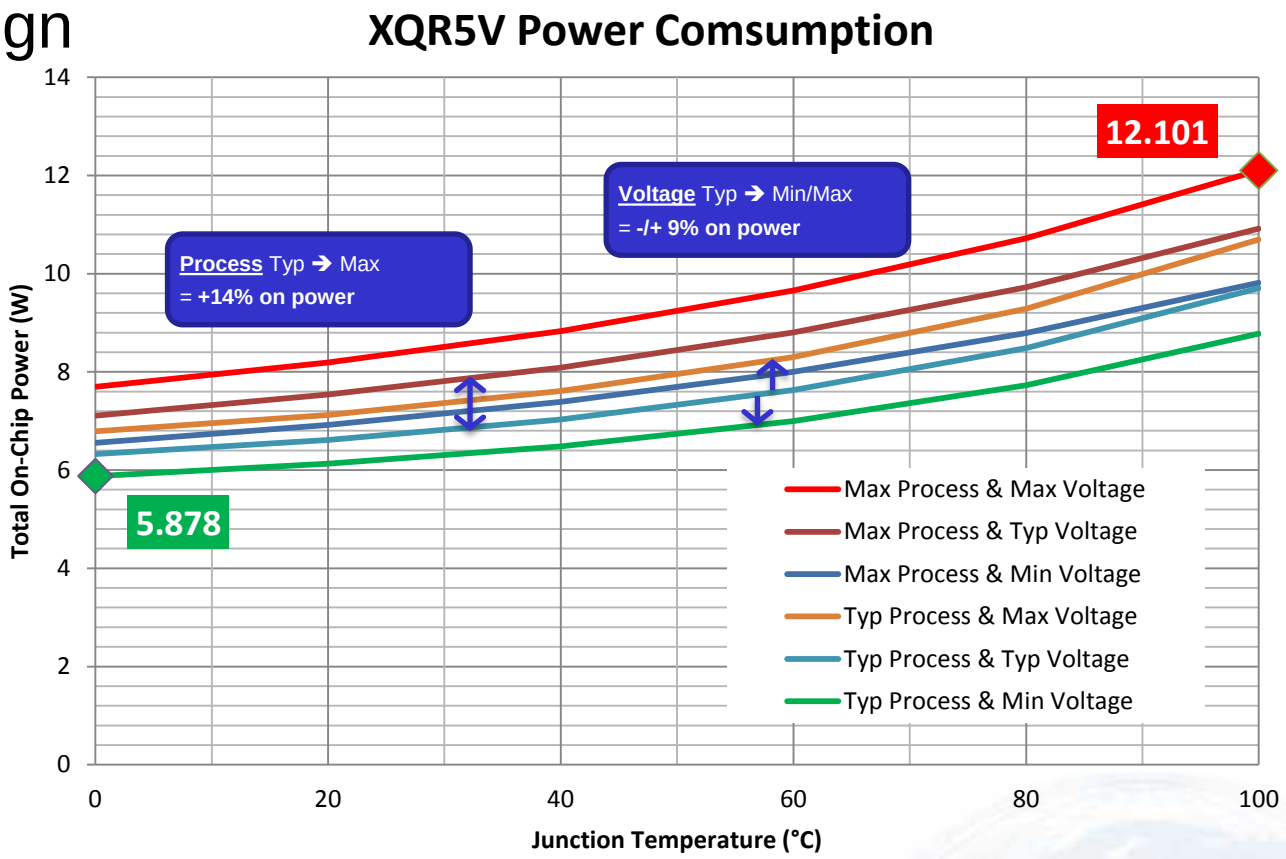
On this design, performances of the Xilinx Space-Grade FPGA is **about 28%** lower than those of the commercial target.

Power consumption of Xilinx Space-Grade FPGA (1/2)

- On the previous design
  - Data from XPE*
- Main issue
  - If the junction t° ↑ then the power ↑
  - And if the power ↑ then the junction t° ↑

➔ **closed-loop system**

*Reference : *Xilinx Power Estimator 14.3*



The **power** and the **junction temperature** must be carrefully monitored.

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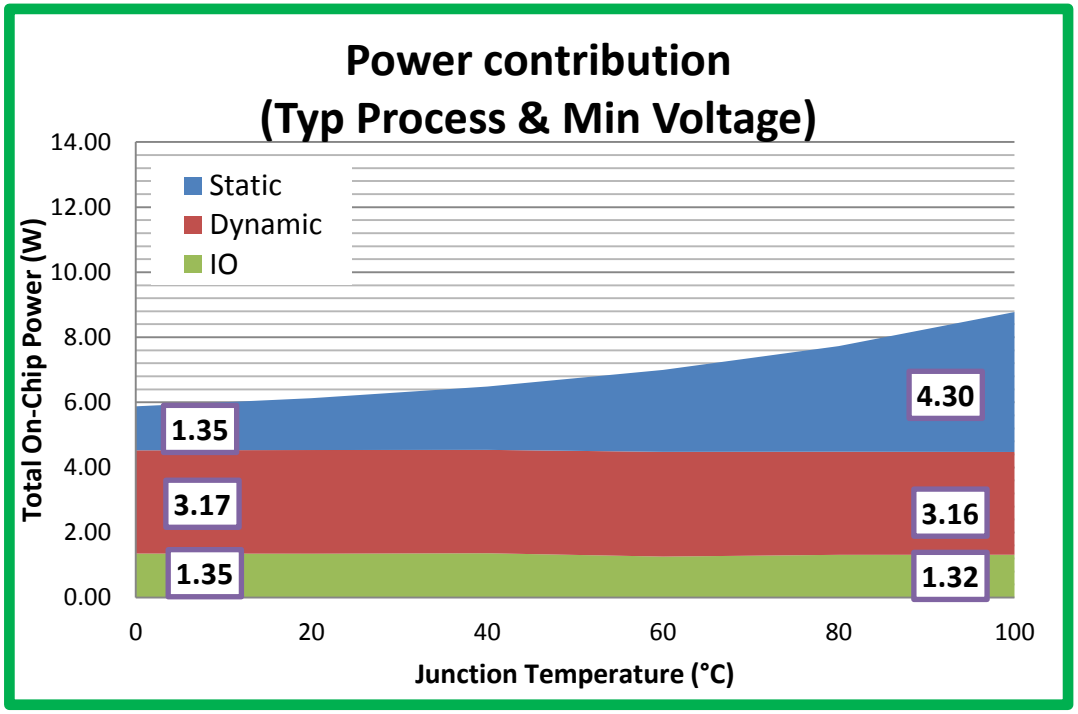
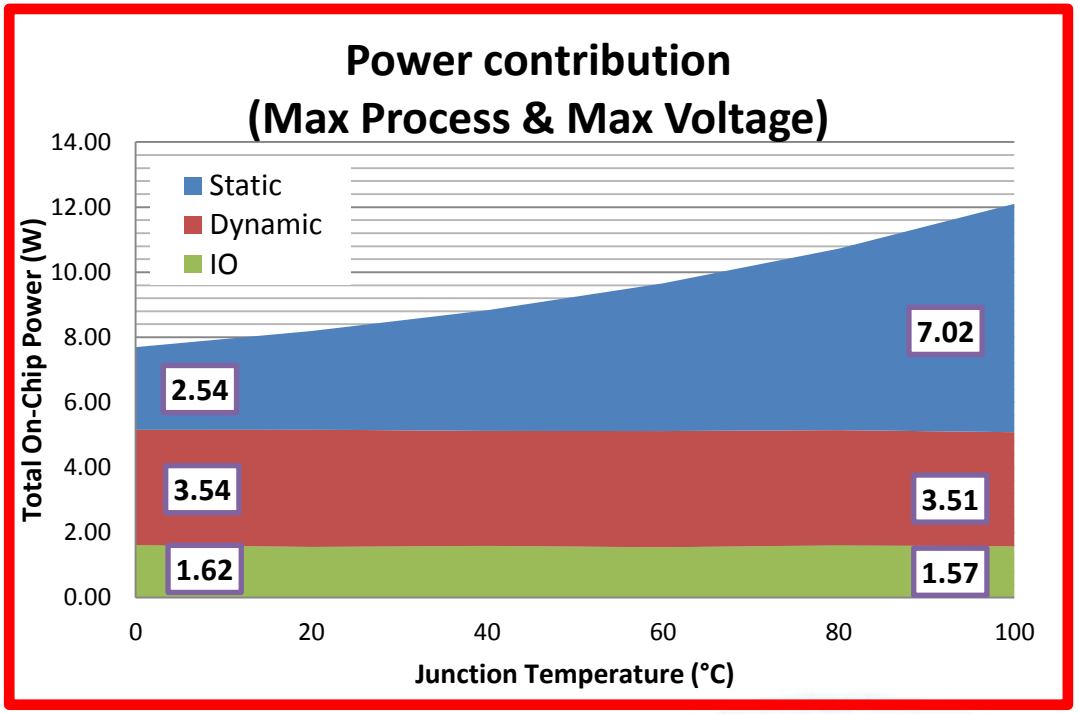
Power consumption of Xilinx Space-Grade FPGA (2/2)

- Power can be splitted into multiple components:

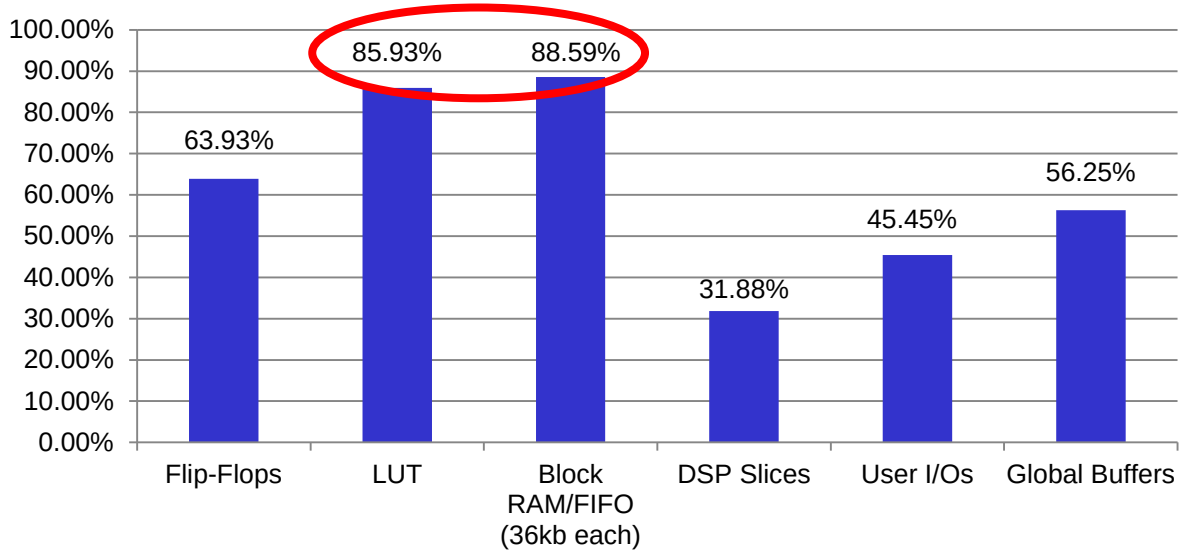


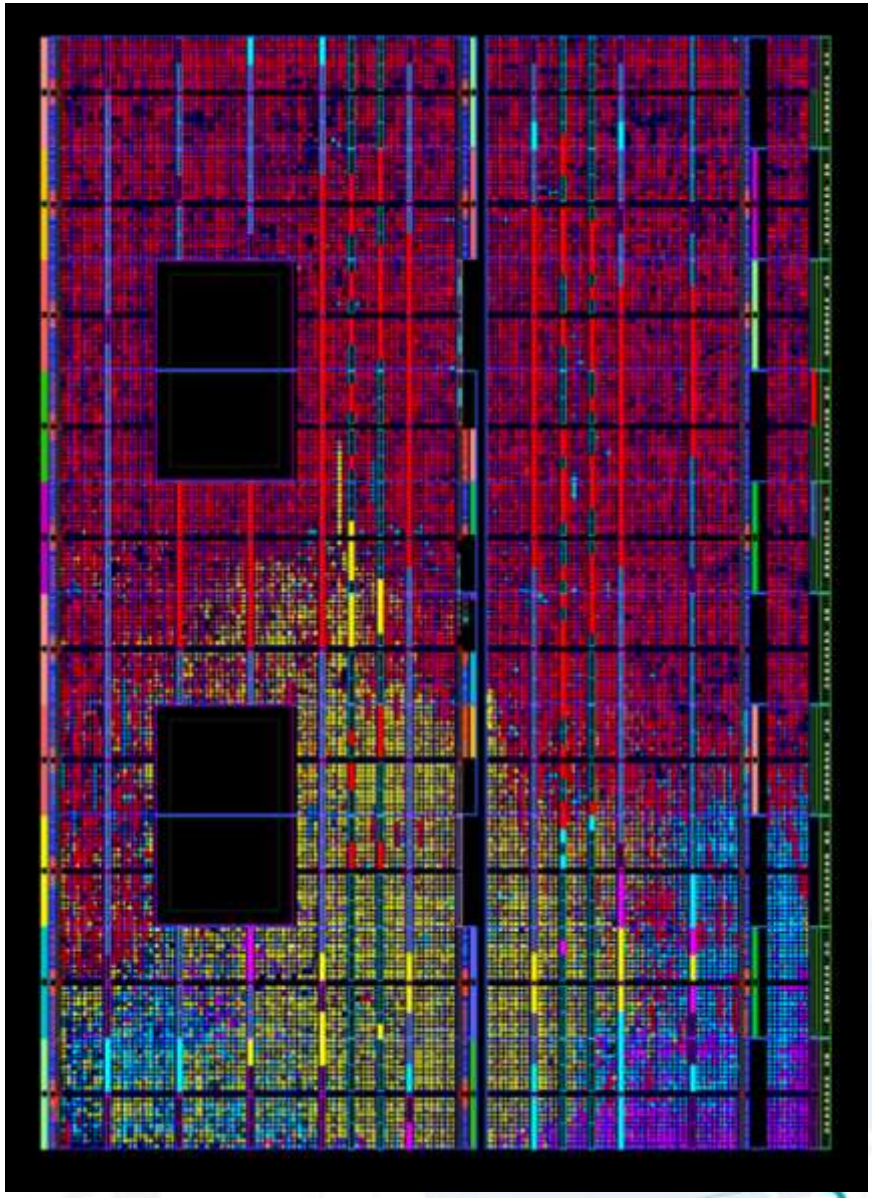


The main contributor of power consumption is the **static power** (~leakage current).

Critical design on V5-QV FPGA

FPGA resources utilization





Congestion can appear and performances can be deteriorated if no precautions are taken.

Recommendations (1/2)

- In order to design with SIRF, you must:
  - Use ISE Design Suite 13.2 (released in 2011)
  - Use the Virtex-5QV FPGA Overlay
  - Use a special XPE for power consumption (including SET filter FF)
  - Potentially, target the commercial FPGA (i.e. *XC5VFX130T-1*) if you don’t use Xilinx flow

Recommendations (2/2)

- And more generally:
  - Properly constrain your design for the P&R tool :
    - Timing exceptions, clocks, etc…
    - Floorplanning / Physical constraints
  - Respect Xilinx coding style
  - Optimize architecture (pipeline, parallelization…)
  - When a stable fully-routed solution was found, you can launch SmartXplorer in order to check if there is a better strategy for your design.

Thank you for your attention.