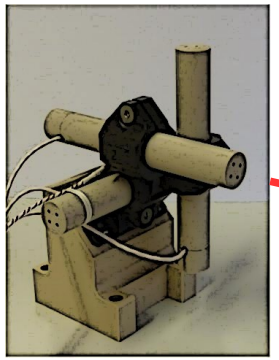
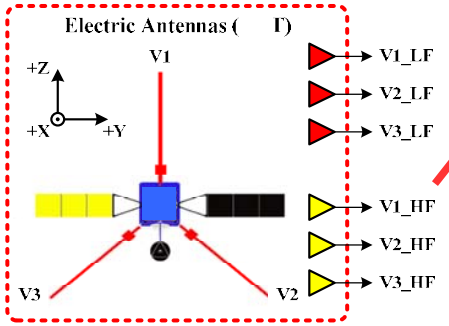
Prototyping a SOC on RTAX4000D for Solar Orbiter's Low Frequency Receiver

SEFUW : SpacE FPGA Users Workshop

Alexis Jeandet
Jean-Christophe Pellion
Paul Leroy
Thomas Chust
Vincent Leray

LFR Instrument





Analog Input buffers

ADC1

ADC8

RTAX4000D

SPW1

SPW2

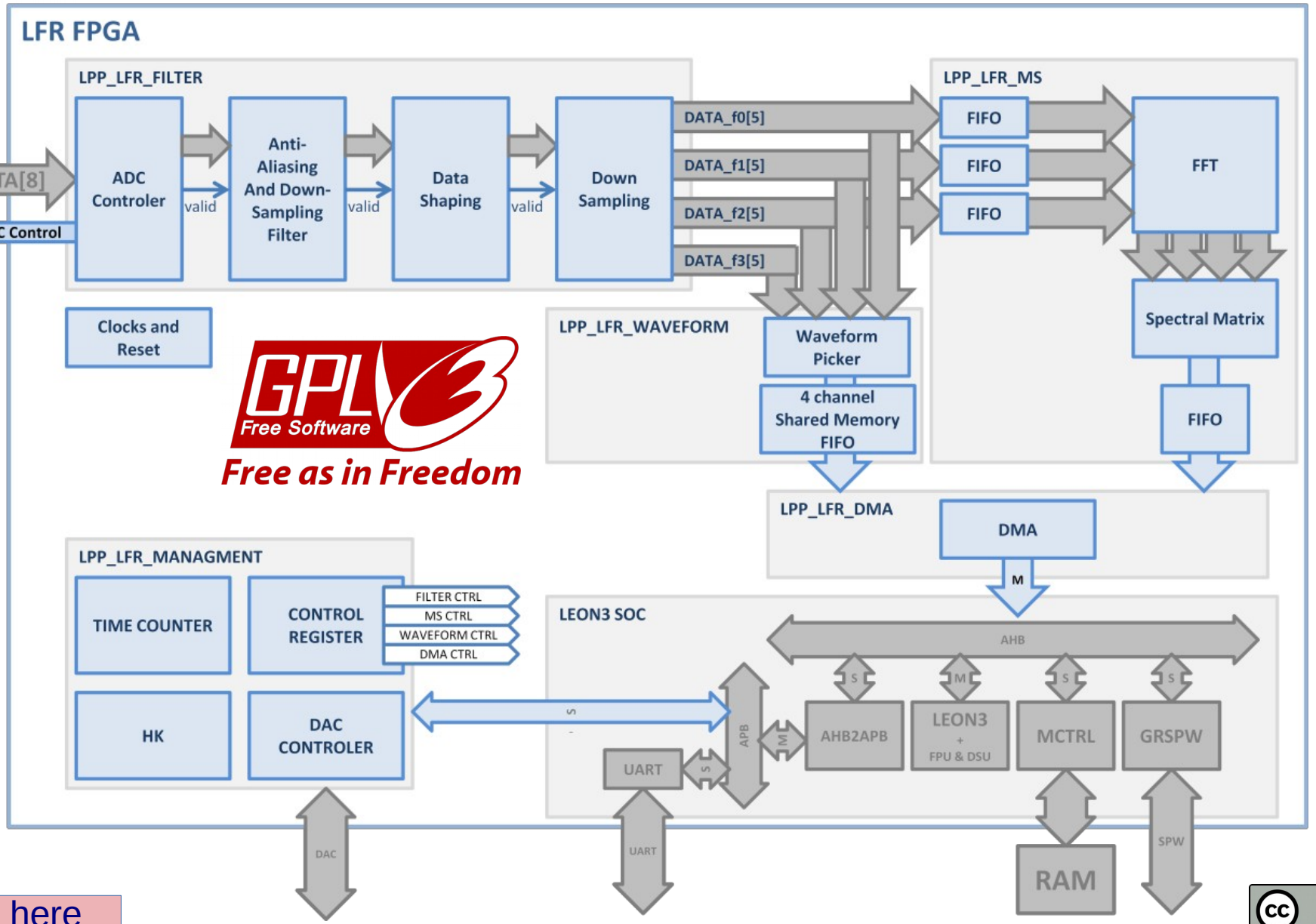
32Mb RAM

Temperatures

Power Supply 1.5V,3.3V,2.5V

LFR Instrument

LFR System On Chip



Get code here

Why RTAX4000D?

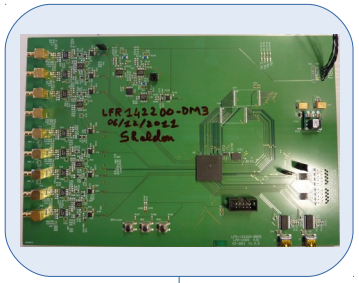
Vs RTAX2000D

- Mostly memory blocks
- Then logical resources
- Timings

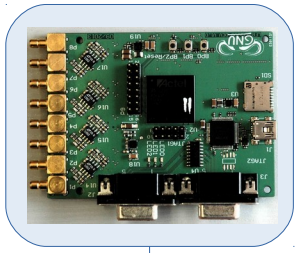
Vs Virtex-5QV

- Static power consumption
- Really big
- Package soldering difficult to qualify

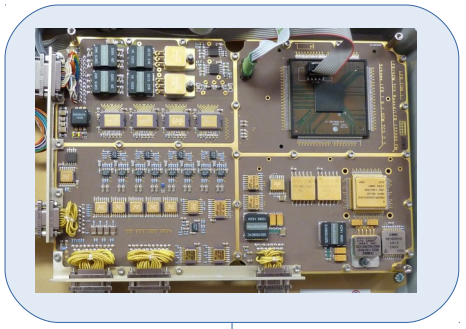
Prototyping philosophy



DM
May 2010



Mini-LFR
Nov 2013

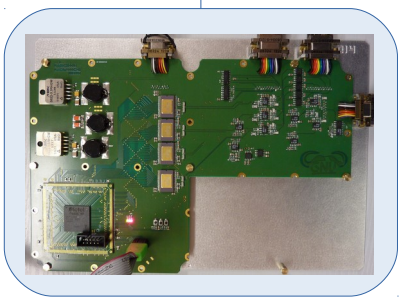


EQM
Feb 2015

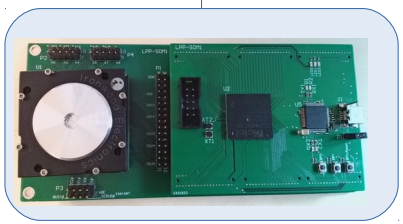
PFM
March 2016

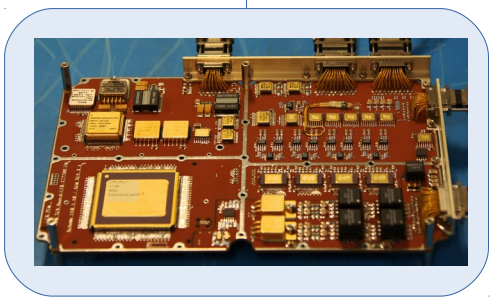
SPARE
Q2 2016

EM
March 2011



RAM-Test
Aug 2014

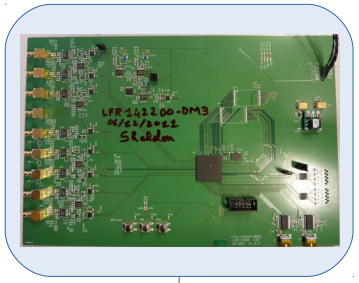




A3PE for prototyping ?

- **Enough RAM blocks for our needs**
- **Less cells but enough for incremental dev**
- **Performances are close to RTAX**
- **Same tools**
- **Power consumption is the same order**
- **Package smaller**

Prototyping EM



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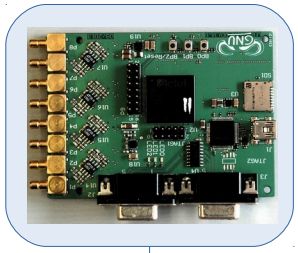

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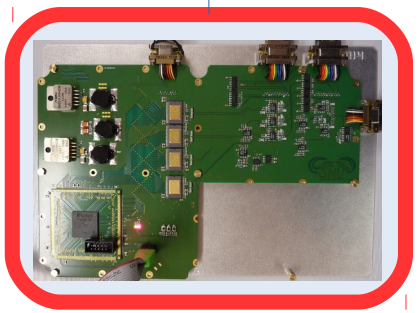

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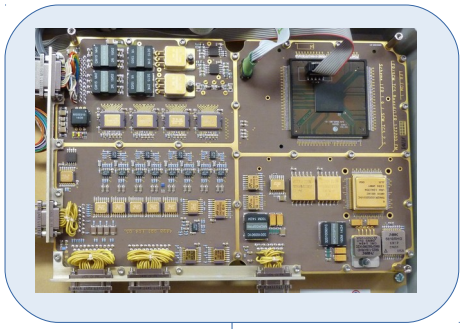

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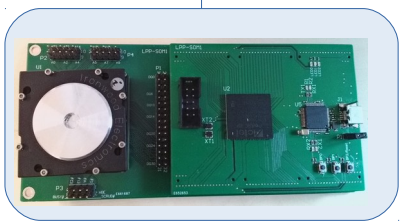

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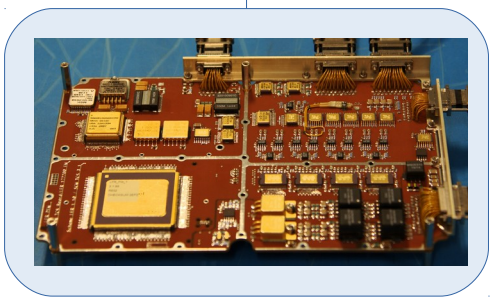
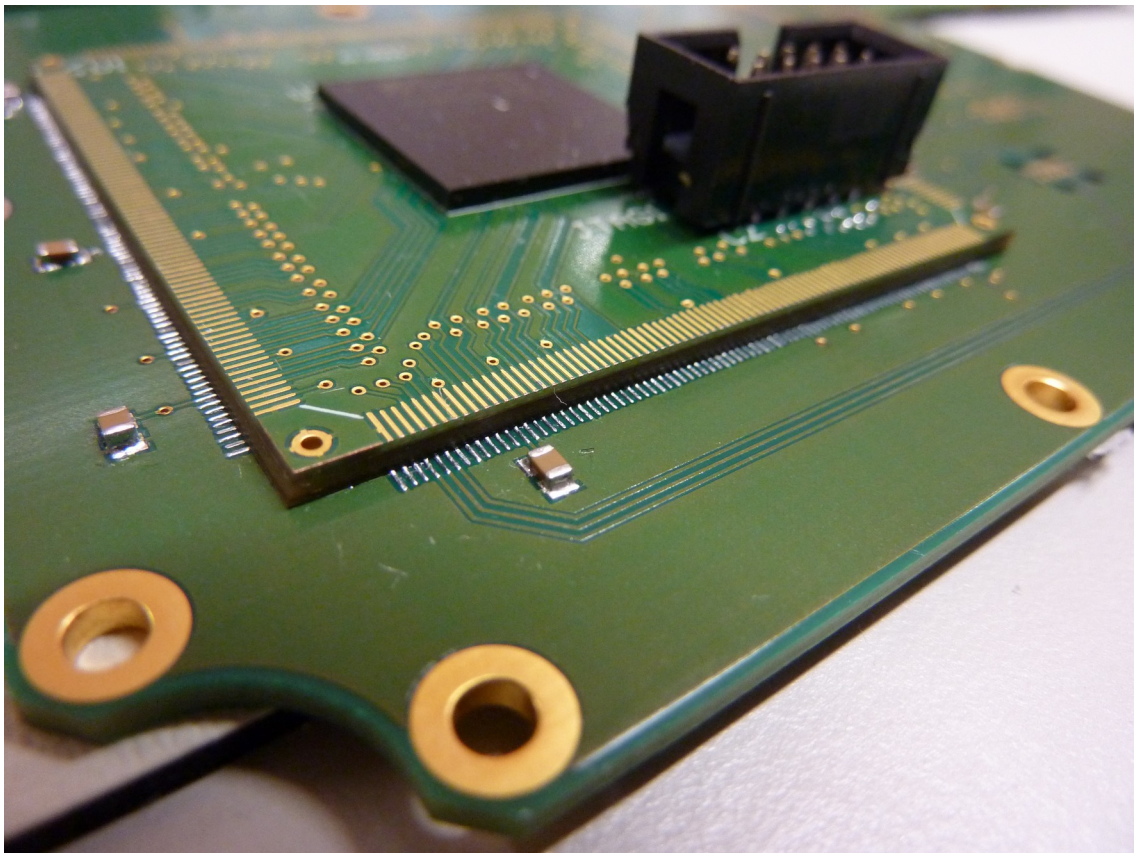


PFM
March 2016

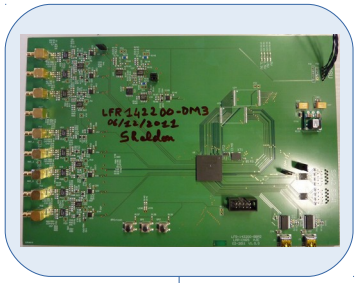
SPARE
Q2 2016

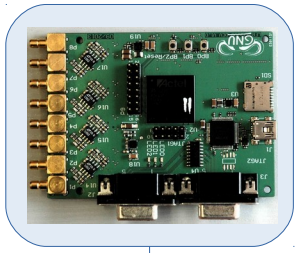
A3PE adapter #1(EM)

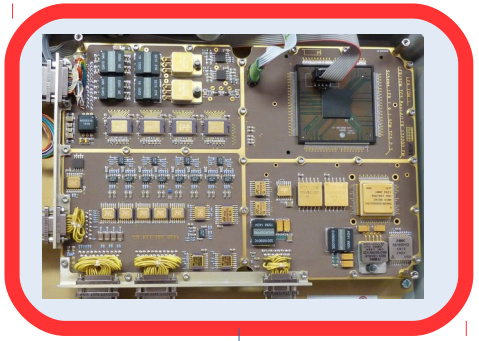


- Low cost (~35€+FPGA)
- Custom
- Hard to solder
- Weak (not tested)

Prototyping EQM







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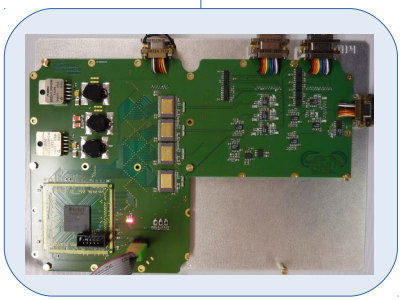
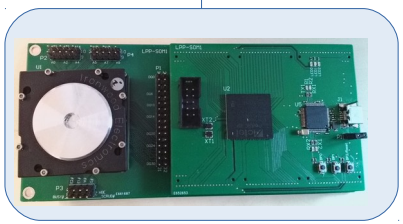
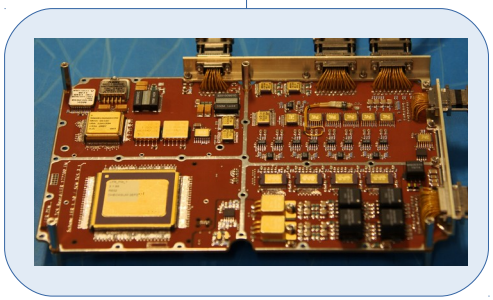
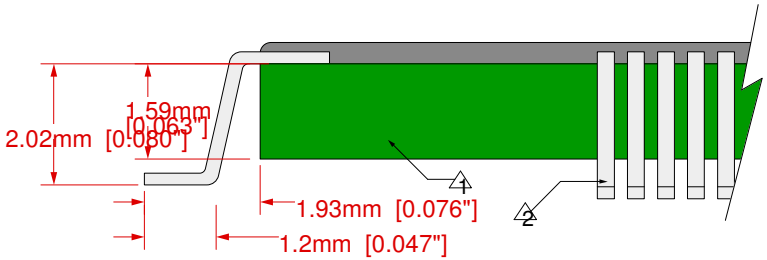
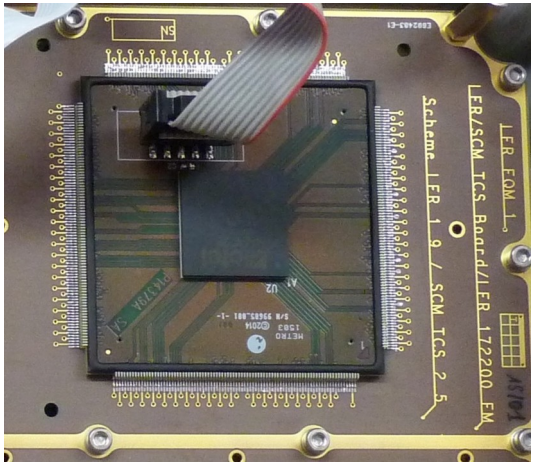


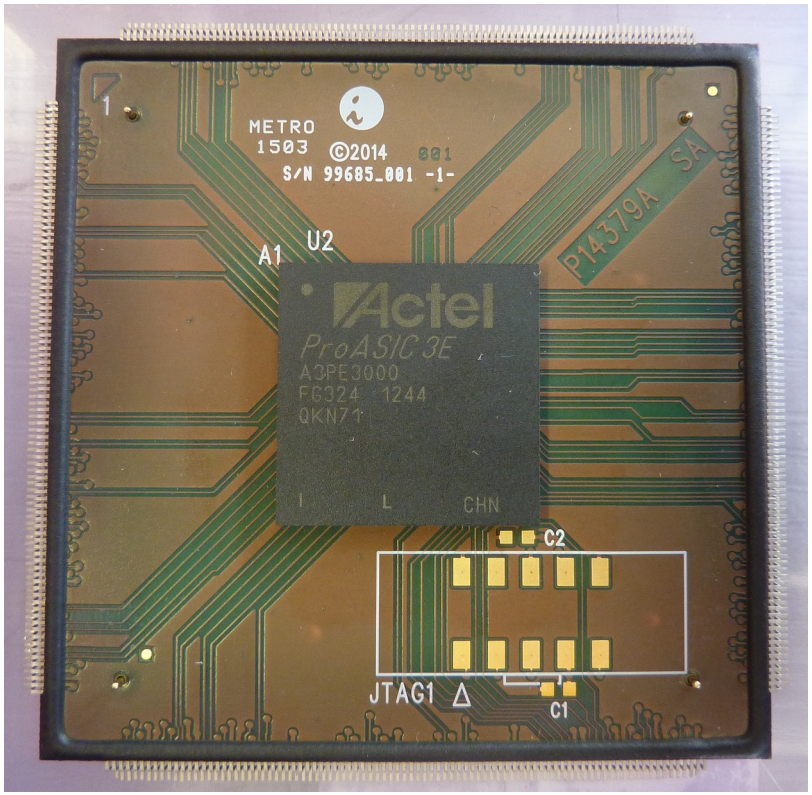




A3PE adapter #2(EQM)

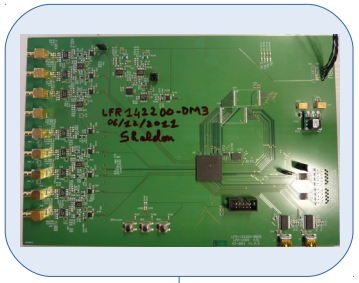


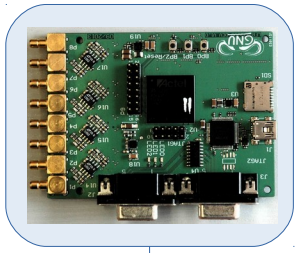


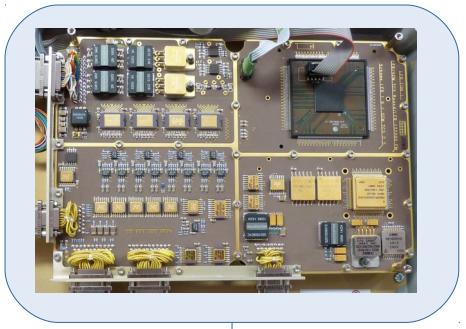


- Custom design
- More robust
- Easy to solder
- Expensive

Tests on PFM







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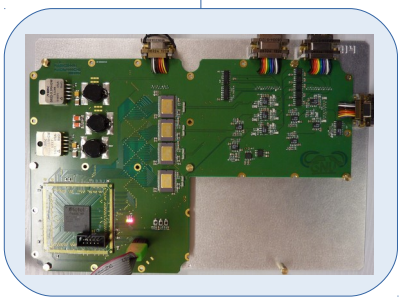
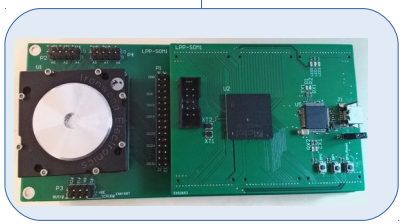
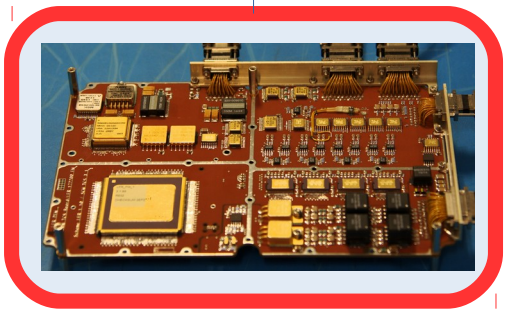


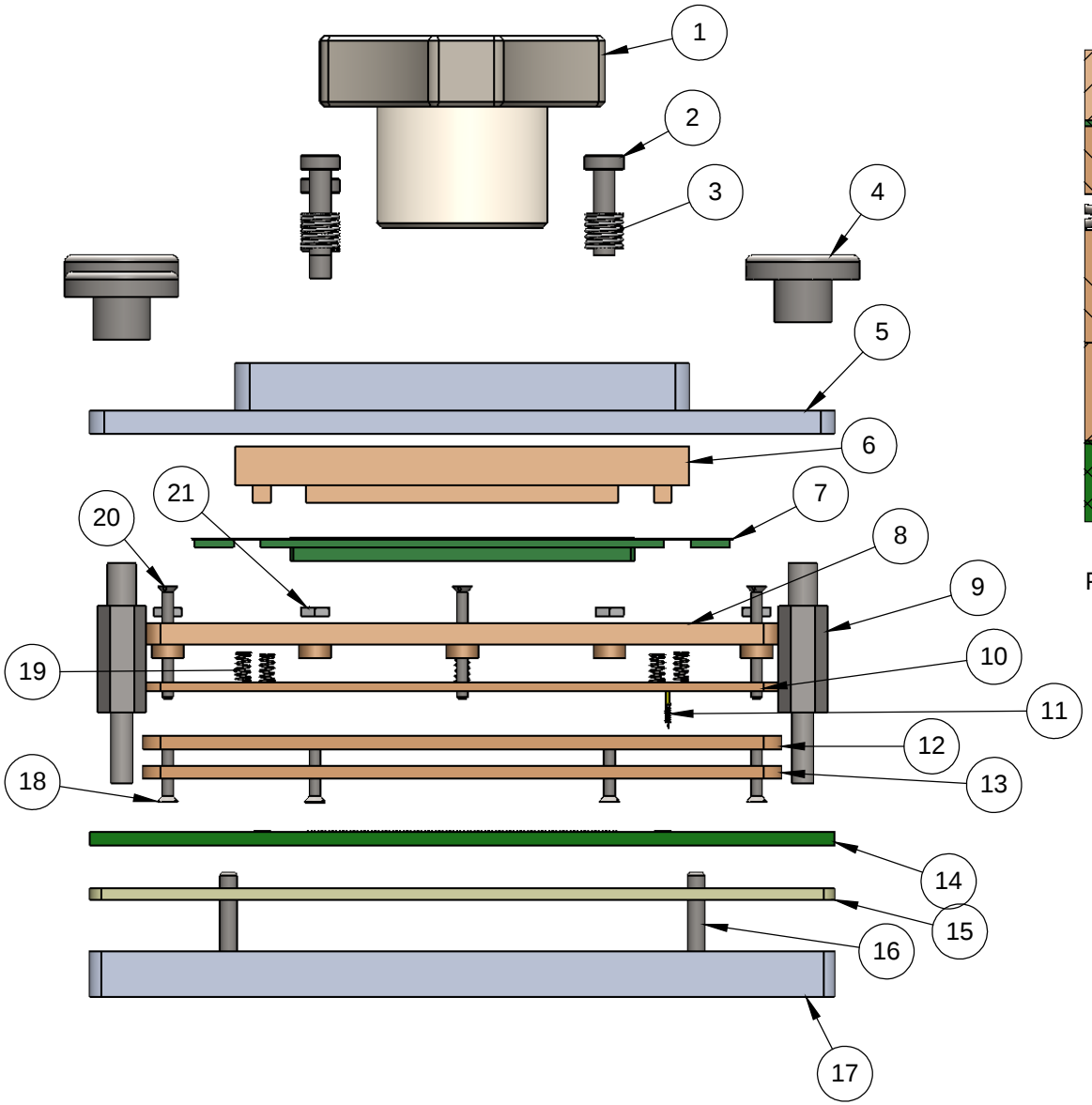




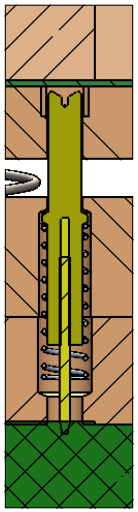
Constraints

- No soldering
- Support from -30°C to +70°C
- No stress for the board and parts
- Reusable

Solderless socket(1)



Compression plate



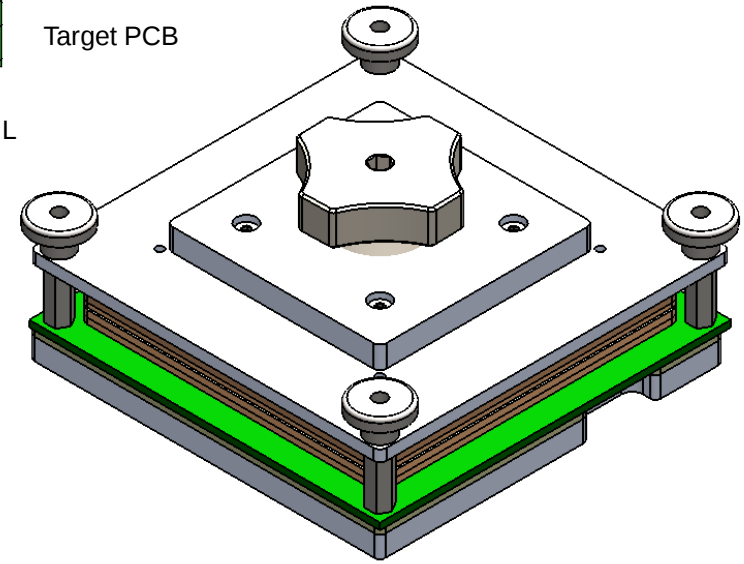
Floating guide

Middle guide

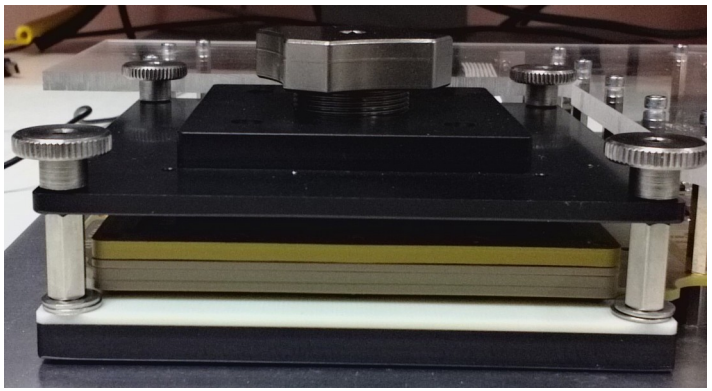
Bottom guide

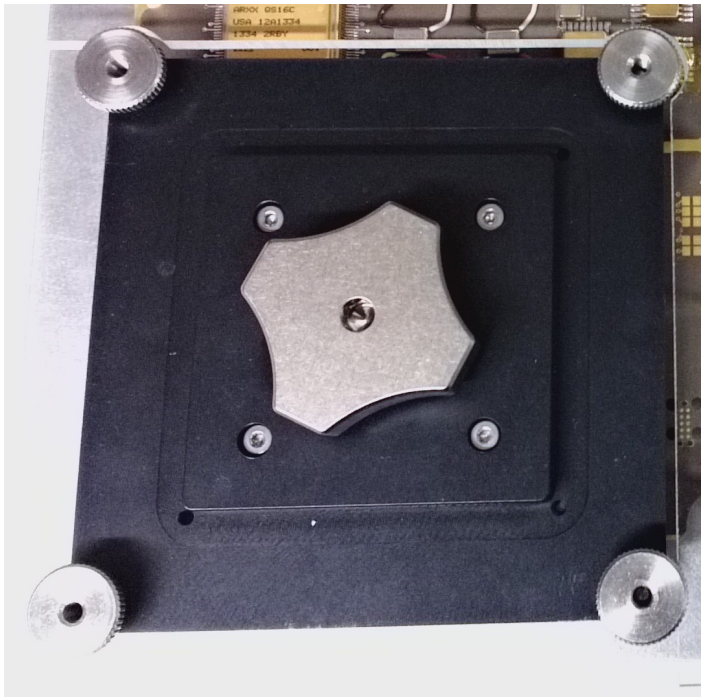
Target PCB

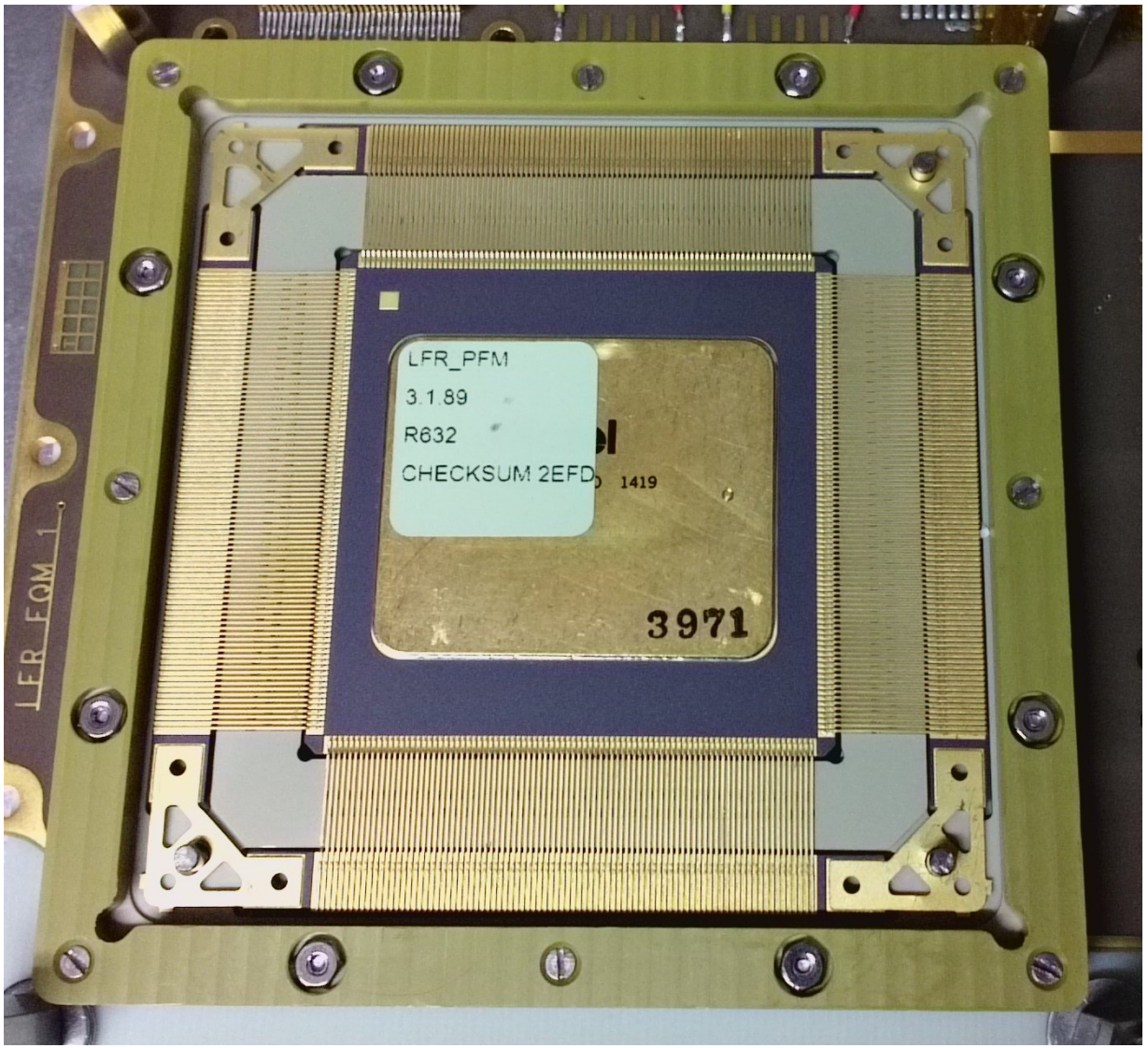
PIN DETAIL



Solderless socket(2)







Solderless socket(3)

- Use RTAX with tie bar
- No solder
- High temperature range(-55 to +180)
- Up to 4A per pin(16mOhms)
- Excellent signal integrity at high frequencies(>14GHz)
- No more NRE (QFE352SC)(~2k€)
- Quite big
- Not so expensive(900€ wo NRE) and reusable(125K cycles)

Well suited for Burn-in and others tests

IRONWOOD PACKAGE CODE: QFE352SC

Design tools

- Libero 9.1.5.1 with default Synplify gives 85 % cell usage + 85 % delay as cell→ total **170 %** cell usage and **12MHz**.
- Libero Version 9.1.5.1 with **Synplify E-2012-03A-SP1-2** gives correct results :

R-CELL=90,99 %

C-CELL=84,05 %

DSP=4,16 %

~26MHz

RTAX4000D

- Compared to A3PE IO delays are different
- As usual add timing constraints to each IO.
- Only 8 global networks with 4 breakable.

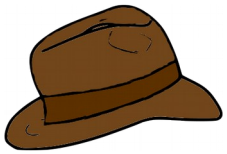
  → Ones should promote most loaded signals to those networks (in VHDL with actel macro).
- Use of multi-pass layout.(50 passes~22 to 26MHz)
- With GRSPW, follow the doc, add constraints and for the best layout pass move and fix the clock recovery gates. (Xor close to input and Flop with long data path to delay data from strobe).
- Poor usage of DSP blocks by GRLIB's IPs...

Conclusions

- Close to RTAX2000 flow
- No AX4000 for prototyping
- Design running at 25MHz, tested between -30°C and +70°C
- Whole board power consumption between 1.7W and 1.9W (Primary)

Caveats:

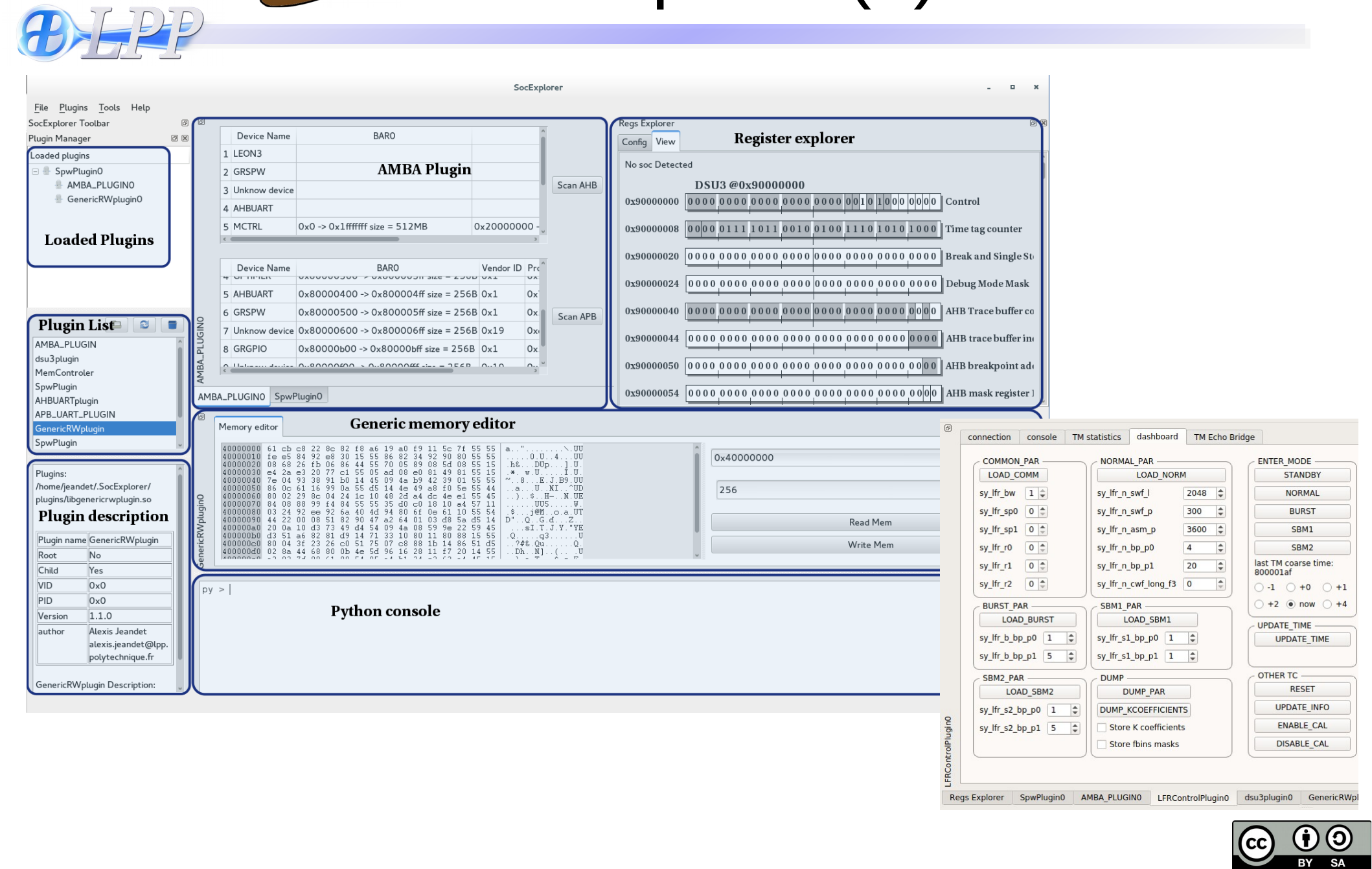
- Don't wait to compile for RTAX
- CQ352 thickness
- Libero version matters
- RTAX4000D pinout != RTAX2000 !
- High programming failure rate (~30%)



SocExplorer

- Ergonomic tool for SOC debug and tests
- Free (GPLv2)
- Written in C++
- Portable thanks to Qt api
- Scriptable with Python
- Extensible with plugins
- Scalable to user needs
- Used for the whole LFR validation from VHDL test and debug to calibration.

SocExplorer(2)



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- Thanks for your attention
- Questions ?