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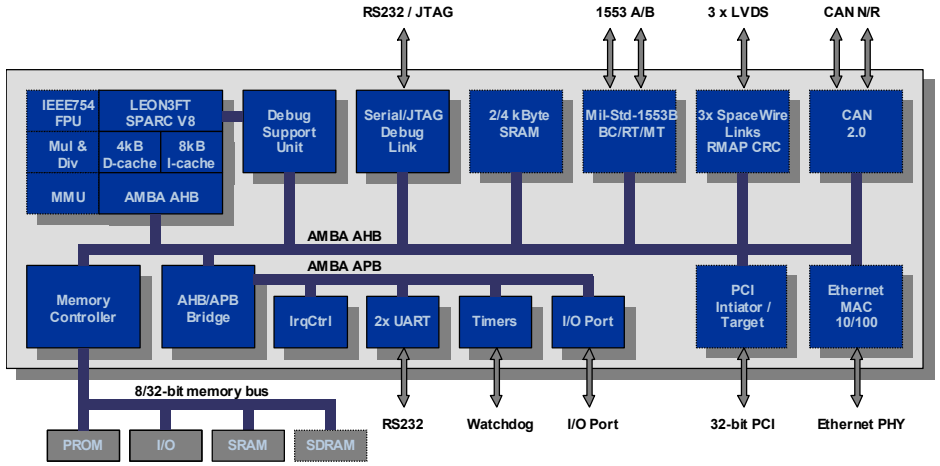
LEON3FT/GRLIB for Space-Grade Programmable Devices Update and Roadmap

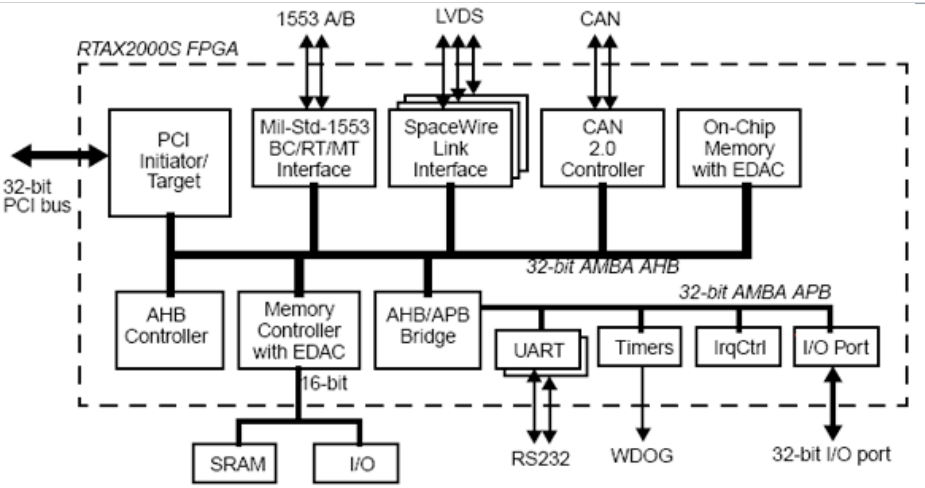
Cobham Gaisler AB

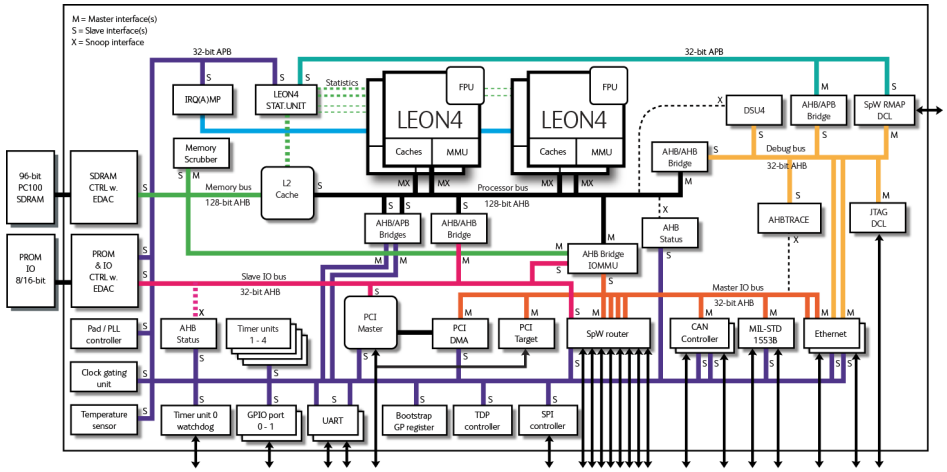
For Public View

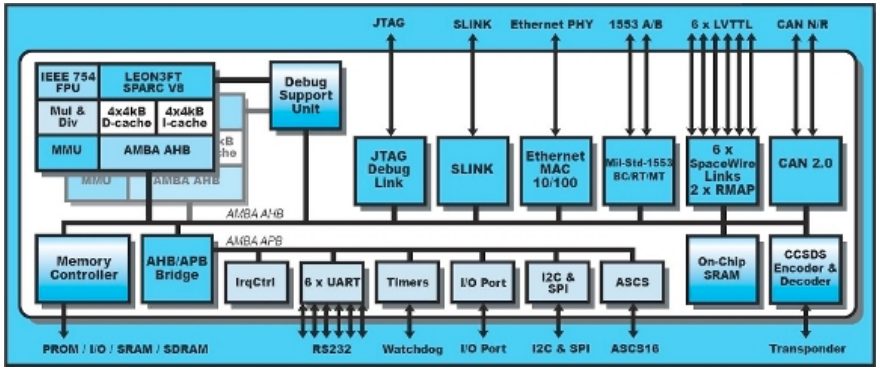
GRLIB

What to do with it?

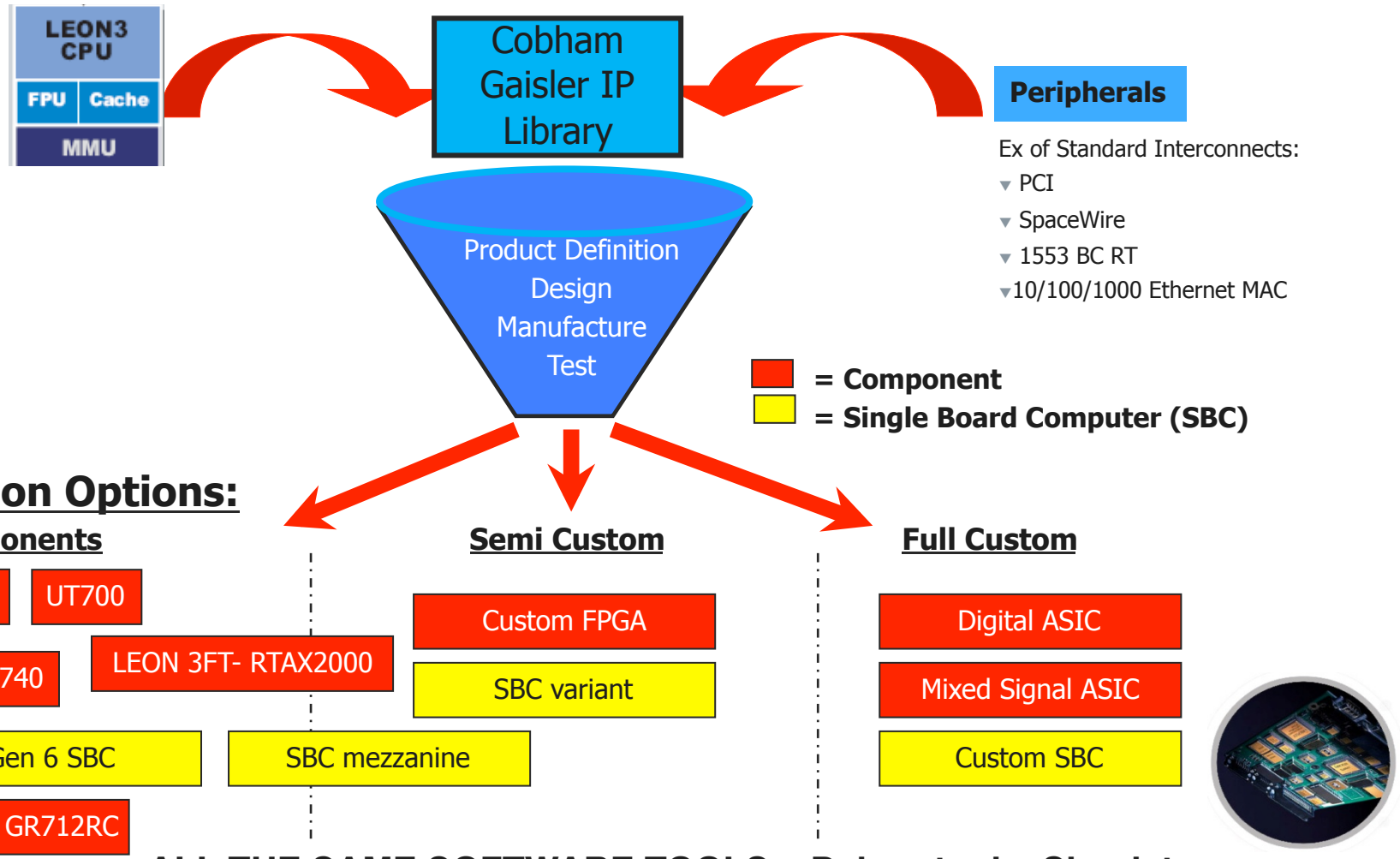








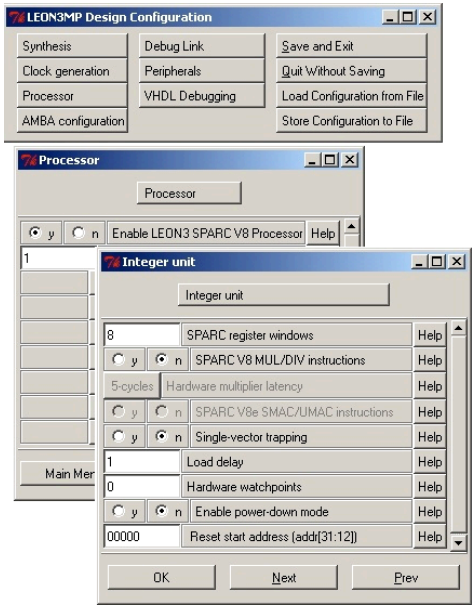
LEON3FT Deployment Options

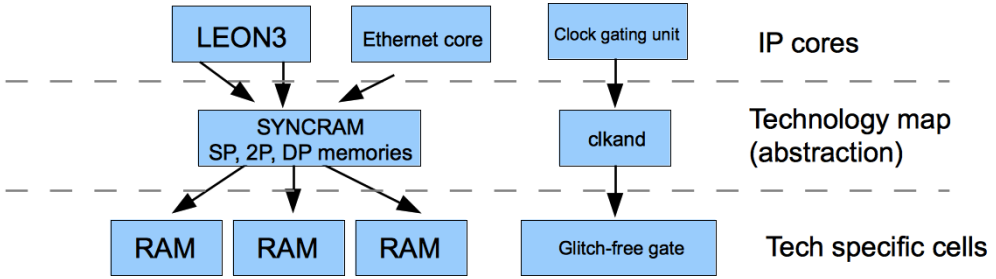


GRLIB

Overview of IP library used in comparisons

- GRLIB is a complete design environment
  - Processors, Peripherals, Memory controllers
- AMBA on-chip bus with plug&play
- Fault-tolerant and standard versions
- Support for tools and prototyping boards
- Portability between technologies
  - IP cores instantiate abstractions, which then map to an element in the target technology
  - Aeroflex, Altera, Atmel, DARE, Microsemi, Ramon C, ST, TSMC, UMC, Xilinx, etc
- Template designs
  - Cobham XC6S – 7-series, Xilinx and Microsemi boards
- Tailored version for hi-rel PLD: GRLIB FT-FPGA

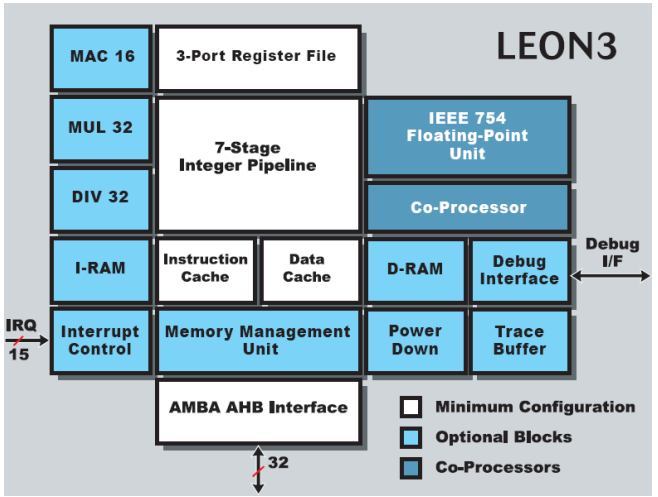




LEON3FT SPARC V8 32-bit Processor

Overview

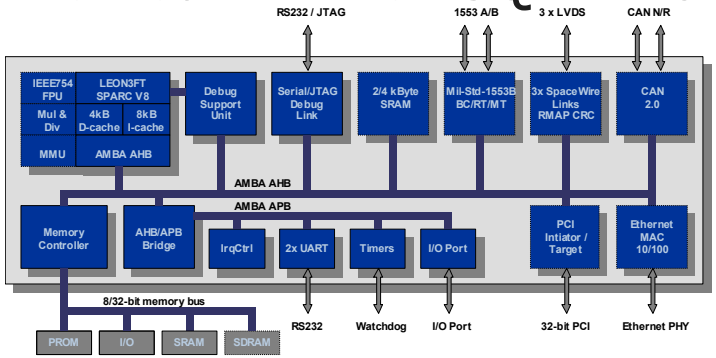
- LEON3FT processor core
  - 1.4 DMIPS/MHz
  - Multi-processor support (AMP/SMP)
  - Highly configurable
    - Cache size 1 – 256 KiB, 1-4 ways
    - Hardware Mul/Div/MAC options
    - Memory Managament Unit
    - Floating-point unit (high-perf or low area)
  - Truly portable between technologies and tools
  - On-chip debug support unit with trace-buffer
  - Detect and correct SEU in all on-chip RAM memories:
    - Register file correction of up to 4 errors per 32-bit word
    - Cache memory error-corretion of up to 4 errors per tag/word
    - Autonomous and software transparent error handling
  - Certified SPARC V8 by SPARC international



Custom SoC in Space-Grade Devices

RTAX-S/SL, RT3PE, V5QV

- Why? – (Re-)Use of software. System typically has SRAM/ SDRAM, SpaceWire, MIL-STD-1553B and various low-speed interfaces. Some form of accelerator or critical function implemented in FPGA fabric.
  - VHDL template designs, netlist, or preprogrammed
- LEON3FT 32-bit SPARC V8 processor implemented on Microsemi RTAX2000S/SL and RT ProASIC3 FPGA
  - RTAX: 20 DMIPS and 4 MFLOPS @ 25 mHz
  - RTAX: 25 MHz, 500 mW at 100% load, 380 mW in power-down
- LEON3FT implemented in Virtex-5QV – 70 DMIPS, 50 MFLOPS @ 50 MHz



Virtex-5: Single/dual core, full UT processor

Fitting a full Cobham UT699/UT700 processor

Design	Slice logic utilization		Slice logic distribution	Specific feature utilization	
	Slice registers	*Slice LUTs*	*Occupied slices*	*36k BlockRAM*	*18k BlockRAM*
LEON3FT MIN	2702 (3%)	8070 (9%)	2686 (13%)	4	4
LEON3FT GP	**5714 (6%)**	**14780 (18%)**	**6593 (32%)**	**6**	**16**
LEON3FT HP	11715 (14%)	30652 (37%)	11860 (57%)	6	18
LEON3FT HP with GRFPU-lite	9720 (11%)	23693 (28%)	9408 (45%)	6	16
LEON3FT MIN dual processors	4074 (4%)	12638 (15%)	5838 (28%)	4	4
LEON3FT GP dual processors	**9770 (11%)**	**25277 (30%)**	**9702 (47%)**	**10**	**32**
LEON3FT HP dual processors	21781 (26%)	57220 (69%)	18258 (89%)	10	34
LEON3FT HP with GRFPU-lite, dual processors	**17991 (21%)**	**43413 (52%)**	**15438 (75%)**	**12**	**32**
UT699/UT699E configuration	**27401 (33%)**	**60428 (73%)**	**18079 (88%)**	**6**	**20**
UT700 configuration	**36405 (44%)**	**81043 (98%)**	**20452 (99%)**	**8**	**38**

- UT699: LEON3FT, CAN, PCI, Ethernet, SpaceWire, …
- UT700: UT699 + MIL-STD-1553B, SPI, EDCL

New LEON3FT FPGA Template Designs

- GRLIB contained several template designs that matched our predefined LEON3FT-RTAX configurations:

Standard configurations

Configuration name	Instrument Controller -1	Instrument Controller -2	Spacecraft Controller -1	Spacecraft Controller -2	Spacecraft Controller -3	Spacecraft Controller -4	Payload Controller -1	Payload Controller -2
Configuration ID (CID)	1	2	3	4	5	6	7	8
LEON3FT Integer Unit	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Hardware multiply & divide					Yes	Yes		Yes
Power down mode	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Memory Management Unit					Yes	Yes		
Floating Point Unit	Yes	Yes	Yes				Yes	Yes
Debug Support Unit	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
UART Debug Link	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
JTAG Debug Link								
On-Chip Memory	4 kBytes		4 kBytes					
1553 RT	1							
1553 BC/RT/MT			1					
SpaceWire		2		3	2		2	
CAN 2.0B	1				1			

- New addition: leon3-ftfpga: New template that is configurable to create all of Cobham Gaisler standard product configurations.
  - One shared core design with different top-levels and config files
  - Attempt to speed-up creation of custom variants while keeping the predefined configurations
  - Predefined configurations updated with new IP and features
  - Currently for RTAX and RT3PE. Extension to additional targets.

LEON3FT in Virtex-5QV

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- Add-on package to GRLIB
  - Adds example/template designs, build targets and documentation. Users select between Xilinx GUI flow and GRLIB CLI flow
  - Template design 1 with LEON3FT, FTMCTRL, PCI, SpW, CAN 1553, Ethernet and system peripherals
  - Template design with LEON3FT, FTDDR2SPA, PCI, Ethernet, system peripherals
- Virtex-5 FX130 numbers:
  - LEON3FT with peripherals
  - Configurations defined in [1]
  - Also includes GPTIMER, UART, IRQCTRL, AHBUART, AHBSTAT, and FTMCTRL
  - LEON/GRLIB SoC: 8% to 30% of FPGA (slice LUTs)

Design	Slice logic utilization		Slice logic distribution	Specific feature utilization	
	Slice registers	*Slice LUTs*	*Occupied slices*	*36k BlockRAM*	*18k BlockRAM*
LEON3FT MIN	2702 (3%)	8070 (9%)	2686 (13%)	4	4
LEON3FT GP	5714 (6%)	14780 (18%)	6593 (32%)	6	16
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LEON3FT HP with GRFPU-lite	9720 (11%)	23693 (28%)	9408 (45%)	6	16

•[1] http://www.gaisler.com/products/grlib/guide.pdf

LEON3FT in RTG4

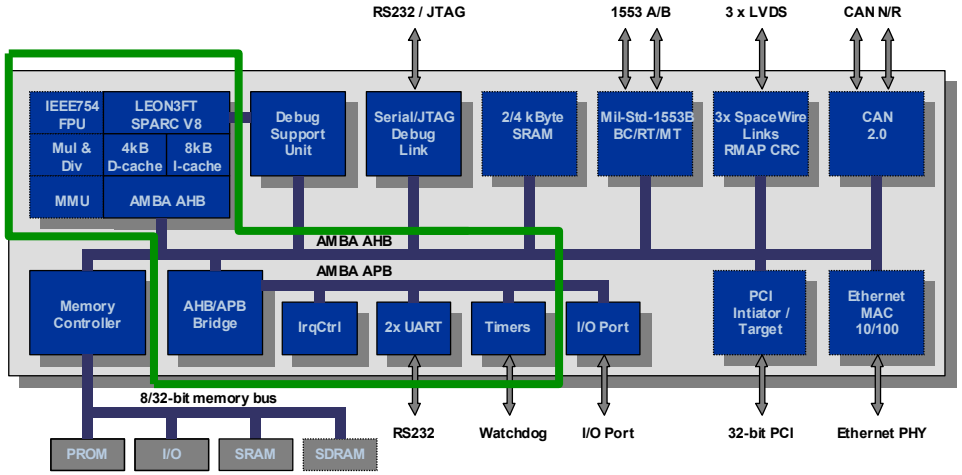
- Add-on package to GRLIB
  - Adds example/template designs, build targets and documentation.
  - Template for Microsemi RTG4 Development board
- Standard GRLIB already contains designs for IGLOO2 starter kit, SmartFusion2 Development Kit, SmartFusion2 Advanced Development kit
- Bridges included to interface with hard subsystem. LEON3FT can execute from Microsemi FDDR controller
- Ethernet via SGMII supported
- Currently working on flow where Microsemi IP wrappers are pregenerated

Design	4LUT	DFF	Logic Element
LEON3, 2 windows, no cache	2521 (1.7%)	1196 (0.8%)	2557 (1.7%)
LEON3 MIN system	4967 (3.3%)	1686 (1.1%)	5029 (3.3%)
LEON3 GP system	13021 (8.6%)	5026 (3.31%)	13371 (8.8%)
LEON3 HP system	31041 (20.5%)	10084 (6.6 %)	32002 (21%)

LEON3FT example implementations

- Post-Layout resource usage for small SoCs (processor, timer unit, UART, interrupt controller). Note: no memory controller.

Design	4LUT	DFF	Logic Element
LEON3, 2 windows, no cache	2521 (1.7%)	1196 (0.8%)	2557 (1.7%)
LEON3 MIN system	4967 (3.3%)	1686 (1.1%)	5029 (3.3%)
LEON3 GP system	13021 (8.6%)	5026 (3.31%)	13371 (8.8%)
LEON3 HP system	31041 (20.5%)	10084 (6.6 %)	32002 (21%)



Design	RT4 4LUT	RTG4 DFF	RTG4 Logic Element	V5 Slice registers	V5 Slice LUTs	V5 Occupied Slices
LEON3, 2 windows, no cache	2521 (1.7%)	1196 (0.8%)	2557 (1.7%)	1070 (1%)	1716 (2%)	680 (3%)
LEON3 MIN system	4967 (3.3%)	1686 (1.1%)	5029 (3.3%)	1481 (1%)	3701 (4%)	1495 (7%)
LEON3 GP system	13021(8.6%)	5026 (3.31%)	13371 (8.8%)	3944 (4%)	8441 (10%)	3149 (15%)
LEON3 HP system	31041 (20.5%)	10084 (6.6 %)	32002 (21%)	8276 (10%)	19672 (24%)	6756 (32%)

•MIN, GP and HP processor configurations are defined in: http://www.gaisler.com/products/grlib/guide.pdf

Summary of latest additions

- New leon3-ftfpga template designs
  - Replaces leon3-rtax-cid* designs
  - Intended to make it easier to develop custom designs
- Extensions to FT-FPGA to support built-in EDAC on RTG4 and Virtex5
  - Current support in SYNCRAMFT*, FTAHBRAM
  - New support for LEON3FT tightly coupled memory (with EDAC)
- Template design for GR-CPCI-XC7K
- New IP core features. LEON-REX, optimized L1 cache coherency implementation, GRDMAC extensions, partial reconfiguration support extensions.

Roadmap – GRLIB IP Library

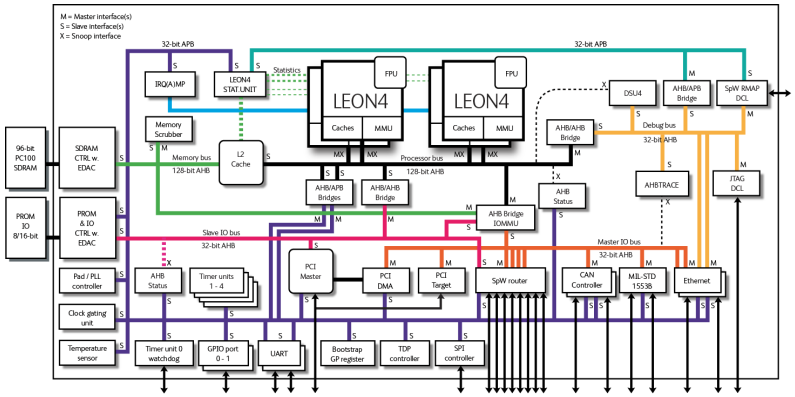
Infrastructure, general extensions

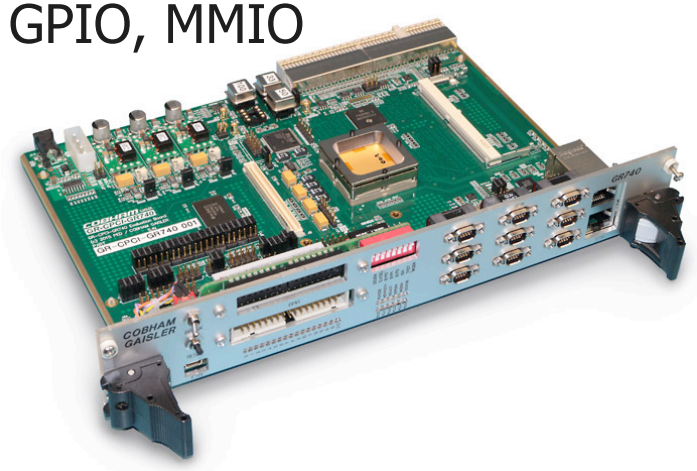
- Continuous improvements
  - New Kintex board. Development of IGLOO2 based FPGA board
  - IP core extensions to further take advantage of RTG4 built-in SRAM ECC and hard subsystem
  - Support for new generation technologies (BRAVE and others)
  - Support for high speed serial links using SerDes macros
- Accellerate the development
  - Rapid prototyping: Further development of examples and template designs to allow rapid design start.
  - Rapid debugging: Real time tracing and extensions to on-chip debug support
- Transition GRLIB to fully Tcl based infrastructure – move away from shell scripts and Make
- Tool integration: Use GRLIB IP as block in vendor flows

Roadmap – Complementing developments

Leverage new developments and FPGAs

- GR740 + FPGA
- Options for interconnect without external active parts:
  - Legacy PCI (33*32 Mbit/s)
    - GRPCI2 IP core in FPGA
  - Aggregated SpW (2*8*200 Mbit/s) with RMAP
    - GRSPW2 in FPGA
  - Ethernet w/o PHY (2*2*1 Gbit/s)
    - GRETH_GBIT in FPGA together with PHY replacement
  - Low speed alternatives: SPI, UART, GPIO, MMIO



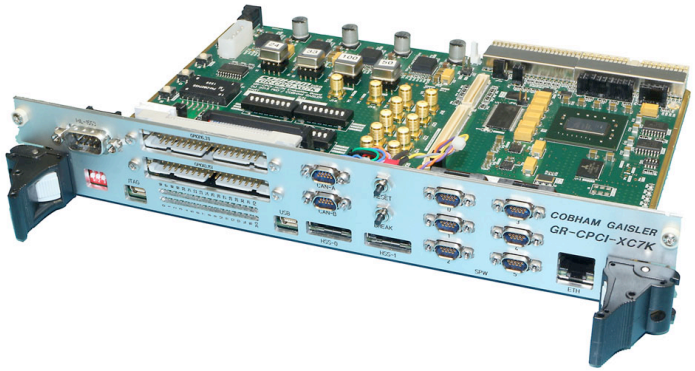


Roadmap - New FPGAs – New opportunities

- Level-2 cache targeted for FPGA and LEON3FT
  - Currently in GR740 and commercial SoCs
- Transfer next-generation processor plans to ”production status” on FPGA
  - Parallelize data paths between CPUs and off-chip memory
  - Extend hardware support for virtualization / partitioning
- Introduction of high-speed serial links requires SoC design adaption
- Transition to new bus protocols and topologies
  - Does not necessarily prevent AMBA 2

Conclusion

- GRLIB IP library is continuously expanded
  - Template designs reworked
  - Support for new target technologies being added
  - Existing IP is being extended. New IP is added.
- Focus of updating library to increase productivity of designers – and then of the design end-users.
- New boards:
  - GR-CPCI-XC7K Kintex board
  - IGLOO2 version in development



- Dynamic partial reconfiguration support: Feedback wanted!