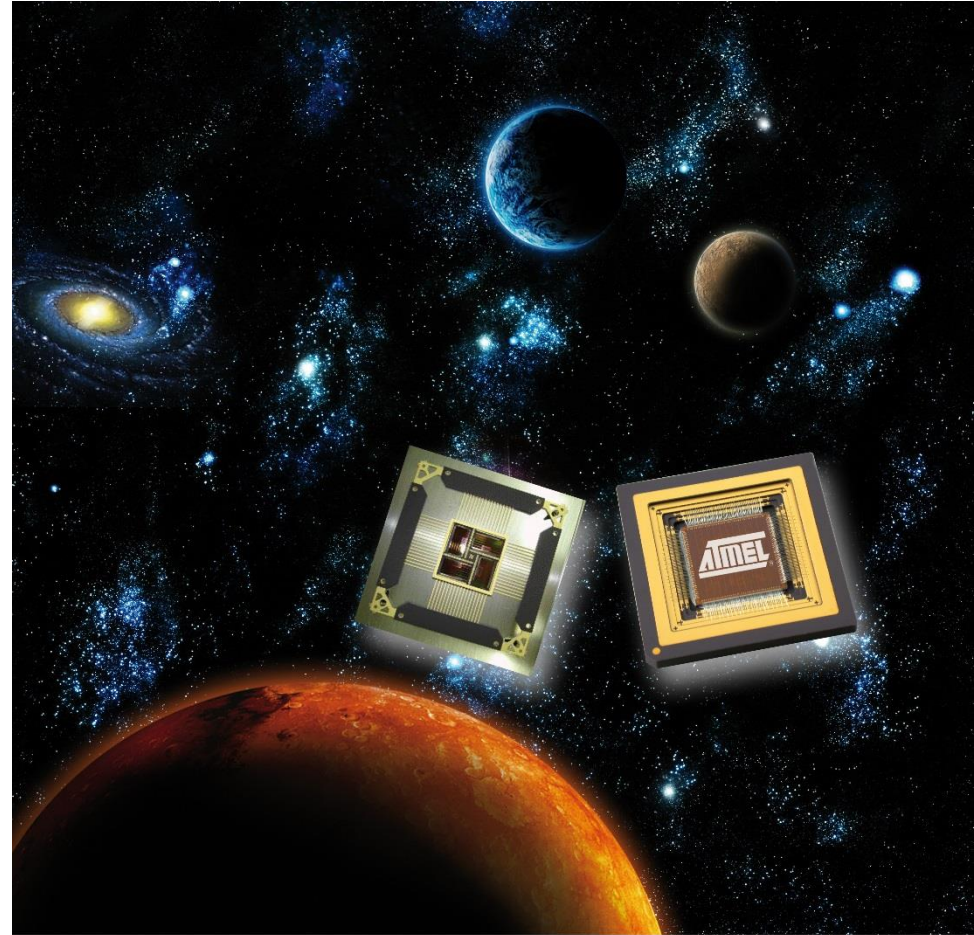




AT40K FPGAs Platform for SPACE APPLICATIONS

Mar-2016 SEFUW



Summary

ATMEL FPGA Platform

1. AT40K general offer
2. Tools: Space FPGA Designer
3. Module 16Mb NVM
4. Reconfigurable Processor

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AT40K offer

RHBD Design

- Radiation Hardened By Design, no need for mitigation

AT40KEL

- 40K gates equivalent

AT17LV010

- 1Mb serial EEPROM, companion chip

ATF280

- 280K gates equivalent

AT69170

- 4Mb Serial EEPROM, companion chip

ATFee560

- Module with 2 ATF280 and 2 EEPROM AT69170

AT69180

- 16 Mb EEPROM module for BRAVE using 4 AT69170

ATF697

- Reconfigurable Processor module with ATF280 and AT697F Leon2FT

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SpaceFpgaDesigner

Mentor Precision

AT40K Synthesis tool

- OEM version available from Atmel
- Contract renewed for 3 years
- VHDL / Verilog entry
- Automatic Figaro Macro soft macro detection and mapping

Enhancements

- New Reset and Clock signals handling
 - Provides better density and limits manual signal allocation
- Better soft macro detection and mapping
 - New Multiplexers and Multipliers configurations
- Efficient Tristate Bus mapping
 - Option to use tri-state logic instead of multiplexers structure
- VHDL post-synthesis simulation library

SpaceFpgaDesigner

Atmel Figaro

AT40K Place and Route tool

- Comprehensive set of soft macro generators
- Automated Place and Route
- Static Timing Analysis

Continuous enhancement through quarterly release

- Static Timing Analysis
 - multi cycle path constraints support
 - min/max path delay exceptions support
 - memory usage & run-time
- Batch command
 - manual placement
- User experience
 - Updated simulations libraries
 - Linux and Windows wrapper script
 - Runs Reproducibility
 - Regional setting support

Trainings organised regularly at Atmel Nantes

SpaceFpgaDesigner

Hardware Macro

Provide pre placed and routed IP's

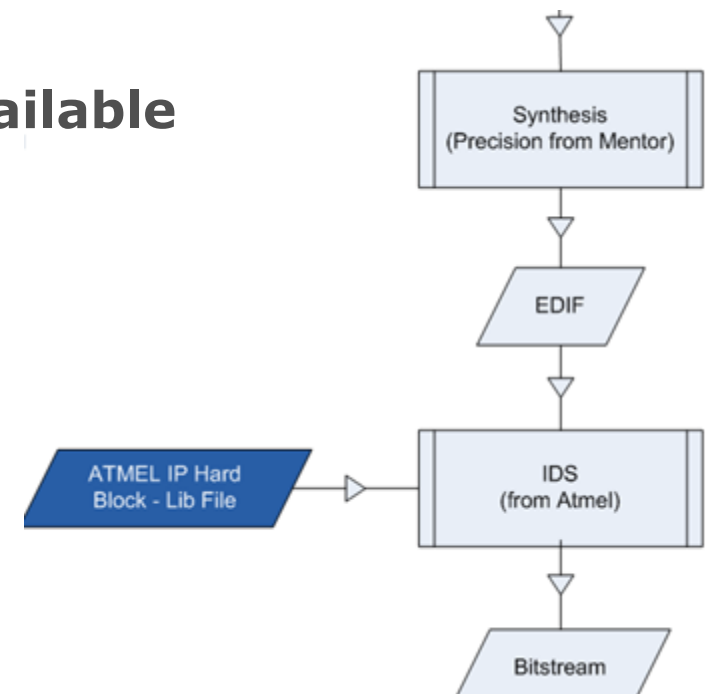
- Guaranteed performances
- Simulation files with high coverage level
- Validated on board

1553-RT from Maya Technologies Available

- MIL-STD-1553B Notice II Compatible
- 28.5 % of an ATF280 matrix
- 12 MHz

Ongoing / Forecasted

- SpaceWire
- PCI
- CAN



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Module 4 x 69170F

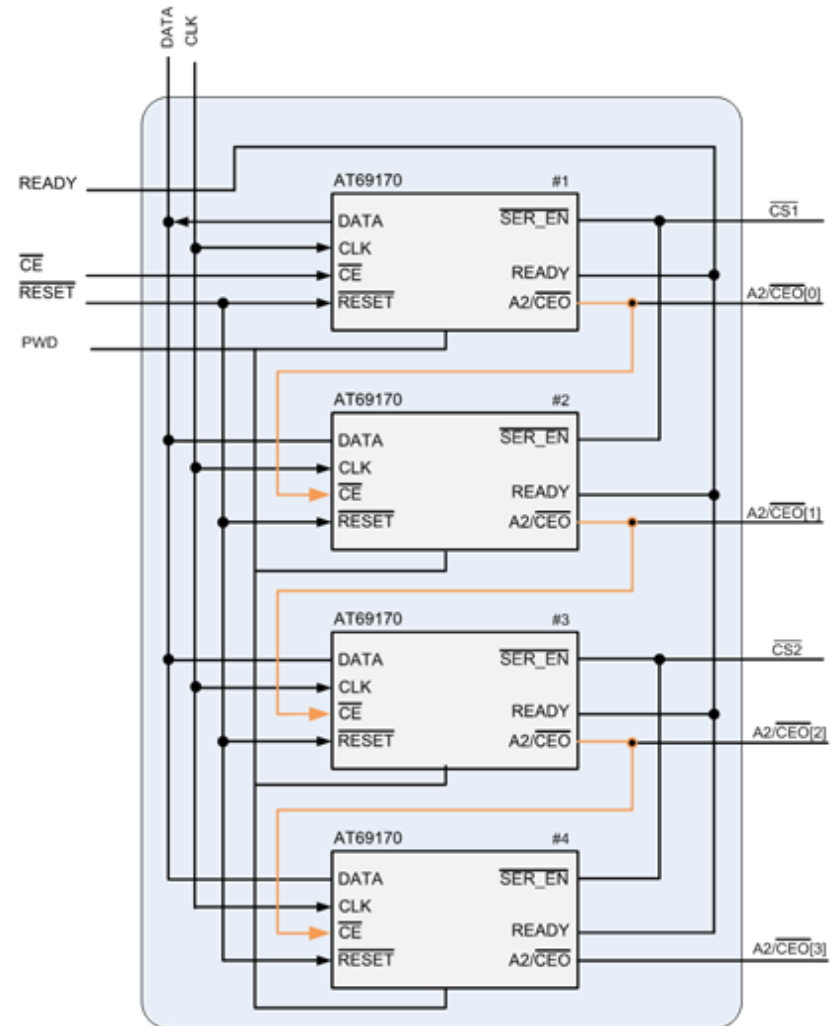
Motivation

- A new generation FPGA (BRAVE) is under development in the frame of a CNES and ESA program.
- The required size of the NVM is 16Megbits
- Technical approach is the reuse of AT69170F NVM (serial 4Mbit) in a Multi Chip Package

Architecture

Serial Configurator

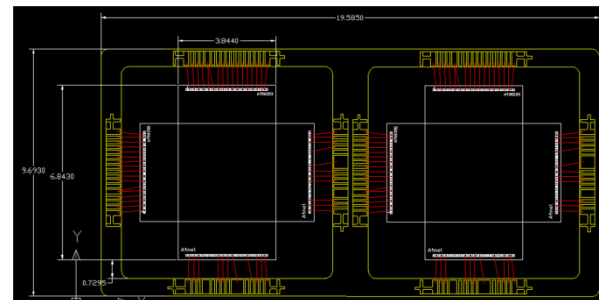
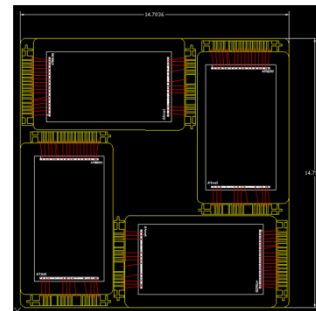
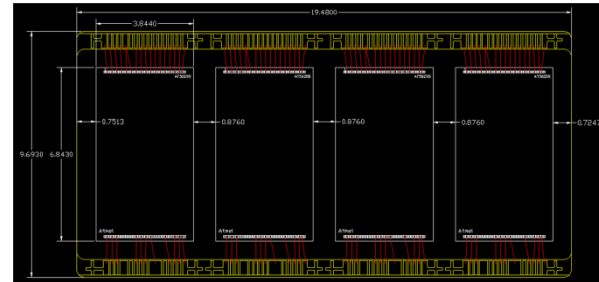
- Architecture of the module
 - 4x 4 Mbits On-Chip Flash Array
 - 4x PWD signals connected together and to be tied to GND (as for AT69170 in standalone mode)
 - 4x Open Drain READY signals connected together to inform FPGA of the availability of the memories
 - A standard cascade architecture
 - 4x AT69170F dies cascaded for dump mode
 - 2x chip selects for TWI interface management
 - Need for the 4 address bits (A2/CEOn) to map correctly the devices when in TWI mode
- Strength
 - Standard already validated on-board architecture
 - Configuration tools already available



Package

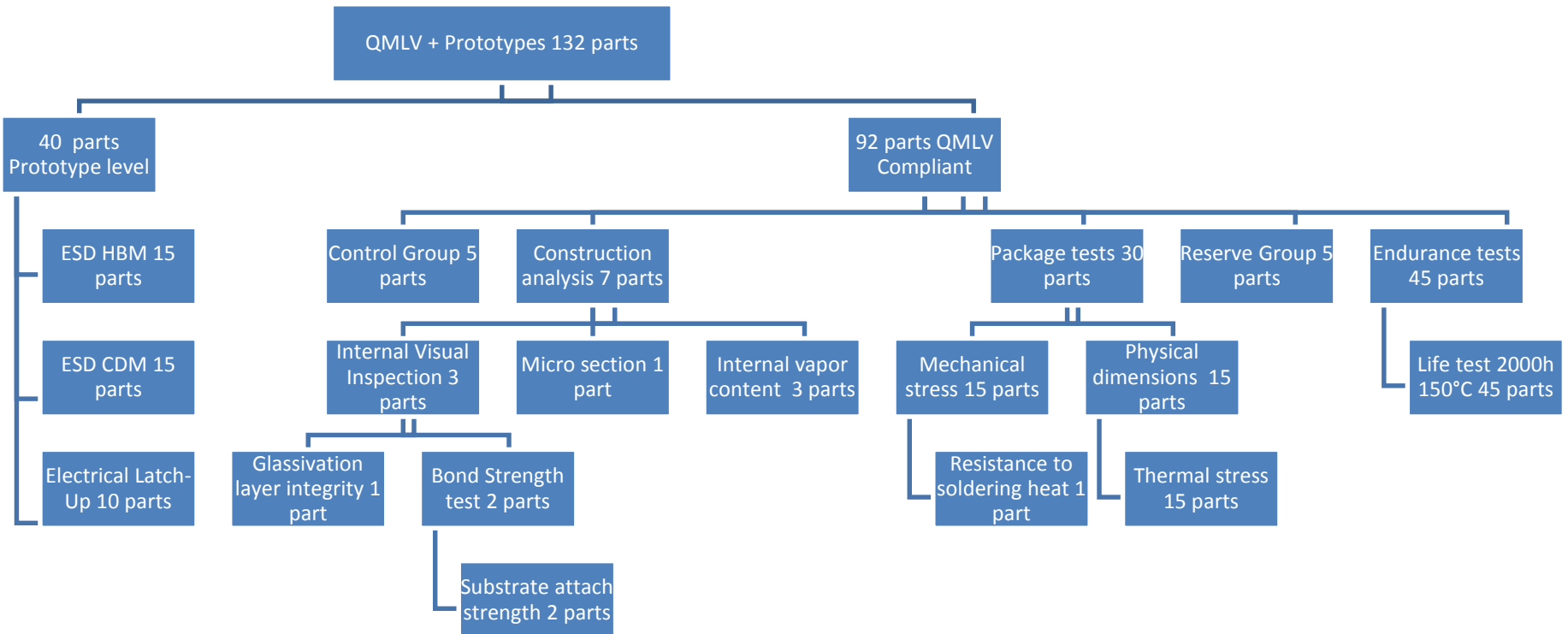
Configuration

- 3 possible package configurations :
- Side by side in Line Package
- Cavity size : $\sim 19.5 \times 9.7 \text{mm}$ (189mm^2)
- Qualification status : reuse of existing qualified technologies
- Side by side in Square package
- Cavity size : $\sim 14.7 \times 14.7 \text{mm}$ (216mm^2)
- Qualification status : reuse of existing qualified technologies
- Stacked 2 x 2 , Side by side in Line or Side by side in Square Package
- Cavity size : $\sim 19.5 \times 9.7 \text{mm}$ (189mm^2)
- Qualification status : Stacked dice process not qualified
- 3 D solution later on



ESCC Evaluation Test Plan

ESCC 2269000



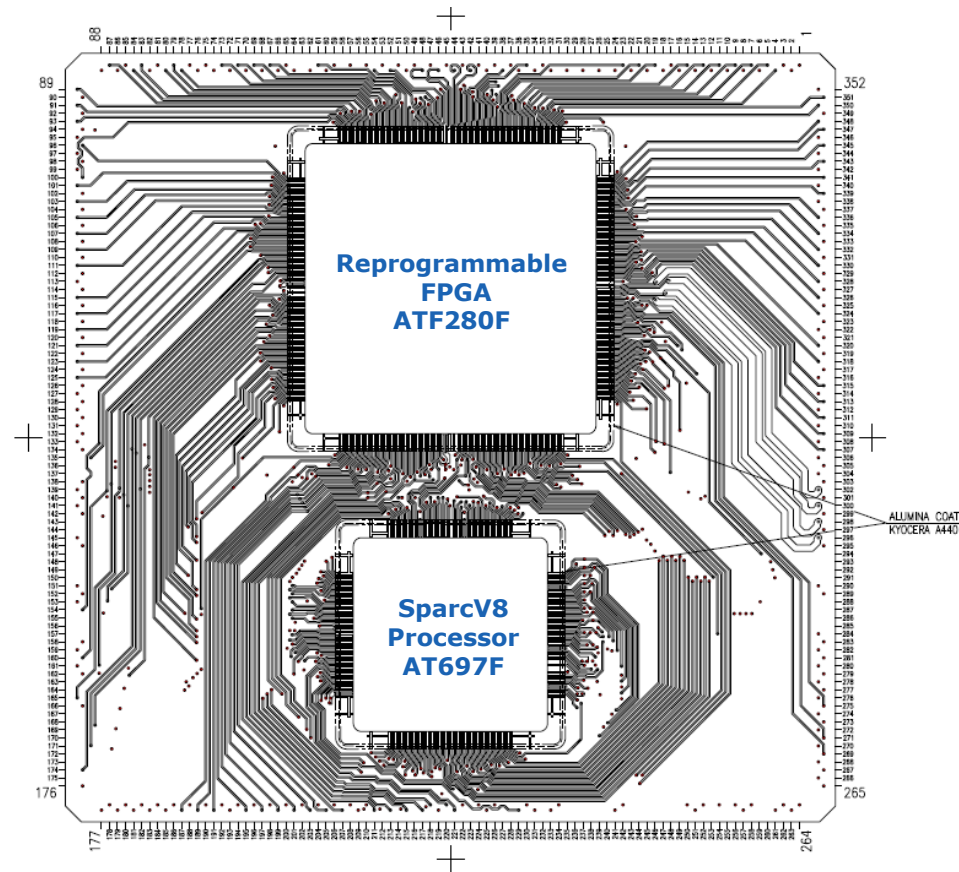
Summary

ATMEL FPGA Platform

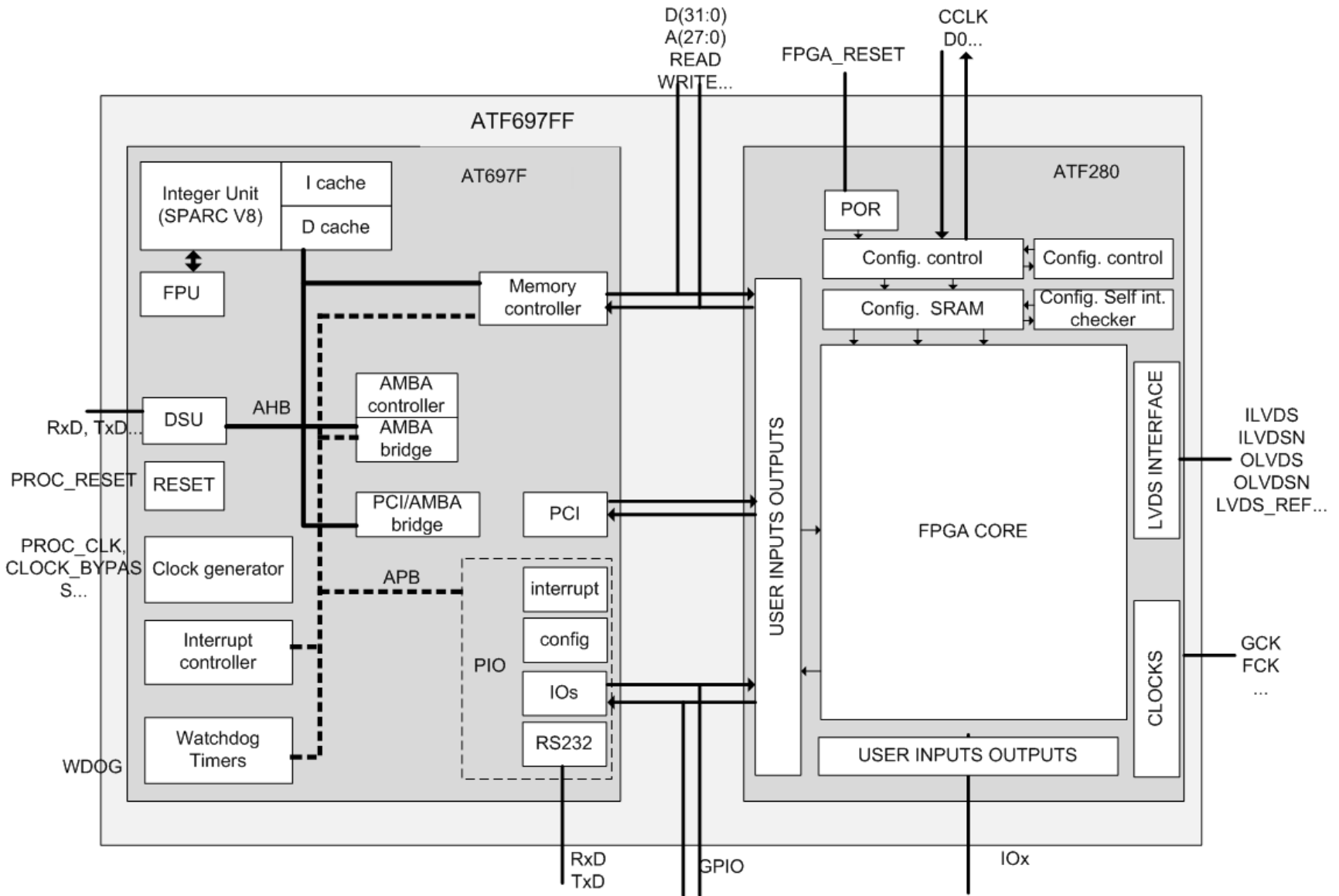
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ATF697FF Reconfigurable Processor

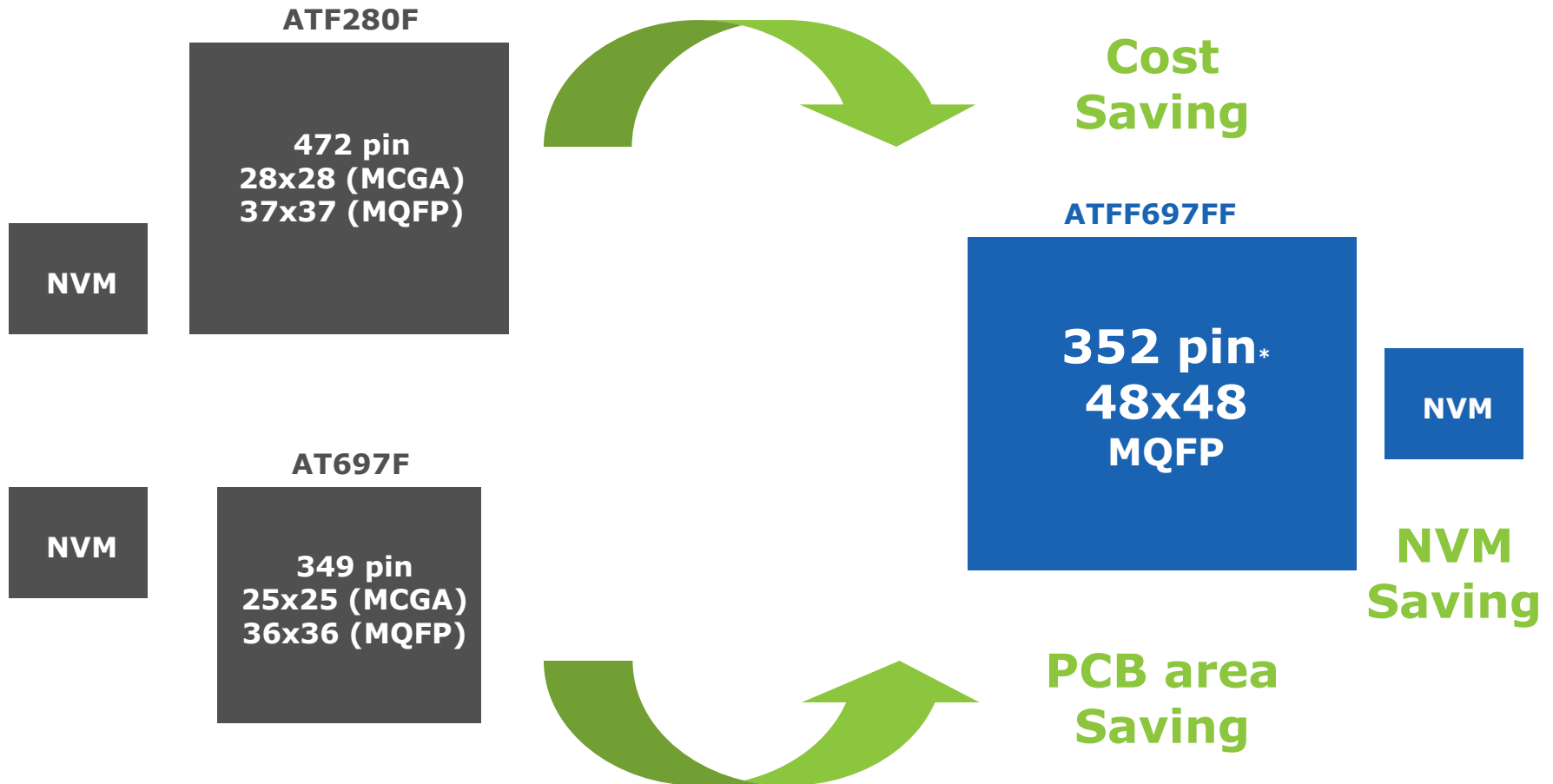
- Combined **Rad Hard Processor + FPGA**
 - **SPARC V8 Processor**
 - AT697F LEON2-FT 100Mhz
 - Powerful & Low Power
 - **Reconfigurable unit**
 - ATF280F SRAM based FPGA (280K)
 - Mapped on SPARC Memory Bus
 - Internal PCI link
- Multi-Chip Package CQFP 352
- Ready for SpaceWire
 - 4 LVDS transmitters & receivers
- Radiation
 - AT697F and ATF280 Legacy
- Operating range
 - 3.3V +/- 0.30V for I/O
 - 1.8V +/- 0.15V for Core
 - -55°C to 125°C
- QML-Q, QML-V and RHA grade



ATF697FF Block Diagram



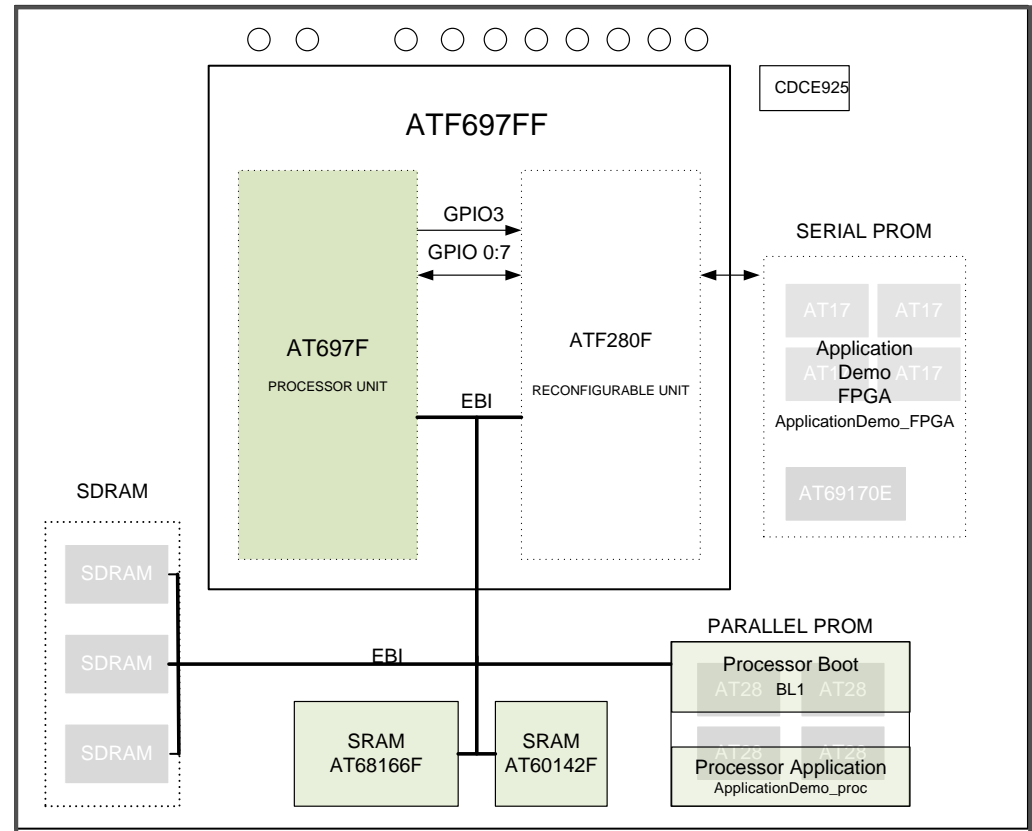
ATF697FF Multi Chip Package Savings



ATF697FF Processor / FPGA Combinations

Processor in master mode

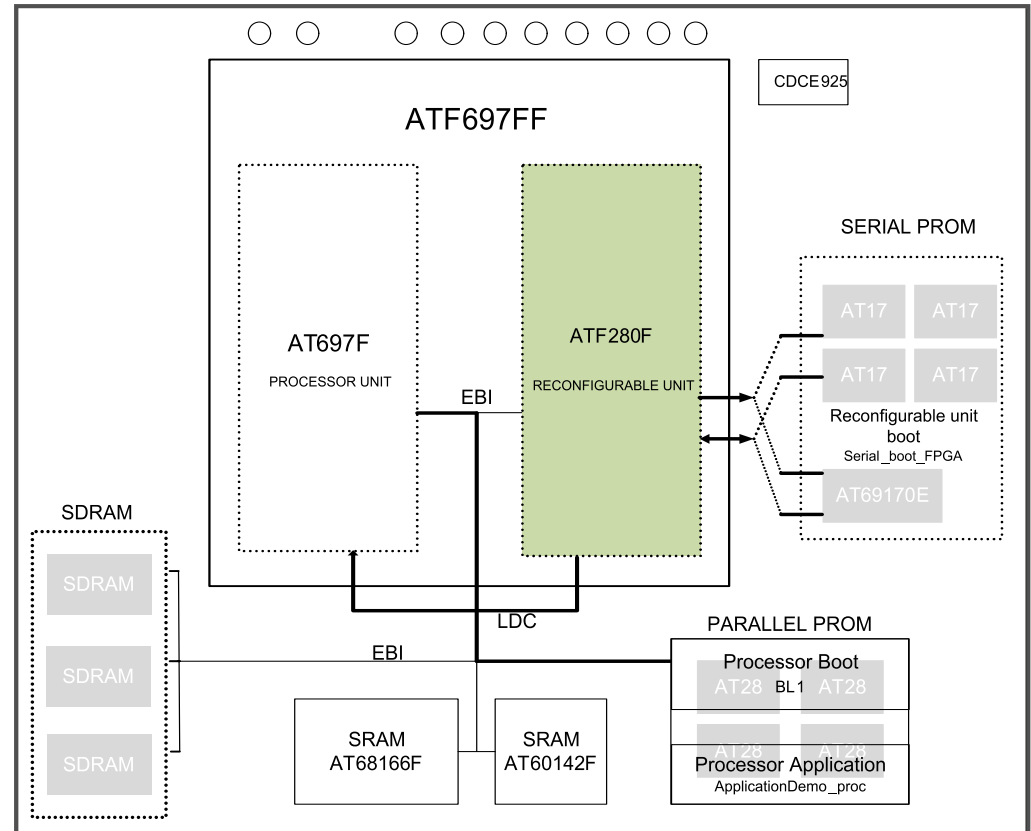
- Each code in its own NVM
- Processor booting 1st
FPGA kept under reset
- FPGA booting 2nd
- Insures Processor in control of FPGA application



ATF697FF Processor / FPGA Combinations

FPGA in master mode

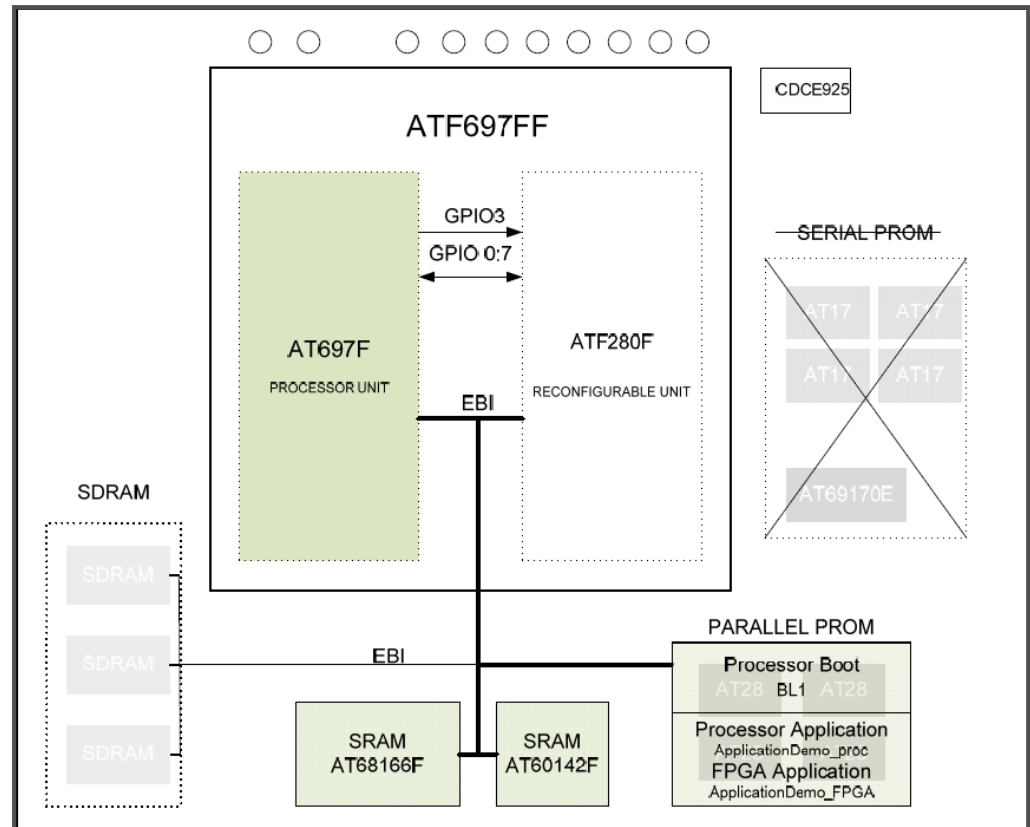
- Each code in its own NVM
- FPGA booting 1st
Processor kept under reset
- Processor booting 2nd
- Insure FPGA interfaces ready before processor start



ATF697FF Processor / FPGA Combinations

Processor in master mode / FPGA in dynamic mode

- All codes in Processor NVM
- Processor booting 1st
FPGA waiting
- Processor uploading FPGA
configuration through GPIOs
- FPGA running once
configuration uploaded
- Processor may upload new
FPGA configuration anytime
- Various use cases:
 - Multiple FPGA configurations
to perform different tasks
 - New (bugfix/updated) FPGA
configuration while keeping
old one as safe backup



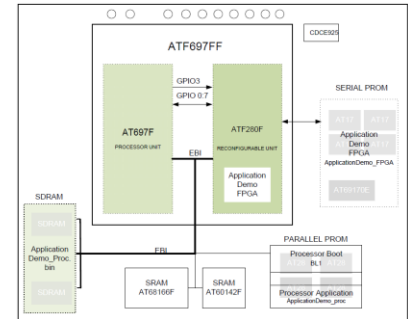
FPGA configuration (3Mb max) bit-rate:

- Serial @ 1/8th F_{cpu} => 250ms @ 100MHz
- Parallel @ 2/3rd F_{cpu} => 45ms @ 100MHz

ATF697FF Development Environment

Documentation

- Datasheet
- User Guide
- Application notes
- Training course



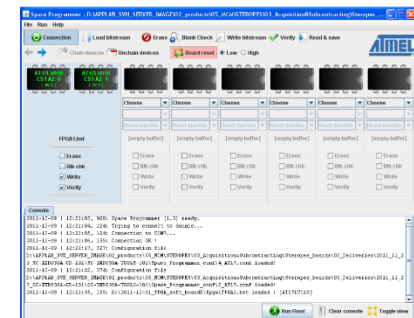
HW Demonstrator

- ATF697FF Hardware board, contains:
 - ATF697FF Reconf. Processor
 - AT68166/AT60142 16/4Mb SRAM
 - AT69170 4Mb serial EEPROM
 - AT17LV010 1Mb serial EEPROM

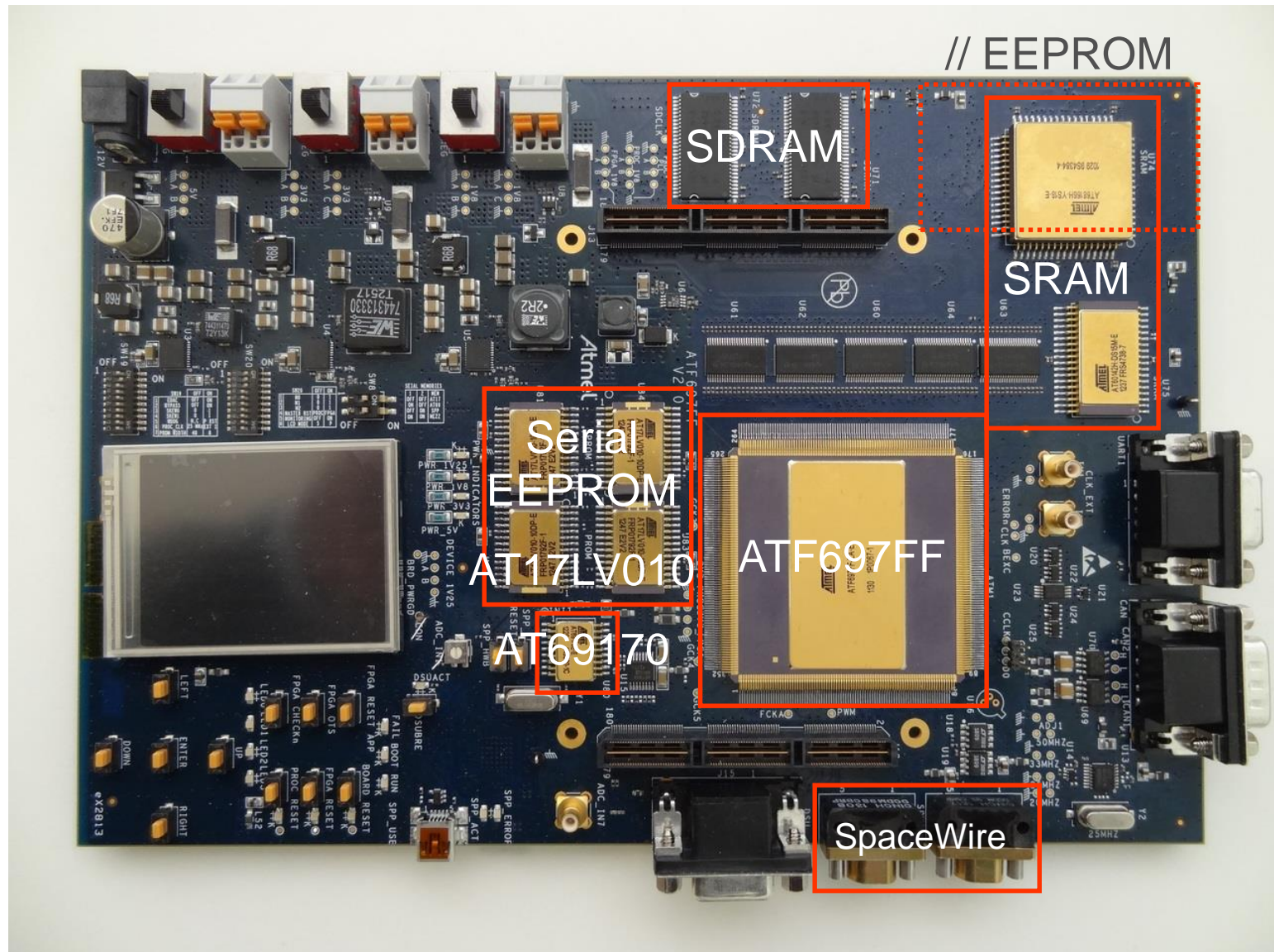


SW & Tools

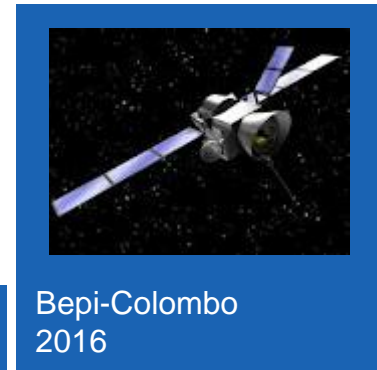
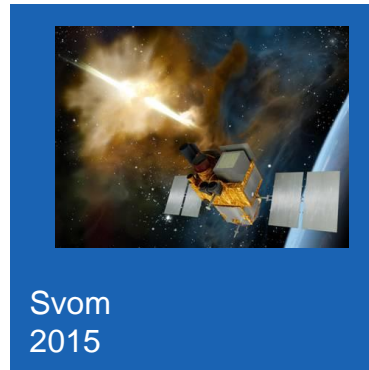
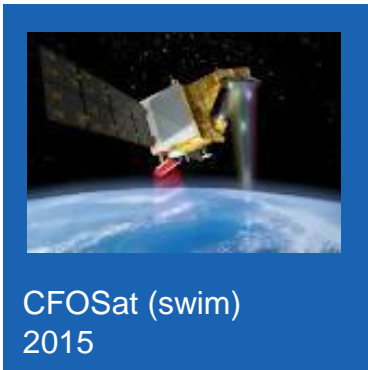
- SW IDE (Eclipse) / Compiler (GCC/GDB)
- SW demonstration code
- SW for FPGA design – IDS & MENTOR
- SW for debug – SDE
- Space programmer



ATF697FF Evaluation Board



FLIGHT HERITAGE & PLANNING TO FLY ...





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