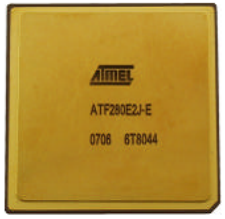
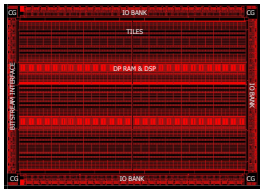
SEFUW: SpacE FPGA Users Workshop 3rd Edition



David Merodio Codinachs (ESA)
David Dangla (CNES)



WELCOME TO ESTEC

European Space Research and Technology Centre (ESTEC)

http://www.esa.int/SPECIALS/ESTEC/index.html

Sponsors

Coffee breaks and

Cocktail reception during the Demo Session are sponsored by

SEFUW Objective

Exchange of highly valuable information and experience among FPGA users, researchers, CAD vendors and FPGA vendors

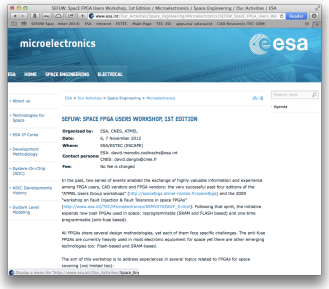
Precursor experiences and SEFUW editions

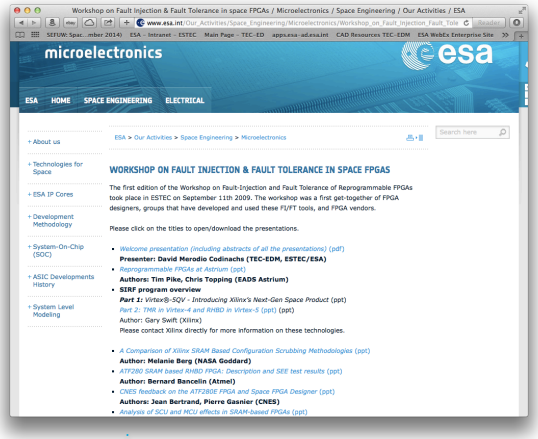
http://spacefpga.atmel-nantes.fr/spacefpga/

***ATMEL** Aerospace FPGA working group: Workshops and website*

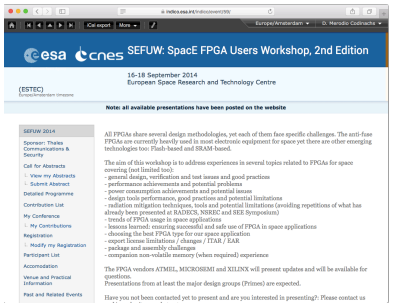
***Workshop** on Fault Injection & Fault Tolerance in space FPGAs (2009)*

*1st **SEFUW**, Oct **2012***





*2nd **SEFUW**, Sep **2014***



http://www.esa.int/TEC/Microelectronics/SEMV57KIWZF_0.html

FPGA updates/ trends

1. New FPGA vendors addressing space
2. Larger and higher performance FPGAs are becoming available
3. COTS FPGAs use is growing
4. FPGA domain usage expands:
    a. High performance using FPGAs
    b. Re-programmability (already addressed in previous SEFUW editions)

FPGA updates/ trends (I): FPGA vendors addressing Space

- ✓ Space FPGA vendors in SEFUW 2016 and also in previous SEFUW editions:

Atmel

Microsemi

XILINX
ALL PROGRAMMABLE™

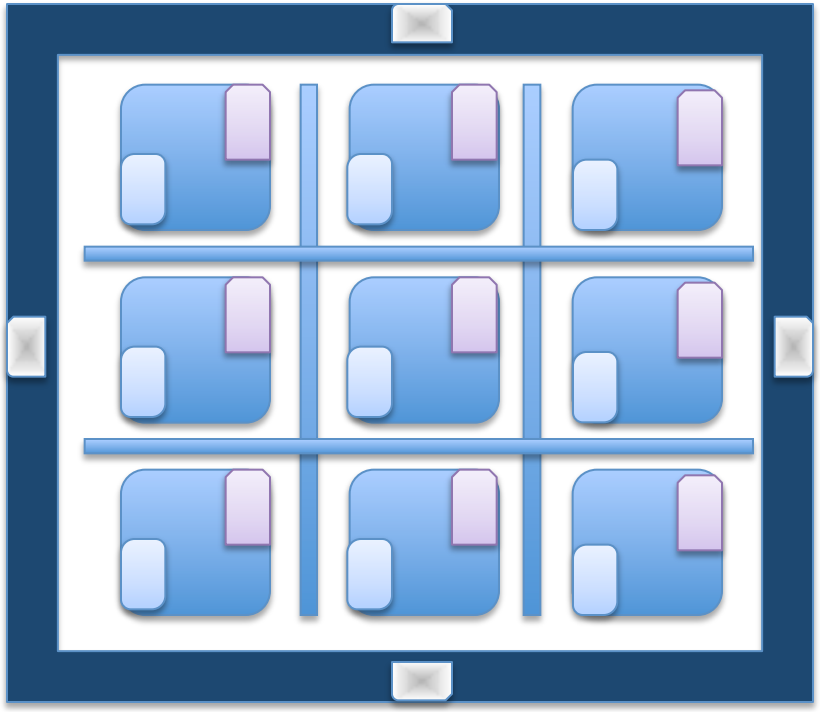
- ✓ NEW FPGA vendors for Space in SEFUW 2016:

ALTERA
now part of Intel

NANOXPLORE

FPGA updates/ trends (II): Larger and higher performance FPGAs (I)

1. FPGA *Architectural features* (general)



Logic fabric

Inter- connection

Internal memory

Clock generation (PLLs, DLLs,…)

Arithmetic (Multipliers, DSP, …)

Flexible IOs

High speed serial links

Embedded processors

Other hard-macros (PCIe, …)

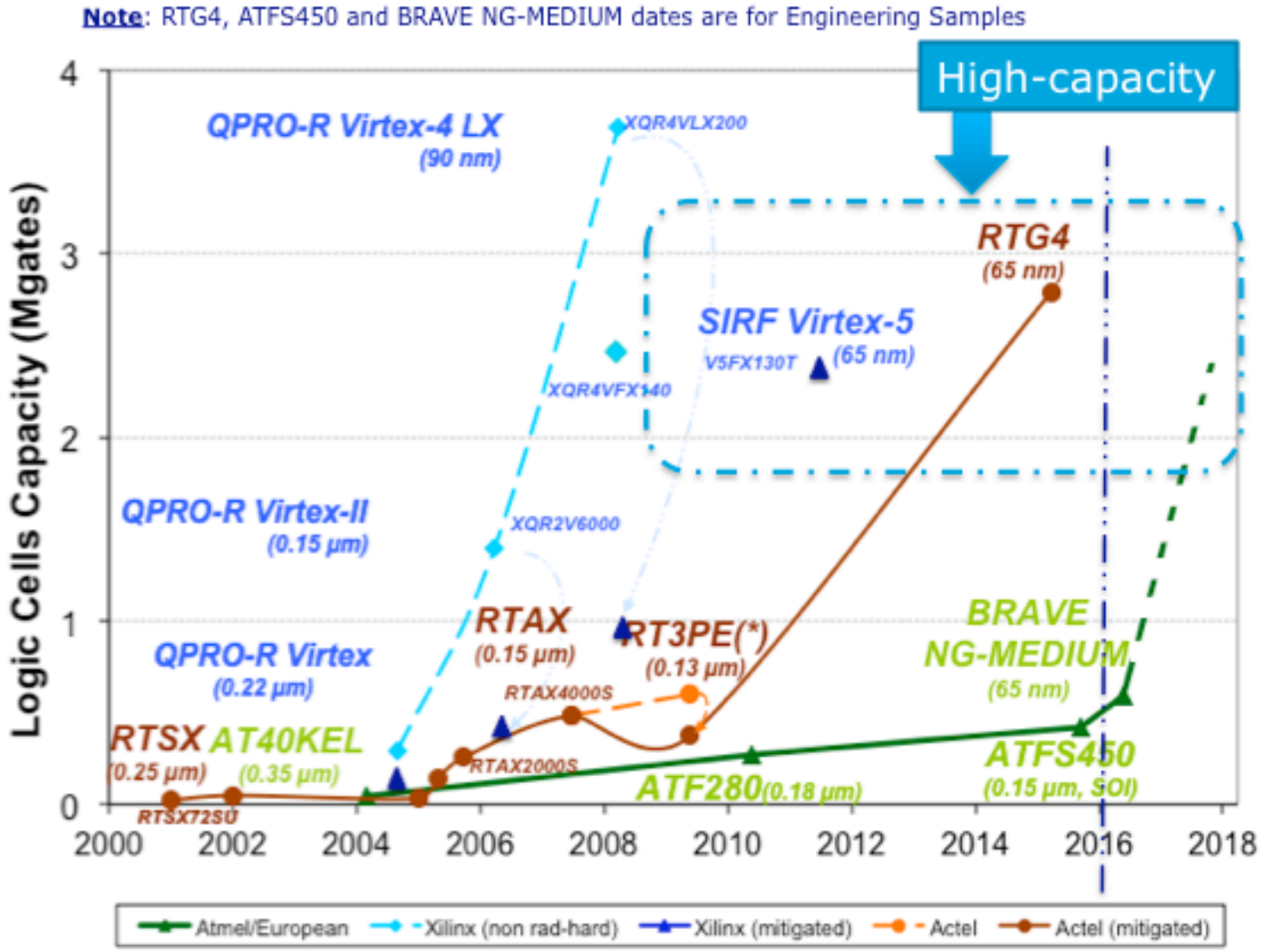
FPGA updates/ trends (II): Larger and higher performance FPGAs (II)

1. FPGA "Eras" (based in their architecture):

1. First: FPGA fabric (e.g. RTSX-SU)
2. Second: FPGA fabric and Internal Memory (e.g. RTAX-S, ATF280F)
3. Third: FPGA fabric, Internal Memory and specialized Hard-macros (DSP, etc). (e.g. Virtex-4/5, RTAX-DSP, RTG4, NG-MEDIUM)
4. Fourth: SoC FPGA (e.g. Zynq, Smartfusion2, Cyclone V SoC, Arria V SoC)

2. Radiation hardened FPGA and COTS FPGAs:
    1. COTS FPGAs: entered the 4th Era some years ago
    2. Radiation hardened FPGAs: "behind" the COTS timeline, but better radiation performance

FPGA updates/ trends (II): Larger and higher performance FPGAs (II)



FPGA updates/ trends (III): COTS FPGAs (I)

1. During subsystems development:

   COTS FPGAs are used for bread boarding (**BB**)

2. When moving to **EQM** and **FM** models, which FPGA is used? The "nominal" choice is:

   a. Radiation hardened FPGA: if the performance can be achieved

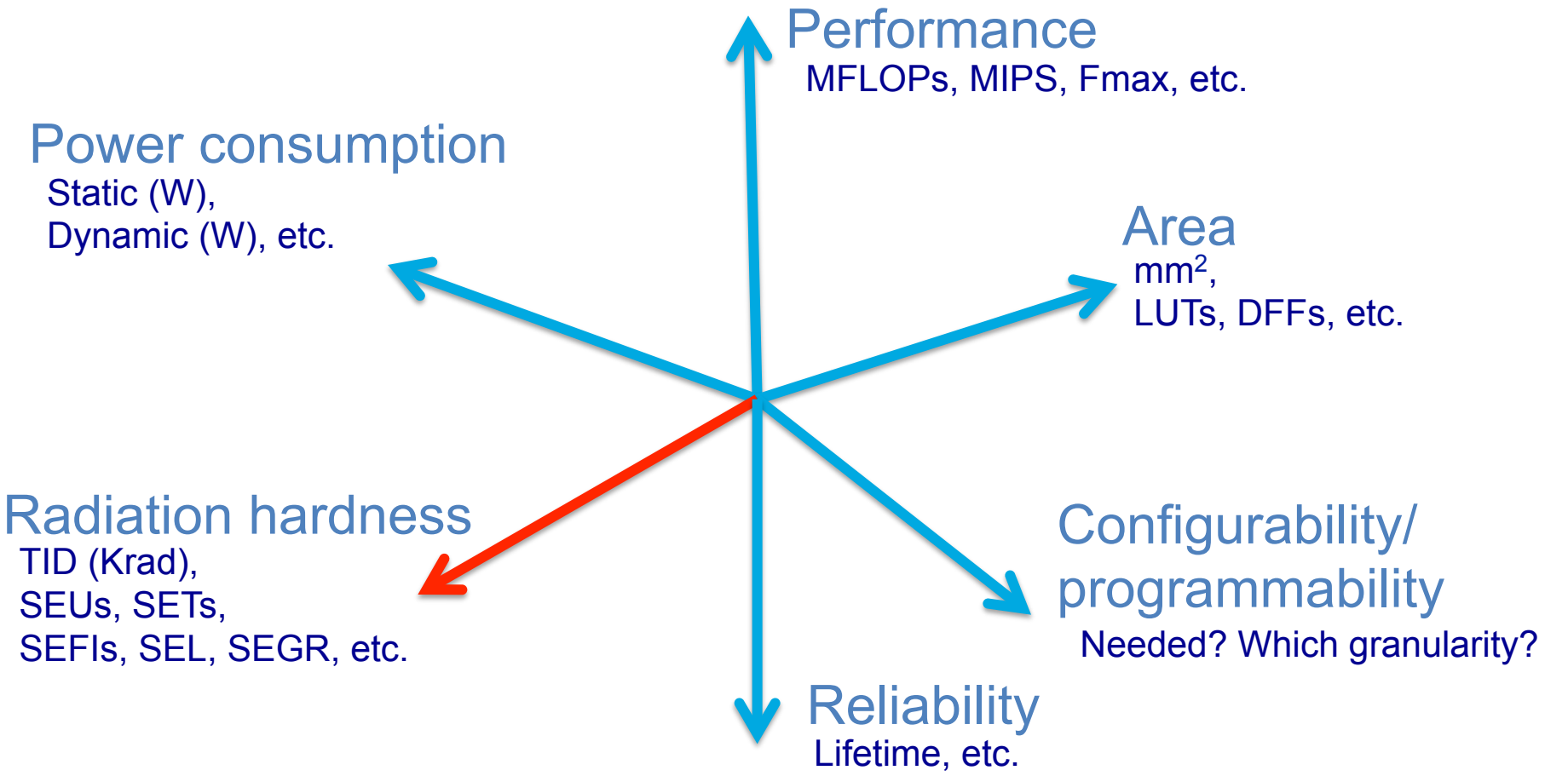
   b. ASIC: if the performance cannot be achieved

3. Due to the changing programmatic constraints (shorted lifetime, better-faster-cheaper, etc.). Specially relevant for **Nanosatellites** and **Cubesats**:

   a. COTS FPGA are proposed for EQM and FM

Understanding their radiation performance, mitigation techniques and guidelines on how to use them is paramount. The overall Quality (ECSS-Q-ST-60-13C) is paramount.

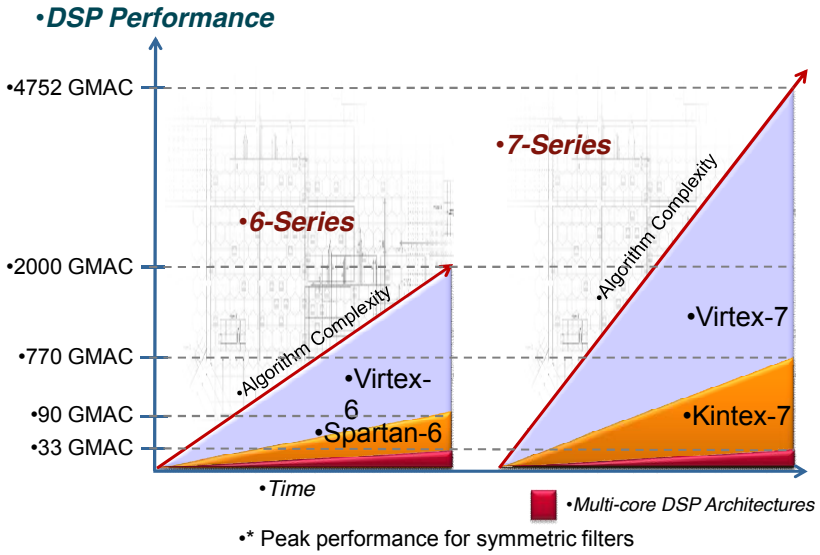
FPGA updates/ trends (III): COTS FPGAs (II)



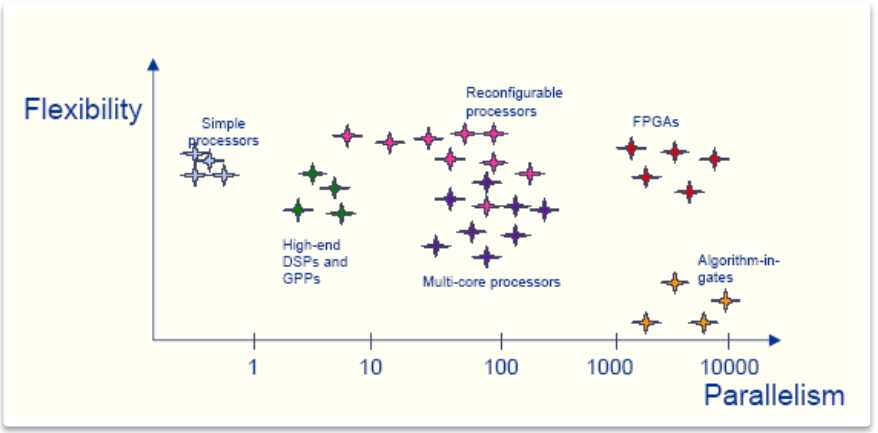
Also <u>VERY</u> important: Quality, Packaging, Mounting, ITAR/ EAR, Price …

FPGA updates/ trends (IV): Domain usage expands

1. Re-configurability, High Performance



Source: Xilinx

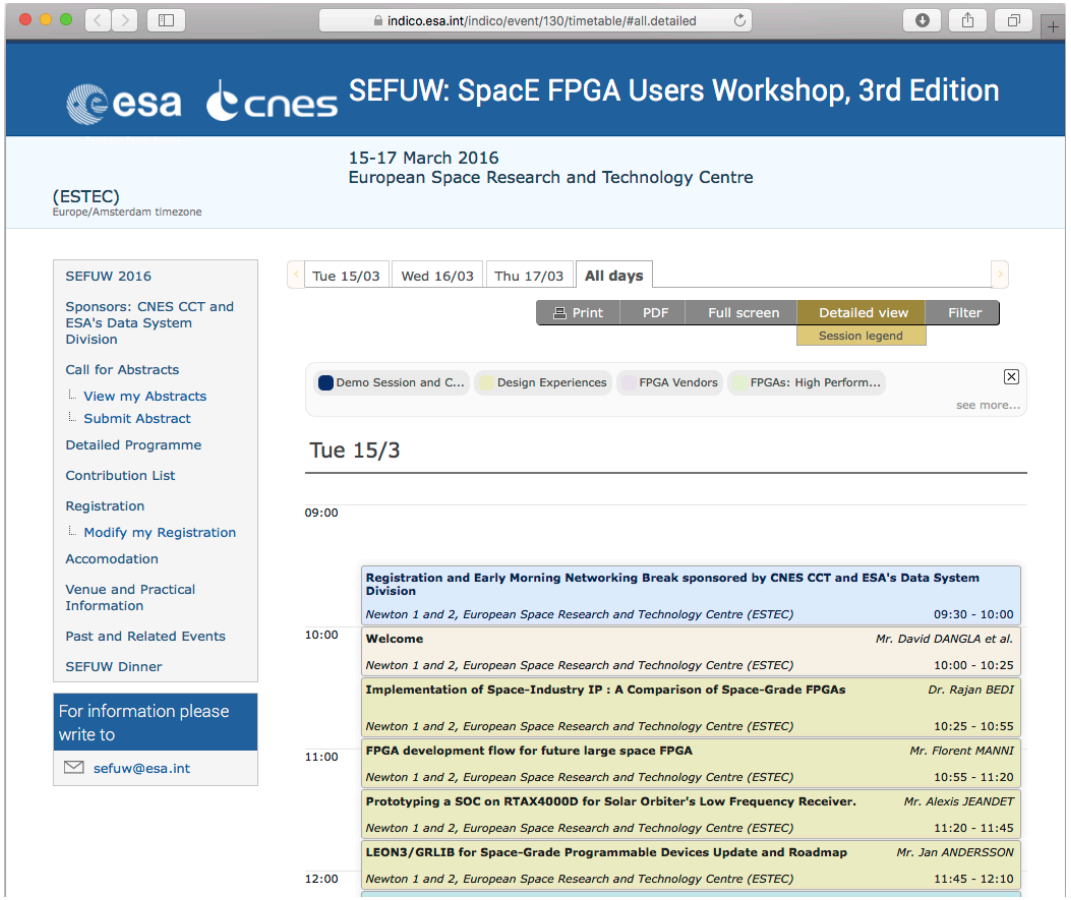


Source: BDTi, "Benchmarking Multithreaded, Multicore and Reconfigurable Processors", 2006

Agenda (I)

https://indico.esa.int/indico/event/130/timetable/#all.detailed

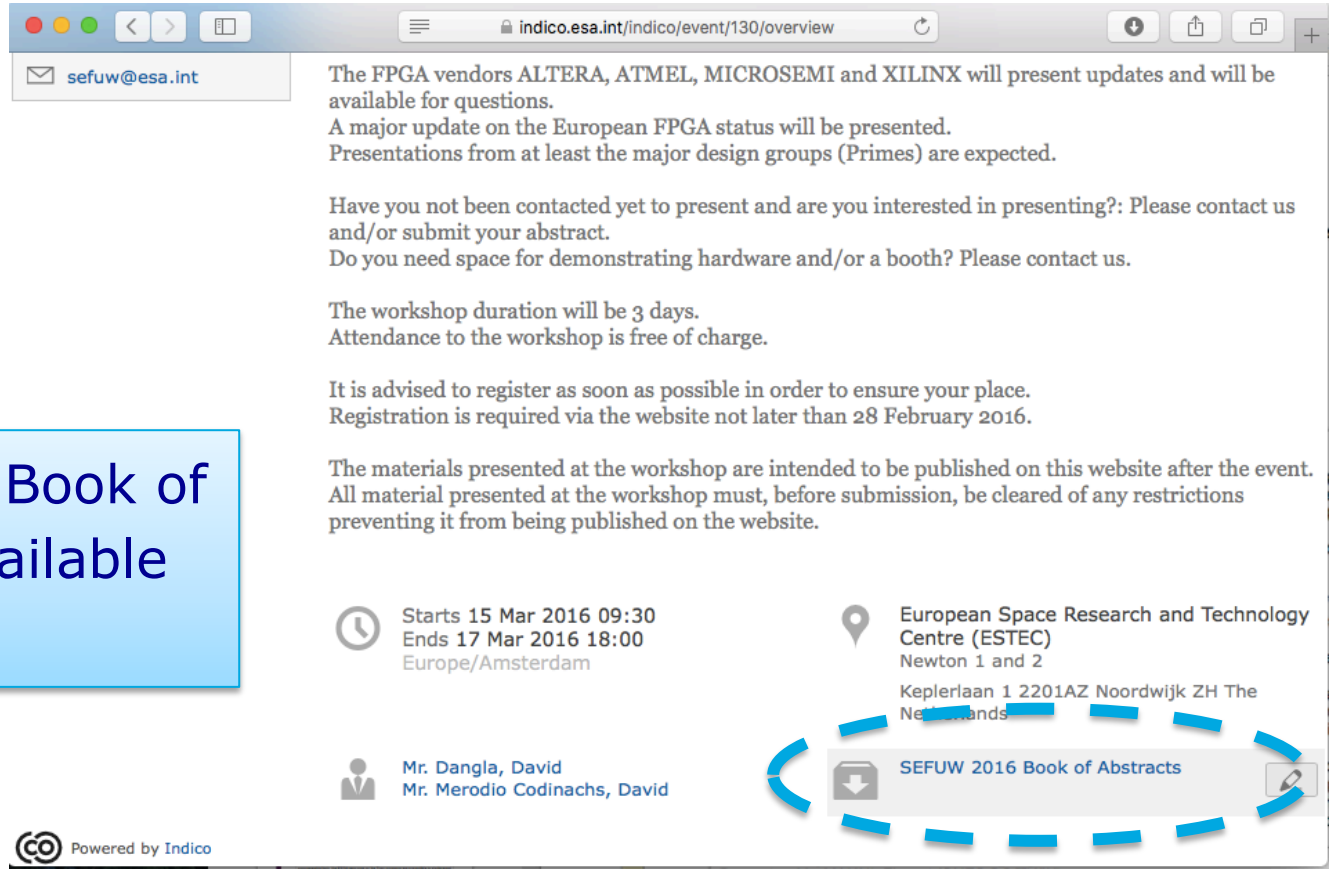
The agenda has been distributed among the participants



Agenda (II)

https://indico.esa.int/indico/event/130/timetable/#all.detailed

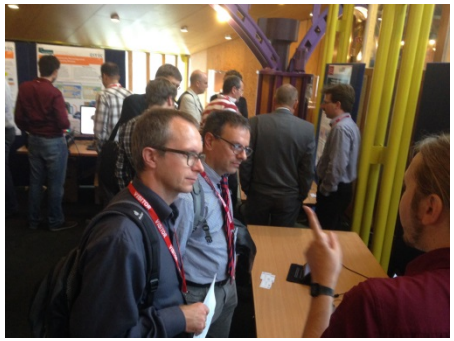
SEFUW 2016 Book of Abstracts: available online



Agenda (III)

1. **Sessions**:
    a. FPGA Vendors
    b. Design experiences
    c. Industry experiences
    d. FPGAs: High Performance
    e. Reconfigurability
    f. Radiation
    g. Fault Tolerance Methodologies

2. **Demo** session



Notes: pictures from the DEMO session of the previous SEFUW

Organization notes

1. **Presenters**:
    a. Provide the presentations (preferably during the breaks, latest the break prior to your presentation) or have your laptop ready.
    b. Do you agree on having it available at the ESA website? **Default: YES** (the final version can be provided another day)

2. **Attendees**:
    a. Do you agree to be included in the attendees list? **Default: YES**

Useful information

1. **Networking Coffee Break sponsored by CNES CTT and ESA TEC-ED**

2. **Networking Luncheon** at ESTEC main canteen

3. **Wireless access**:
    a. Login and password included at the back of your visitor badge. Valid throughout the workshop

        SSID: **esa-public** Authentication: Open
        Username: *d.merodiocodinachs*
        Password: *xxxxxx*

If your badge does NOT include this information, please report to the Registration Desk

Optional social dinner

Restaurant: Iets Anders in Bistro Bardot

Date: 16th March 2016

At 8pm

Address: Pickeplein 4, 2202 CK Noordwijk

Price: 43 EUR

The price includes a 3 course menu and drink arrangement.

Confirmation: Before lunch time (if not done yet)

ENJOY THE WORKSHOP !!!