

SEFUW: Space FPGA Users Workshop 3rd Edition



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David Dangla (CNES)



WELCOME TO ESTEC



European Space Research and Technology Centre (ESTEC)

<http://www.esa.int/SPECIALS/ESTEC/index.html>



Coffee breaks and
Cocktail reception during the Demo
Session are sponsored by



Communautés de Compétences Techniques



Exchange of highly valuable information and experience among FPGA users, researchers, CAD vendors and FPGA vendors

Precursor experiences and SEFUW editions

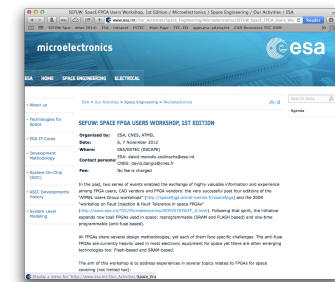
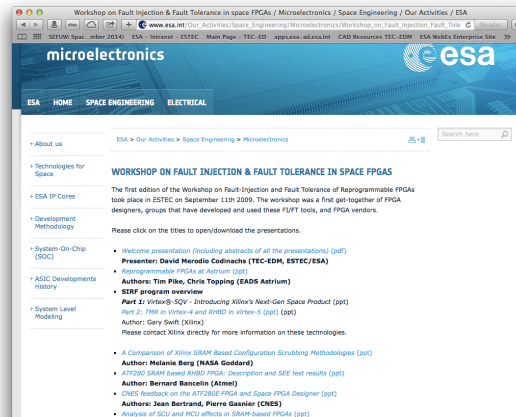


<http://spacefpga.atmel-nantes.fr/spacefpga/>

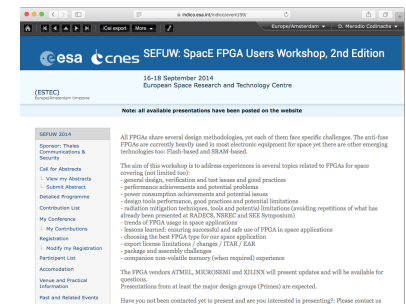
ATMEL Aerospace
FPGA working group:
Workshops and
website

Workshop on Fault
Injection & Fault
Tolerance in space
FPGAs (2009)

1st **SEFUW**, Oct 2012



2nd **SEFUW**, Sep 2014



http://www.esa.int/TEC/Microelectronics/SEM57KIWF_0.html

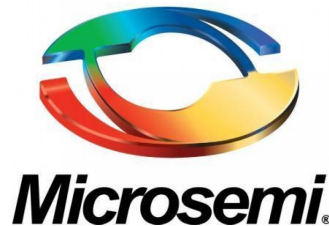
1. New FPGA vendors addressing space
2. Larger and higher performance FPGAs are becoming available
3. COTS FPGAs use is growing
4. FPGA domain usage expands:
 - a. High performance using FPGAs
 - b. Re-programmability (already addressed in previous SEFUW editions)

FPGA updates/ trends (I): FPGA vendors addressing Space



- ✓ Space FPGA vendors in SEFUW 2016 and also in previous SEFUW editions:

Atmel



XILINX
ALL PROGRAMMABLE™

- ✓ NEW FPGA vendors for Space in SEFUW 2016:

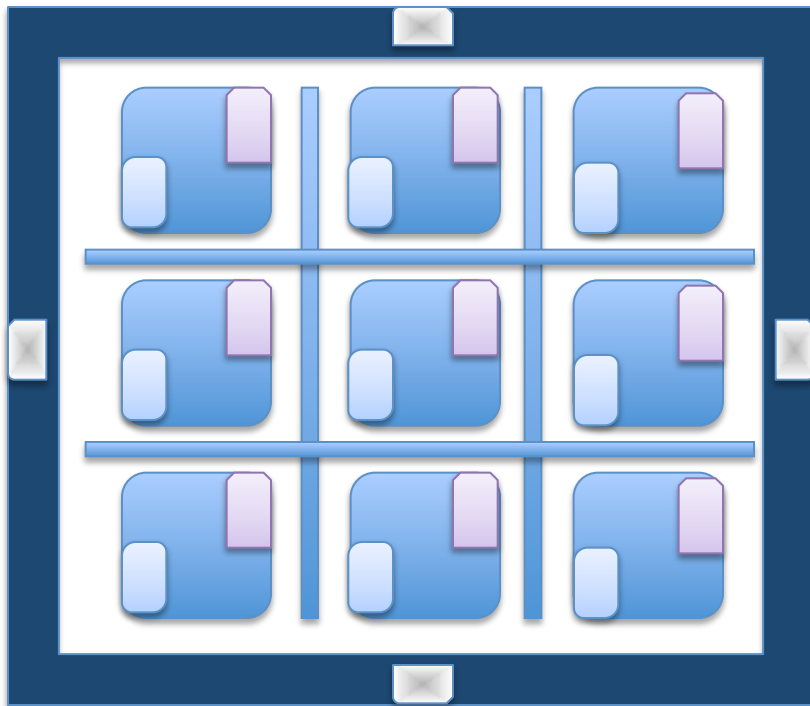
ALTERA
now part of Intel



FPGA updates/ trends (II): Larger and higher performance FPGAs (I)



1. FPGA Architectural features (general)



Logic fabric

Inter-connection

Internal memory

Clock generation (PLLs, DLLs,...)

Arithmetic (Multipliers, DSP, ...)

Flexible IOs

High speed serial links

Embedded processors

Other hard-macros (PCIe, ...)

FPGA updates/ trends (II): Larger and higher performance FPGAs (II)



1. FPGA “Eras” (based in their architecture):

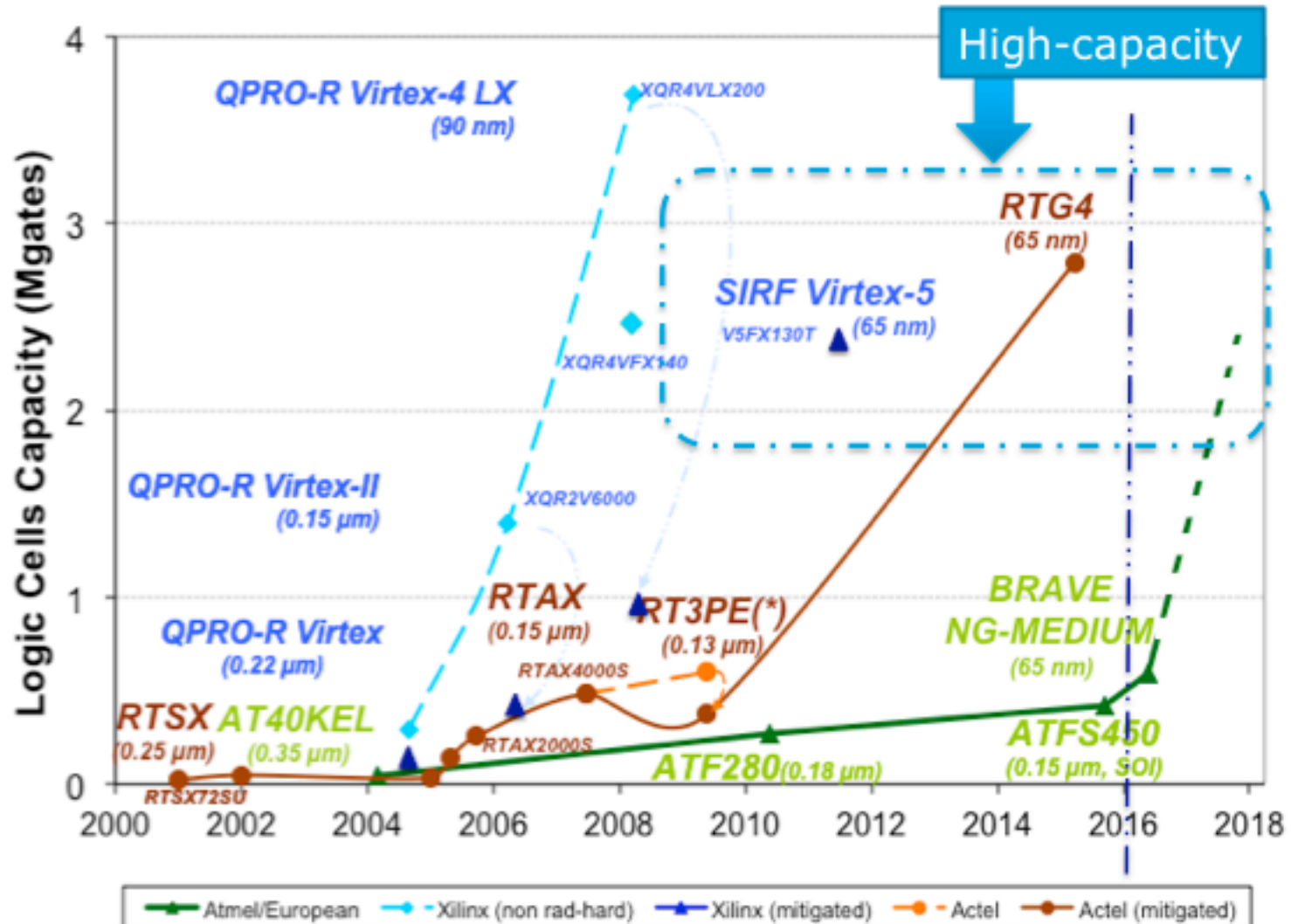
1. **First**: FPGA fabric (e.g. RTSX-SU)
2. **Second**: FPGA fabric and Internal Memory (e.g. RTAX-S, ATF280F)
3. **Third**: FPGA fabric, Internal Memory and specialized Hard-macros (DSP, etc). (e.g. Virtex-4/5, RTAX-DSP, RTG4, NG-MEDIUM)
4. **Fourth**: SoC FPGA (e.g. Zynq, Smartfusion2, Cyclone V SoC, Arria V SoC)

2. Radiation hardened FPGA and COTS FPGAs:

1. COTS FPGAs: entered the 4th Era some years ago
2. Radiation hardened FPGAs: “behind” the COTS timeline,
but better radiation performance

FPGA updates/ trends (II): Larger and higher performance FPGAs (II)

Note: RTG4, ATFS450 and BRAVE NG-MEDIUM dates are for Engineering Samples



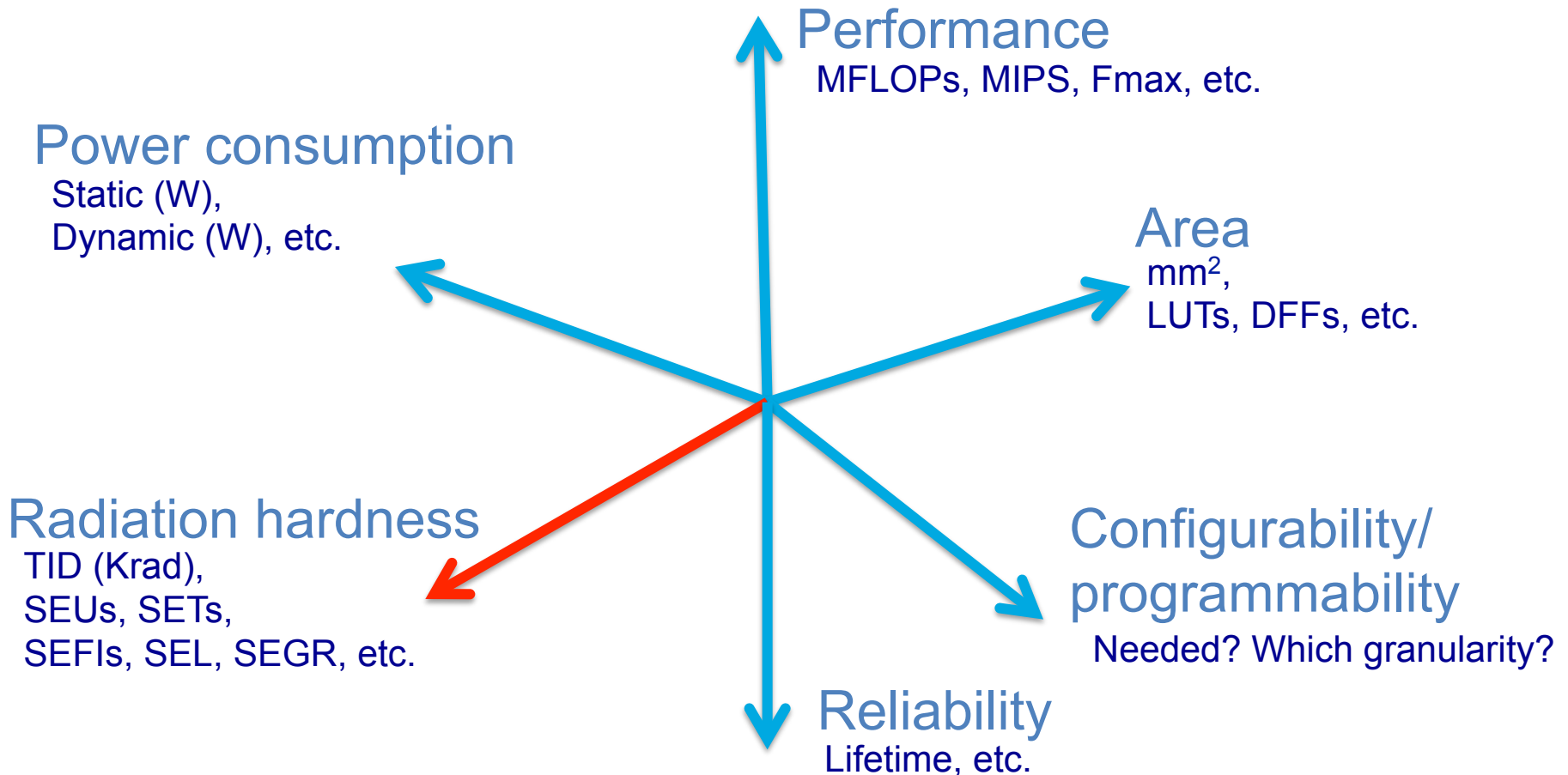
FPGA updates/ trends (III): COTS FPGAs (I)



1. During subsystems development:
COTS FPGAs are used for bread boarding (**BB**)
2. When moving to **EQM** and **FM** models, which FPGA is used?
The “nominal” choice is:
 - a. **Radiation hardened FPGA**: if the performance can be achieved
 - b. **ASIC**: if the performance cannot be achieved
3. Due to the **changing programmatic constraints** (shorted lifetime, better-faster-cheaper, etc.). Specially relevant for **Nanosatellites** and **Cubesats**:
 - a. **COTS FPGA** are proposed for EQM and FM

Understanding their radiation performance, mitigation techniques and guidelines on how to use them is paramount. The overall Quality (ECSS-Q-ST-60-13C) is paramount.

FPGA updates/ trends (III): COTS FPGAs (II)

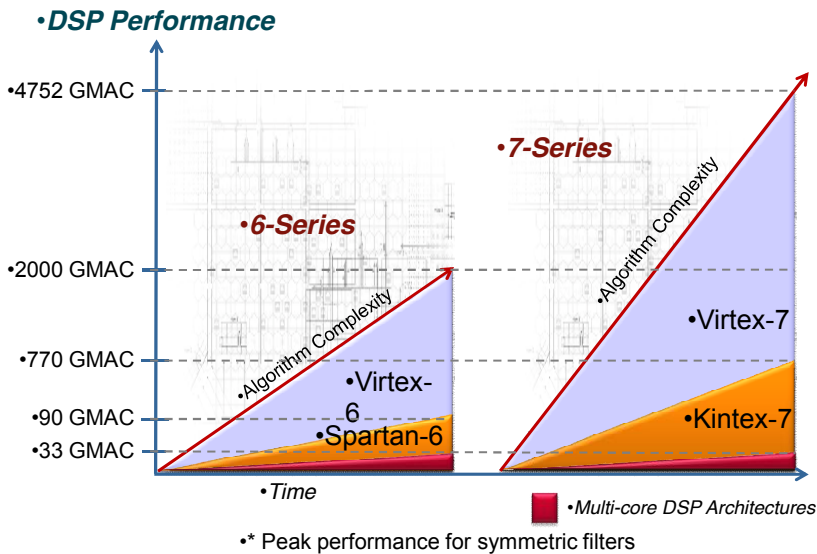


Also VERY important:

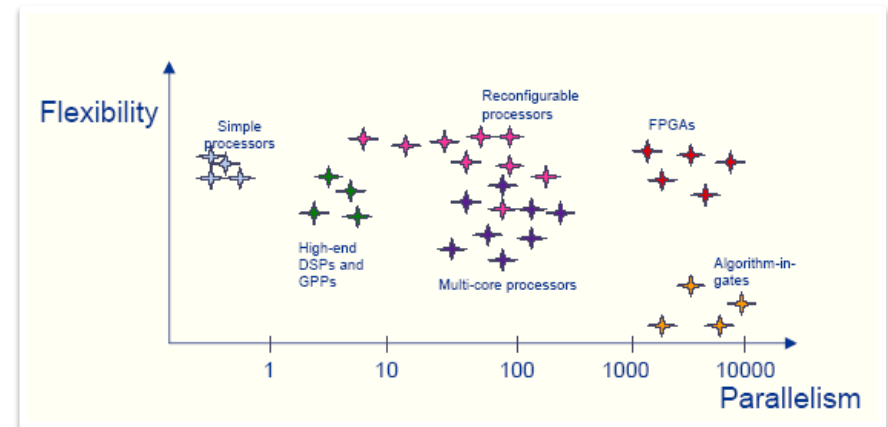
Quality, Packaging, Mounting,
ITAR/ EAR, Price ...

FPGA updates/ trends (IV): Domain usage expands

1. Re-configurability, High Performance



Source: [Xilinx](#)



Source: [BDTi](#), “Benchmarking Multithreaded, Multicore and Reconfigurable Processors”, 2006

Agenda (I)



<https://indico.esa.int/indico/event/130/timetable/#all.detailed>

The agenda has been distributed among the participants

SEFUW: Space FPGA Users Workshop, 3rd Edition

15-17 March 2016
European Space Research and Technology Centre

(ESTEC)
Europe/Amsterdam timezone

SEFUW 2016

Sponsors: CNES CCT and ESA's Data System Division

Call for Abstracts

- View my Abstracts
- Submit Abstract

Detailed Programme

Contribution List

Registration

- Modify my Registration

Accommodation

Venue and Practical Information

Past and Related Events

SEFUW Dinner

For information please write to
sefuw@esa.int

Tue 15/03 Wed 16/03 Thu 17/03 All days

Print PDF Full screen Detailed view Filter

Session legend

Demo Session and C... Design Experiences FPGA Vendors FPGAs: High Perform... see more...

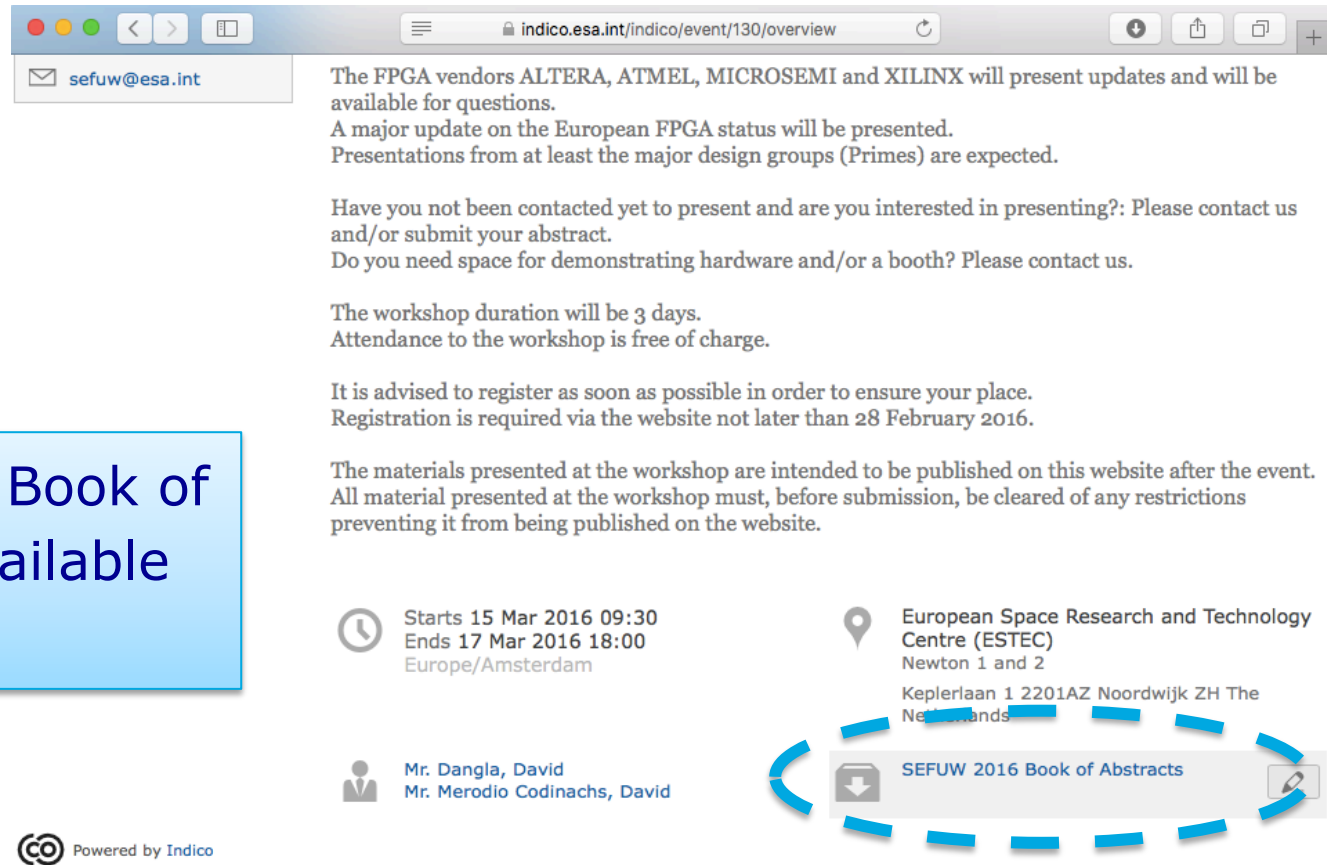
Tue 15/3

09:00

Registration and Early Morning Networking Break sponsored by CNES CCT and ESA's Data System Division	
Newton 1 and 2, European Space Research and Technology Centre (ESTEC)	09:30 - 10:00
10:00 Welcome	Mr. David DANGLA et al.
Newton 1 and 2, European Space Research and Technology Centre (ESTEC)	10:00 - 10:25
Implementation of Space-Industry IP : A Comparison of Space-Grade FPGAs Dr. Rajan BEDI	
Newton 1 and 2, European Space Research and Technology Centre (ESTEC)	10:25 - 10:55
11:00 FPGA development flow for future large space FPGA	Mr. Florent MANNI
Newton 1 and 2, European Space Research and Technology Centre (ESTEC)	10:55 - 11:20
Prototyping a SOC on RTAX4000D for Solar Orbiter's Low Frequency Receiver. Mr. Alexis JEANDET	
Newton 1 and 2, European Space Research and Technology Centre (ESTEC)	11:20 - 11:45
LEON3/GRLIB for Space-Grade Programmable Devices Update and Roadmap Mr. Jan ANDERSSON	
Newton 1 and 2, European Space Research and Technology Centre (ESTEC)	11:45 - 12:10

<https://indico.esa.int/indico/event/130/timetable/#all.detailed>

SEFUW 2016 Book of Abstracts: available online



The FPGA vendors ALTERA, ATMEL, MICROSEMI and XILINX will present updates and will be available for questions.
A major update on the European FPGA status will be presented.
Presentations from at least the major design groups (Primes) are expected.

Have you not been contacted yet to present and are you interested in presenting?: Please contact us and/or submit your abstract.
Do you need space for demonstrating hardware and/or a booth? Please contact us.

The workshop duration will be 3 days.
Attendance to the workshop is free of charge.

It is advised to register as soon as possible in order to ensure your place.
Registration is required via the website not later than 28 February 2016.

The materials presented at the workshop are intended to be published on this website after the event.
All material presented at the workshop must, before submission, be cleared of any restrictions preventing it from being published on the website.

Starts 15 Mar 2016 09:30
Ends 17 Mar 2016 18:00
Europe/Amsterdam

Mr. Dangla, David
Mr. Merodio Codinachs, David

European Space Research and Technology Centre (ESTEC)
Newton 1 and 2
Keplerlaan 1 2201AZ Noordwijk ZH The Netherlands

SEFUW 2016 Book of Abstracts

Powered by Indico

1. Sessions:

- a. FPGA Vendors
- b. Design experiences
- c. Industry experiences
- d. FPGAs: High Performance
- e. Reconfigurability
- f. Radiation
- g. Fault Tolerance Methodologies



2. Demo session



1. Presenters:

- a. Provide the presentations (preferably during the breaks, **latest** the break prior to your presentation) or have your laptop ready.
- b. Do you agree on having it available at the ESA website? **Default: YES** (the final version can be provided another day)

2. Attendees:

- a. Do you agree to be included in the attendees list?
Default: YES

1. Networking Coffee Break sponsored by CNES CTT and ESA TEC-ED

2. Networking Luncheon at ESTEC main canteen

3. Wireless access:

- a. Login and password included at the back of your visitor badge. Valid throughout the workshop

SSID: esa-public Authentication: Open

Username: *d.merodiocodinachs*

Password: *xxxxxx*

If your badge does NOT include this information, please report to the Registration Desk

Restaurant: Iets Anders in Bistro Bardot

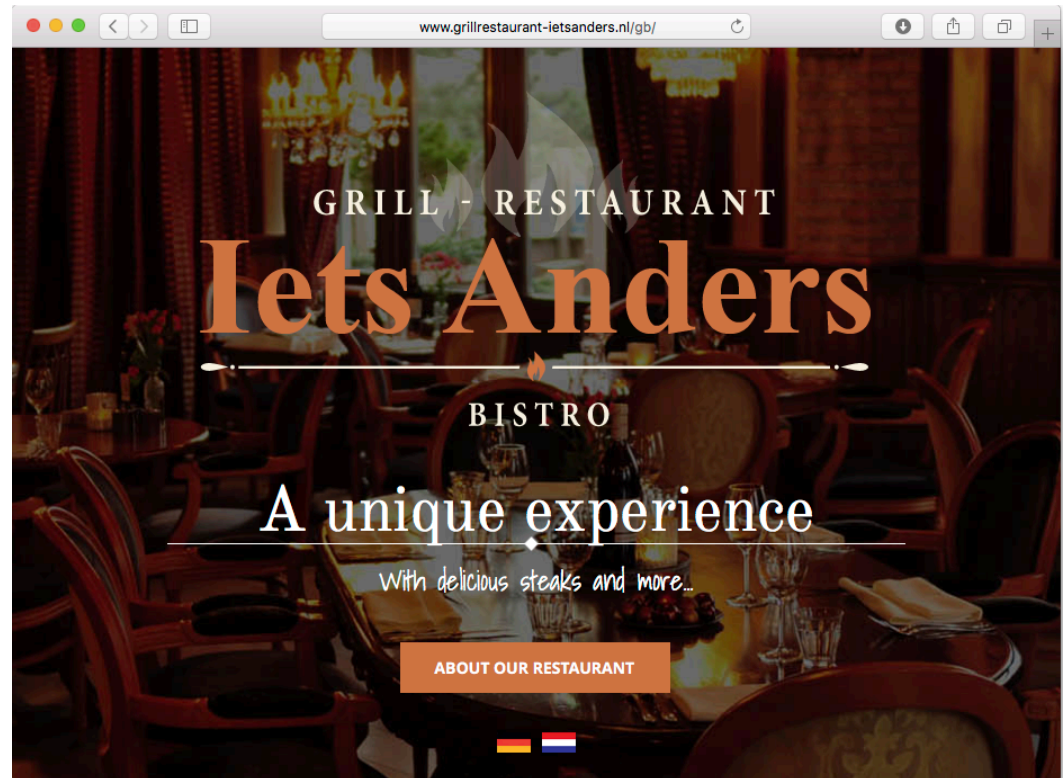
Date: 16th March 2016

At 8pm

Address: Pickeplein 4,
2202 CK Noordwijk

Price: 43 EUR

The price includes a 3 course menu and drink arrangement.



Confirmation: Before lunch time (if not done yet)

ENJOY THE WORKSHOP !!!