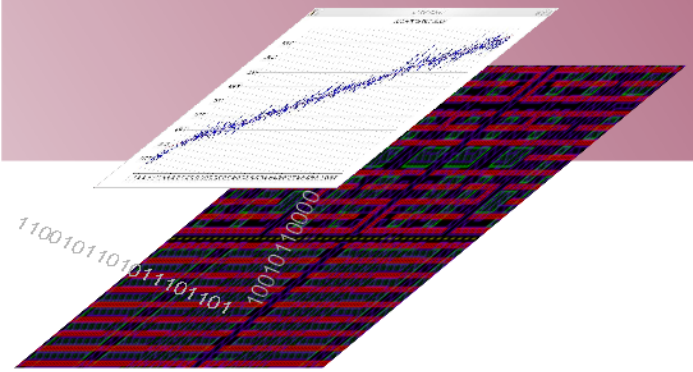


SEFUW workshop

Feb 17th 2016

NanoXplore overview

- French fabless company with two activities
  - FPGA core IP
  - High reliable FPGA devices
- Lead by FPGA industry experts with more than 25 years track records
  - Has developed FPGA core from 1µm down to 28nm process
  - Already developed 750k LUTs FPGA in 65nm and 500k LUTs FPGA core in 28nm
- Technology has been used in emulation systems for 20 years

BRAVE project overview

- ESA / CNES project to develop a new generation of rad hard FPGAs
- Well defined consortium
  - ESA and CNES
  - NanoXplore as project leader
  - STM as foundry and IP provider
  - Airbus DS and TAS as alpha users
- Based on NanoXplore ultra dense patented FPGA architecture and STM 65nm “space” process
- NXT 35 “NG-MEDIUM” is our first rad-hard FPGA
- Fully ITAR free

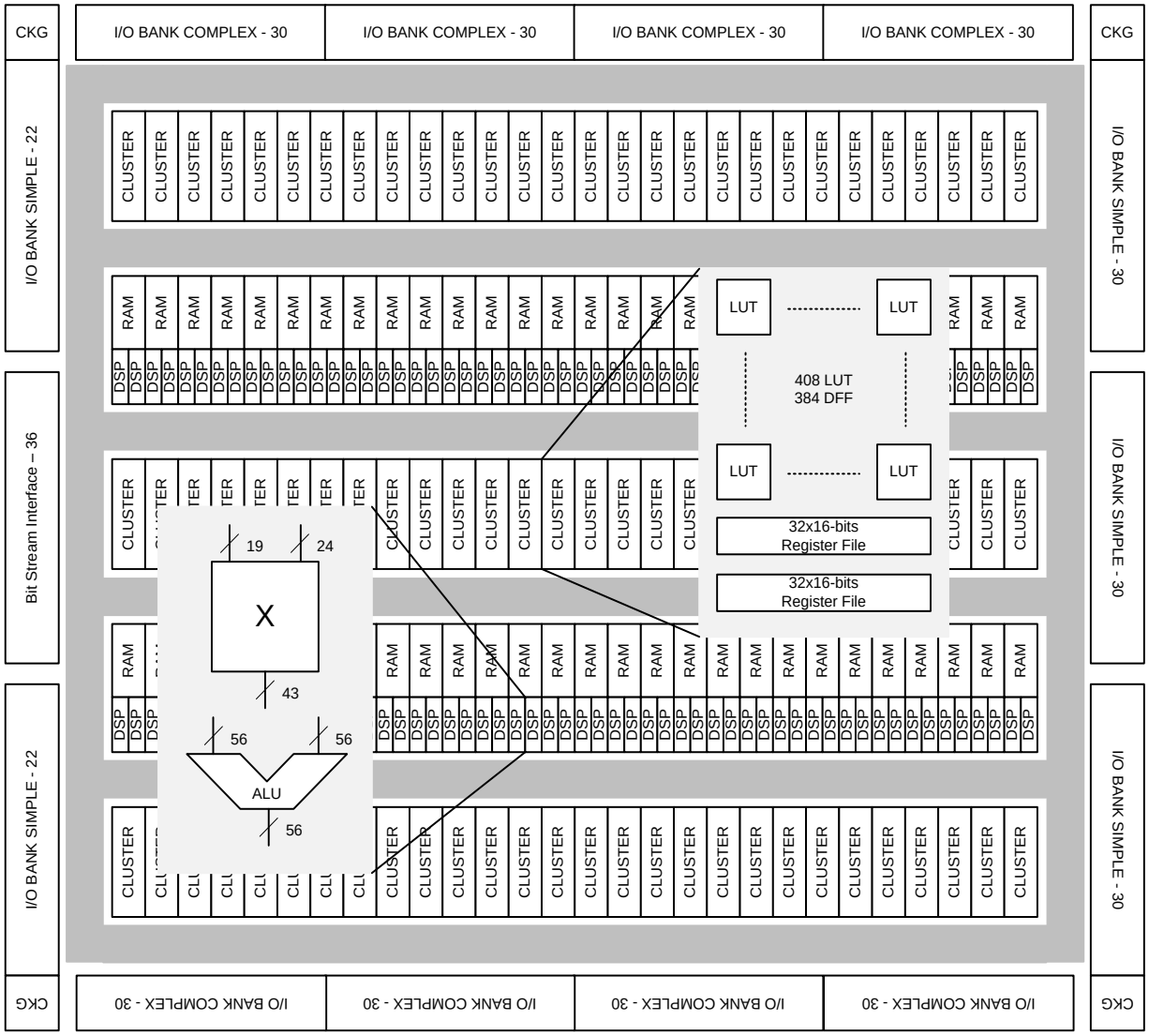
NG-MEDIUM Overview

- SRAM based FPGA
  - Four inputs LUT
  - Embedded RAM
  - Embedded DSP
  - Multiple clock domains
  - Programmable IO banks
- Radiation hardened by design
  - Specifically designed for space applications
  - No software level mitigation
  - SEE immune for LEO/GEO environment
- Meet QML-V qualification flow for two packages
  - CQFP-352
  - LGA-625

NG-MEDIUM Summary

Device	NG-MEDIUM
Capacity	
Equivalent System Gates	4 400 000
ASIC Gates	550 000
Modules	
Register	32 256
LUT-4	34 272
Carry	8 064
Embedded RAM	
Core RAM Blocks (48K-bits)	56
Core RAM Bits (K = 1024)	2688 K
Core Register File (64 x 16-bits)	168
Core Register File Bits	168 K
Embedded DSP	112
Clocks	32
Embedded Serial Link	
SpaceWire 400Mbps	1
I/Os	
I/O Banks	13
User I/Os	
LGA-625	390
MQFP-352	208
I/O PHY	
DDR	16
SpaceWire	16

NG-MEDIUM Architecture



NG-FPGA-MEDIUM Characteristics

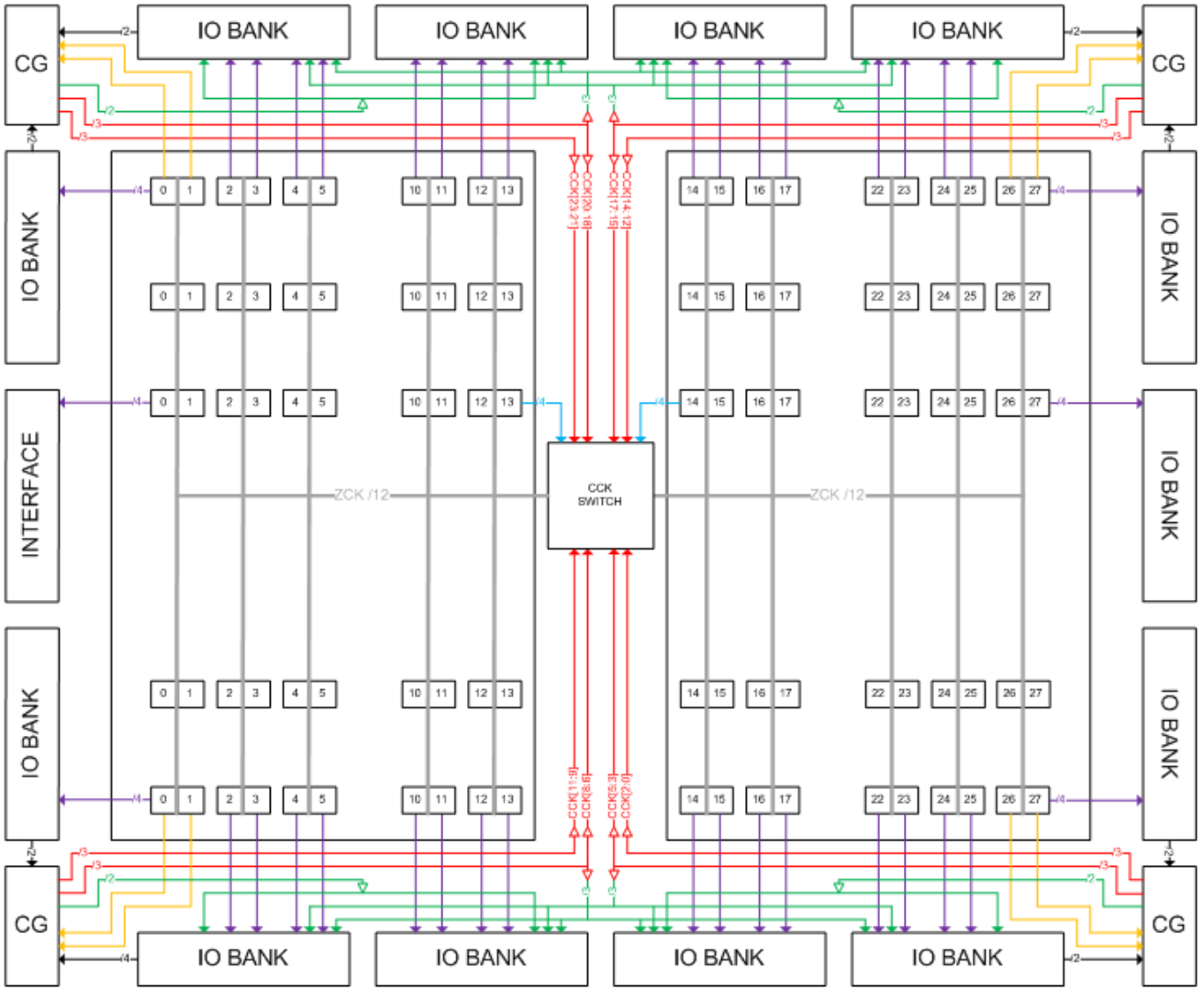
- Power supply
  - Core: 1,2V ±10%
  - IOS: 1.5V ±10% or 1.8V ±10% or 2.5V ±10% or 3.3V ±10%
- Performance
  - 250MHz Logic
  - 333MHz DSP
  - 800Mbps I/O
- Temperature
  - -55ºC to +125ºC
- ESD
  - HBM > 2000V for all IOB, Control IO and power supplies

Embedded DSP

- Implements arithmetic functions
  - Multiply
  - Multiply-add/subtract
  - Multiply-accumulate
- Single / Dual DSP mode
  - 18 x 18 multiplication
  - 24 x 24 multiplication
- Possibility to cascade multiple DSP to implement high performance algorithms

Clock distribution

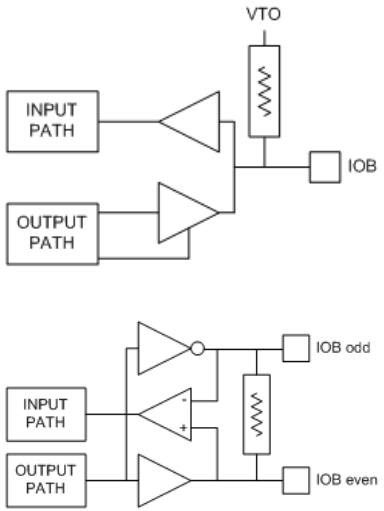
- Four clock generators
  - PLL
  - Post scaler
  - Waveform generator
  - PVT Oscillator
- Hierarchical clock distribution
  - Core clocks
  - Zone clocks
  - I/O bank clocks



IO system

- Programmable I/O buffer
  - Single ended
  - Differential
  - Resistive termination

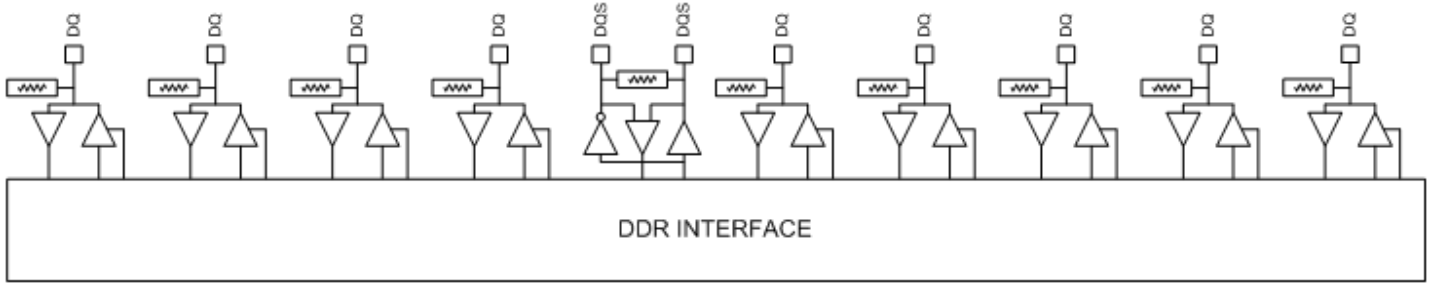
Standard	Type	Supply	Drive	Speed	Special considerations	Notes
LVCMOS 3.3V	SE	3.3 V	2–6 mA	200Mb/s		
LVCMOS 2.5V	SE	2.5 V	2–5 mA	200Mb/s		
LVCMOS 1.8V	SE	1.8 V	3.5 mA	600Mb/s		
LVCMOS 1.5V	SE	1.5 V	3 mA	600Mb/s		
PCI/PCI-X	SE	3.3 V	30 mA	200Mb/s		
SSTL 2.5V – I/II	SE	2.5 V	15/22 mA	600Mb/s		
SSTL 3.3V – I/II	SE	3.3 V	20/30 mA	600Mb/s		
HSTL 2.5V – I/II	SE	2.5 V	20/30 mA	600Mb/s		
HSTL 1.8V – I/II	SE	1.8 V	13/16 mA	800Mb/s	Controlled Source Impedance	DDR2
HSTL 1.5V – I/II	SE	1.5 V	11/16 mA	800Mb/s	Controlled Source Impedance	DDR3
GTL/GTL+	SE	3.3 V	24 mA	200Mb/s	Sink only / External load	
LVPECL 2.5V	DIF	2.5 V	18 mA	800Mb/s	Source only / External load	
LVDS 2.5V	DIF	2.5 V	18 mA	800Mb/s		



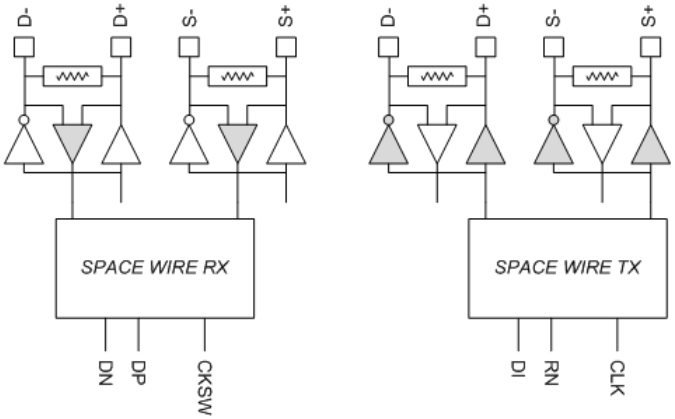
- Multiple Banks
  - One bank has same supply voltage
  - 8 x 30 I/Os complex banks
  - 3 x 30 I/Os simple banks
  - 2 x 22 I/Os simple banks

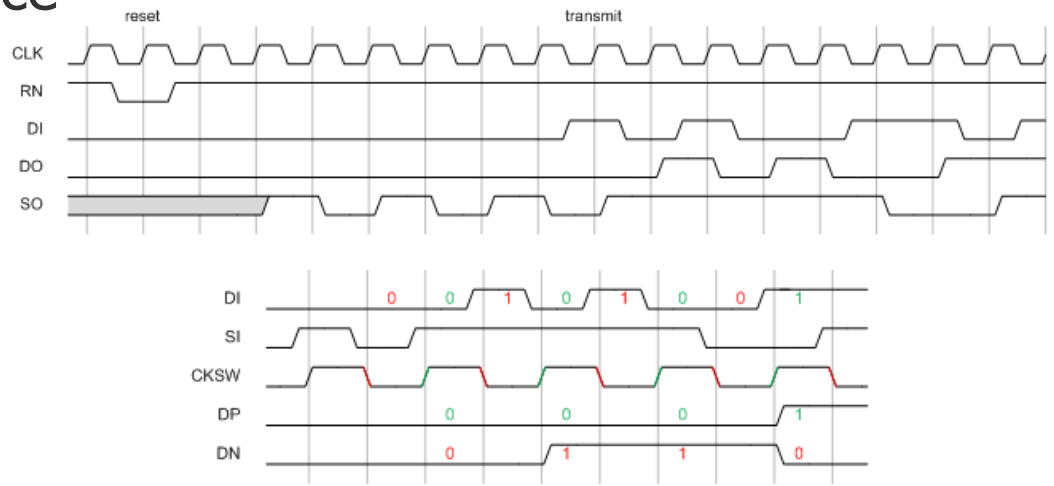
Complex bank features

- DDR2 / DDR3 800Mb/s physical interface



- SpaceWire physical interface





Bit stream management

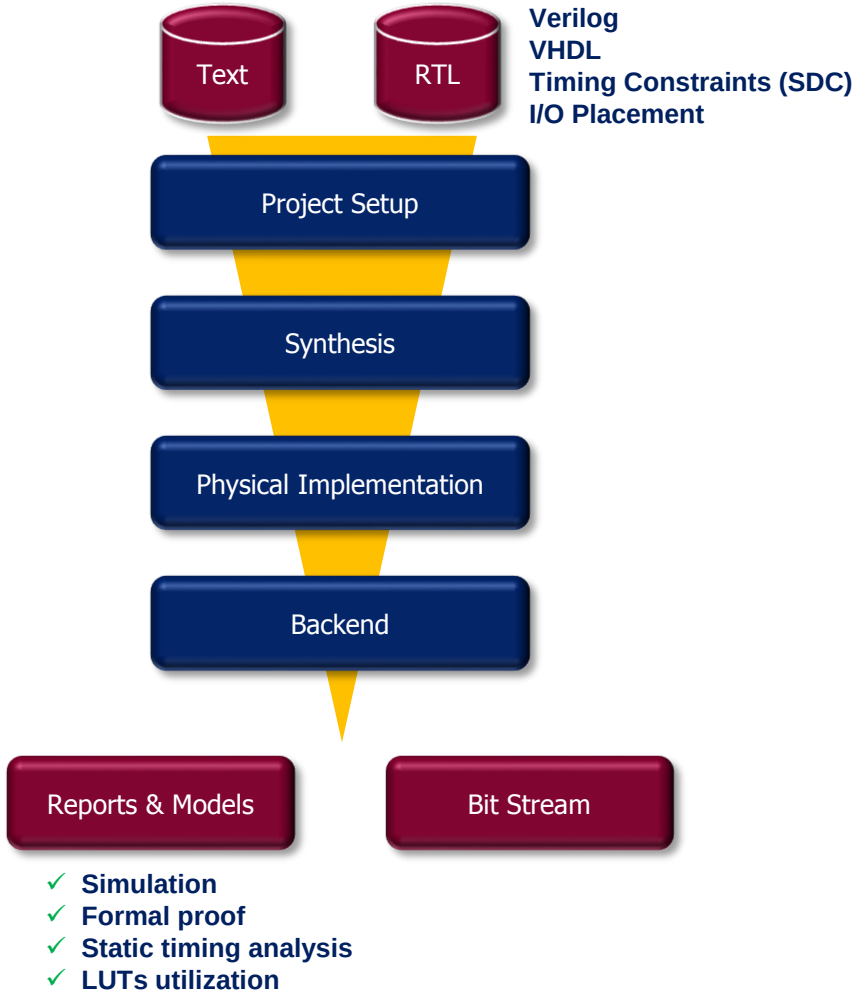
- Download interfaces:
  - JTAG
  - SpaceWire (up to 400Mbps).
  - Slave // 8-bits
  - Slave // 16-bits
  - Master / Slave Dump (compatible AT69170E)
  - Master SPI
- Advanced bit stream protection mechanisms
  - Frame Integrity Check (FIC)
  - Configuration Memory Integrity Check (CMIC)
- Seamless external SPI memory integration
  - Auto powering by FPGA
  - Built in SEL monitoring and mitigation

Hardening overview

- SEL immune
  - ST 65nm technology with PDK space design rules provides immunity at 60MeV/mg cm2, 125ºC, 1.32V
  - SEL TCAD simulations performed on IO buffers
- SEU / SET immune for LEO / GEO applications
  - Cell level hardening by design:
    - Implement a certain level redundancy
    - Optimize layout to reduce charge collection on critical nodes
    - Validate susceptibility with cross section simulation tools
  - Functional level hardening:
    - Use error detection and correction functions
    - Implement filters on critical signals (i.e. clock, reset)
  - System level:
    - Check bit stream integrity with signatures (FIC)
    - Check configuration integrity at run time (CMIC)

Programming software: NanoXmap overview

- NanoXplore rad-hard FPGA offering is supported by its own software NanoXmap
- Fully integrated flow from synthesis down to bit stream generation and reports (timing, LUTs utilization etc)
- NanoXmap is already released and meet the initial expectations
  - Utilization rate >80%
  - Best compilation time of the market
- Support Verilog IEEE 1364-1995/2001 and VHDL IEEE 1076 – 1993 / 2008



NG-MEDIUM roadmap

- NanoXmap: Q2 2016
- Evaluation kit: Q4 2016
- Samples: Q4 2016
- QML-V eq flow: Q4 2017
- QML-Q eq flow: Q4 2017

Conclusion

- NG-MEDIUM is the first rad-hard FPGA of a well identified roadmap
  - NG-MEDIUM in 2016
  - NG-LARGE in 2017
  - NG-ULTRA in 2018
- NG-MEDIUM has validated NanoXplore design methodology and software tools for all future high performance rad-hard FPGA

- For more information feel free to contact us!
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www.nanoxplore.com