Heavy-Ion Micro Beam Study of Flash-Based FPGA Microcontroller Implementation

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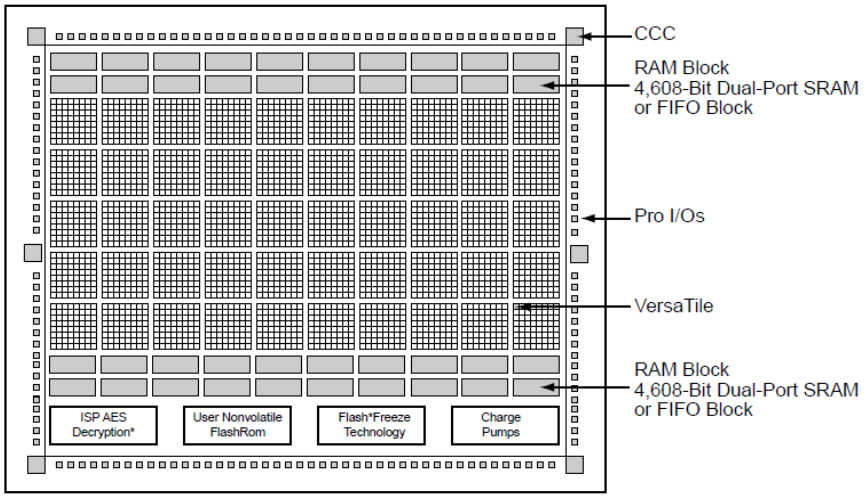
Outline

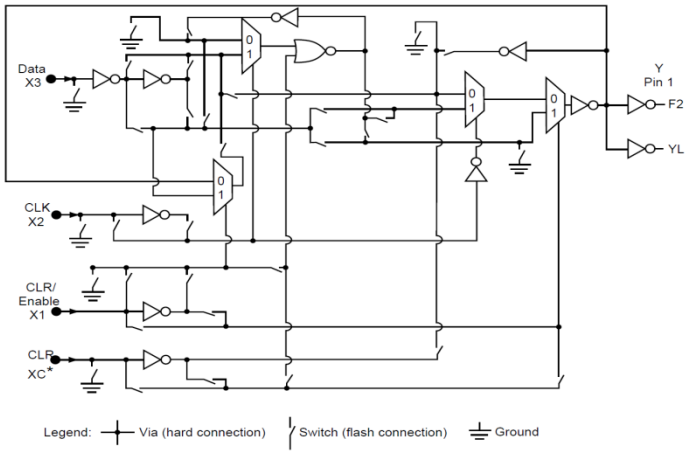
- Background
  - Microsemi ProASIC3L
  - Background - ARM® Cortex® M0+ Implementation
  - Heavy-ion Micro Beam (GSI)
- Test Setup
  - Control Logic
  - Physical Calibration
- Results
  - Results Classification (SDC, DUE,…)
  - Sensitivity Maps; SEUs vs SETs
  - Simulation Based Analysis
- Conclusions and Future Work

Background

MicroSemi ProASIC3L

	A3PE3000L
Core Voltage (V)	1.2 .. 1.5
Technology	130nm, 7ML
VeraTiles	75 264
4608 bit BRAMS	112
CCC (including PLL)	6
VersaNet Globals	18





VersaTile

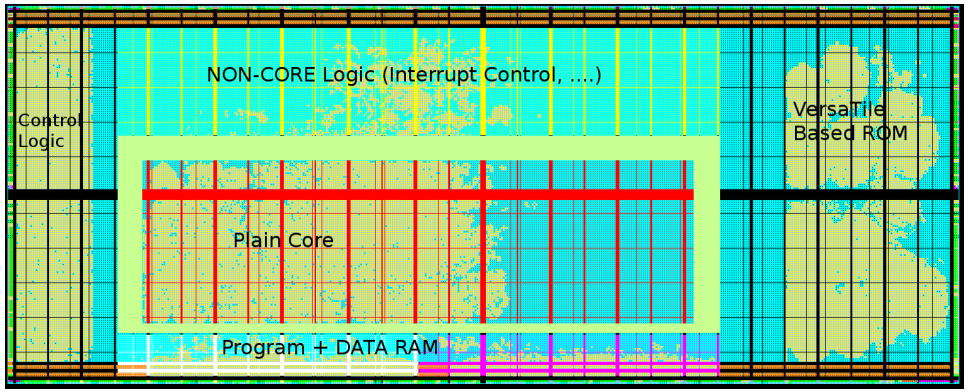
One VersaTile can implement:

- Any 3 input combinatorial function
- A DFF or latch with options for preset, clear, enable
- Configuration is controlled by floating gate switch

ARM® Cortex® M0+ Micro Processor

- 2-stage pipeline
- 10 MHz operation – to facilitate timing closure
- Running modified Dhrystone (customized to add end-of-test checks)
- 2 design versions : Protected and unprotected
  - Plain version – regular Libero synthesis flow
  - ASTMR (Automatic Sequential TMR)
    - 3x replication of FFs
    - SFSMC (Safe Finite State Machine Coding)

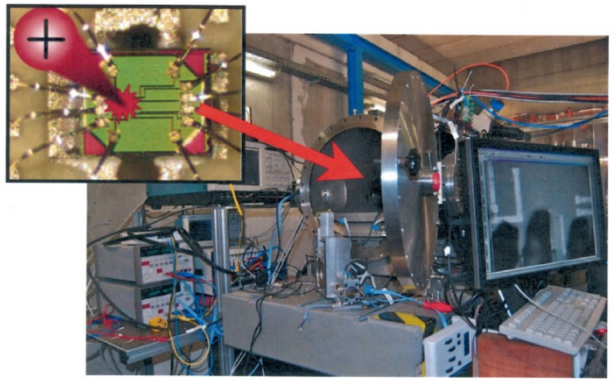
Core	Flip-Flops	Combo VTs	Total Cells
Plain	10 735 (90%)	1 231 (10%)	11 966
ASMTR	12 723 (78%)	3 495 (22%)	16 227



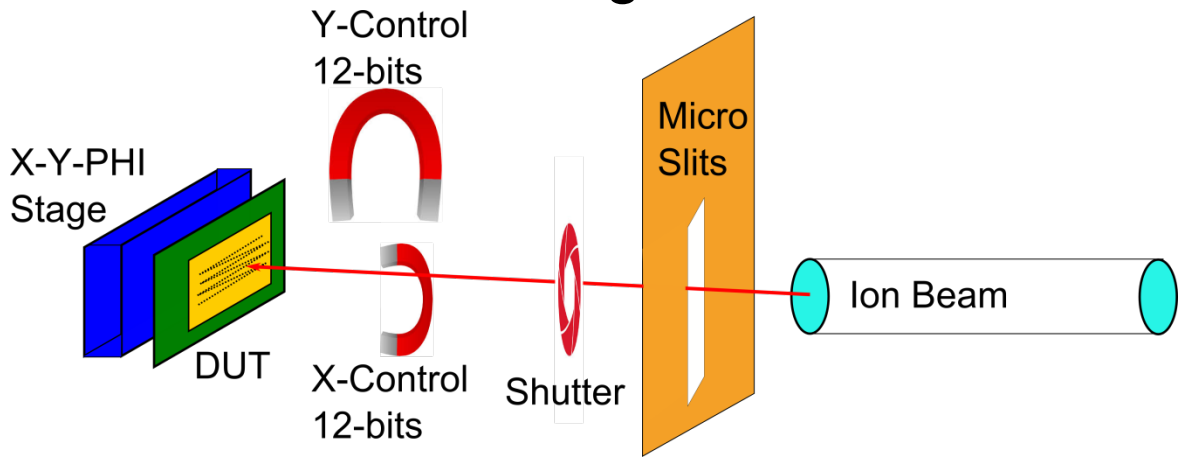
GSI Heavy Ion Micro-Beam

GSI Helmholtzzentrum für Schwerionenforschung GmbH

- Located in Darmstadt (near Frankfurt)
- Individual ions launched at specific x-y positions
- Beam is scanned over a region
  - 624µm x 503 µm – in this experiment
- Multiple scans to cover processor
- 500 nm spatial resolution of ion
- Ions accelerated up to 11.4 MeV/µm
  - Au – 4.8MeV/µm. LET=94 MeV•cm^2/mg)
- 1 million individual ions fired on each design

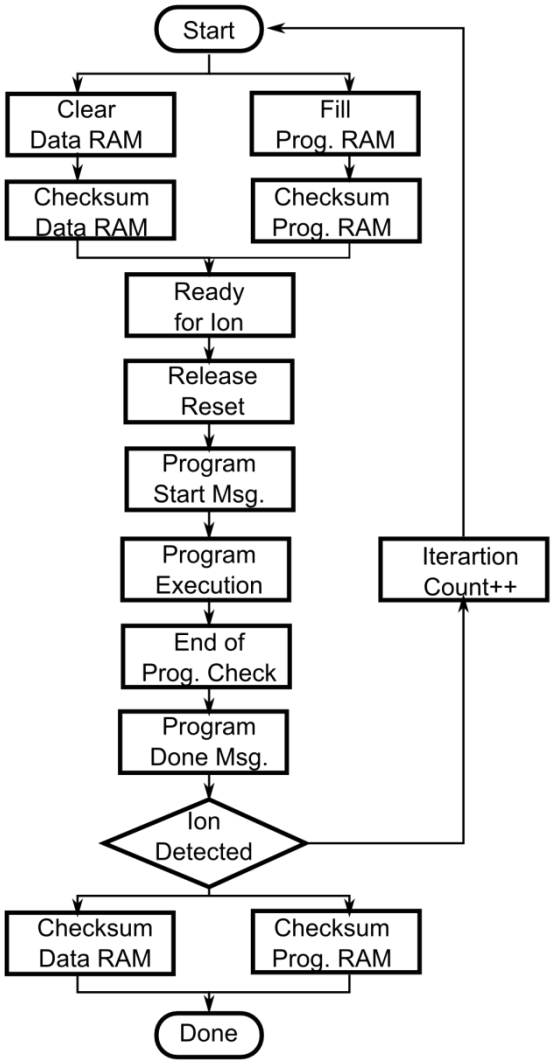


Opened
A3P3000L



Test Setup

Test Sequence



- **Several times a second a single ion is fired**
- Prior to firing the ion:
  - Processor and memory are initialized
  - Checksum of memories (CRC of good data)
  - Program starts running
- Program sends a start message
- **DUT Signal to GSI that – ready for ion**
- Program runs (potentially many times)
- **After an ion is detected (i.e. signaled by GSI)**
  - Wait for program to complete
  - Checksum of memories (CRC final data)
  - Report a “DONE” message
- At any time: If any interrupt (IRQ, NMI, …) occurs, recorded with time-stamp

Physical Calibration

- How do we know the exact location of the ion on the die?

- Two phase process:

Phase 1 - Calibration

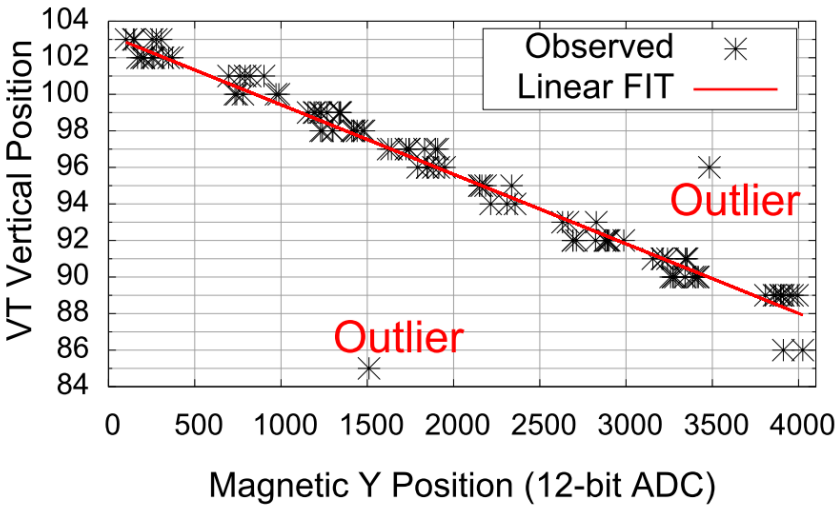
1. Program the FPGA with a “calibration load”
2. Fire ions on the “calibration load” and record logical position *and* magnetic co-ordinates.
3. Use these data points to get the mapping from magnetic co-ordinates to VT co-ordinates.

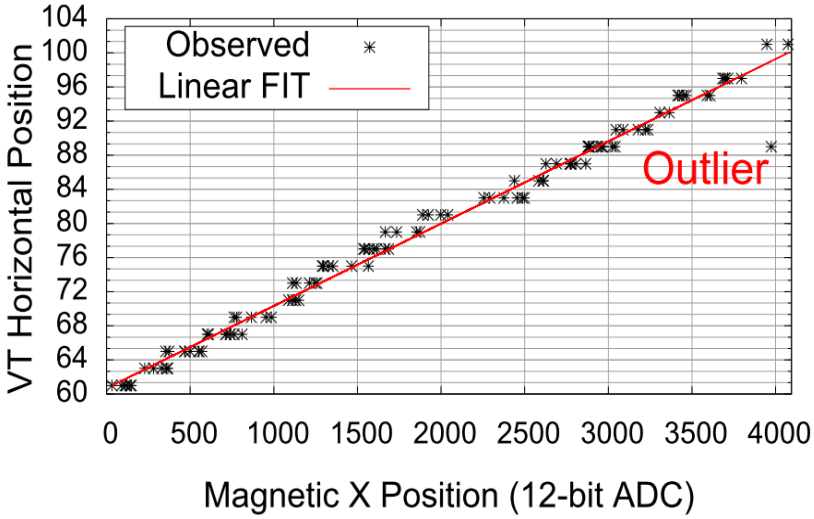
Phase 2 - CPU Testing

1. Fire ions at the CPU
2. Record magnetic co-ordinates (from GSI)
3. Convert back to physical location using mapping

Physical Calibration (2)

- Calibration mode → FPGA configured as array of FFs
- After ion is fired, FFs shifted out → get physical location





- Good alignment between magnetic and logical co-ordinates
- Small number of outliers (during calibration, these are filtered out)

Results

Classification of Failing Results

Build on the classification scheme from [1]

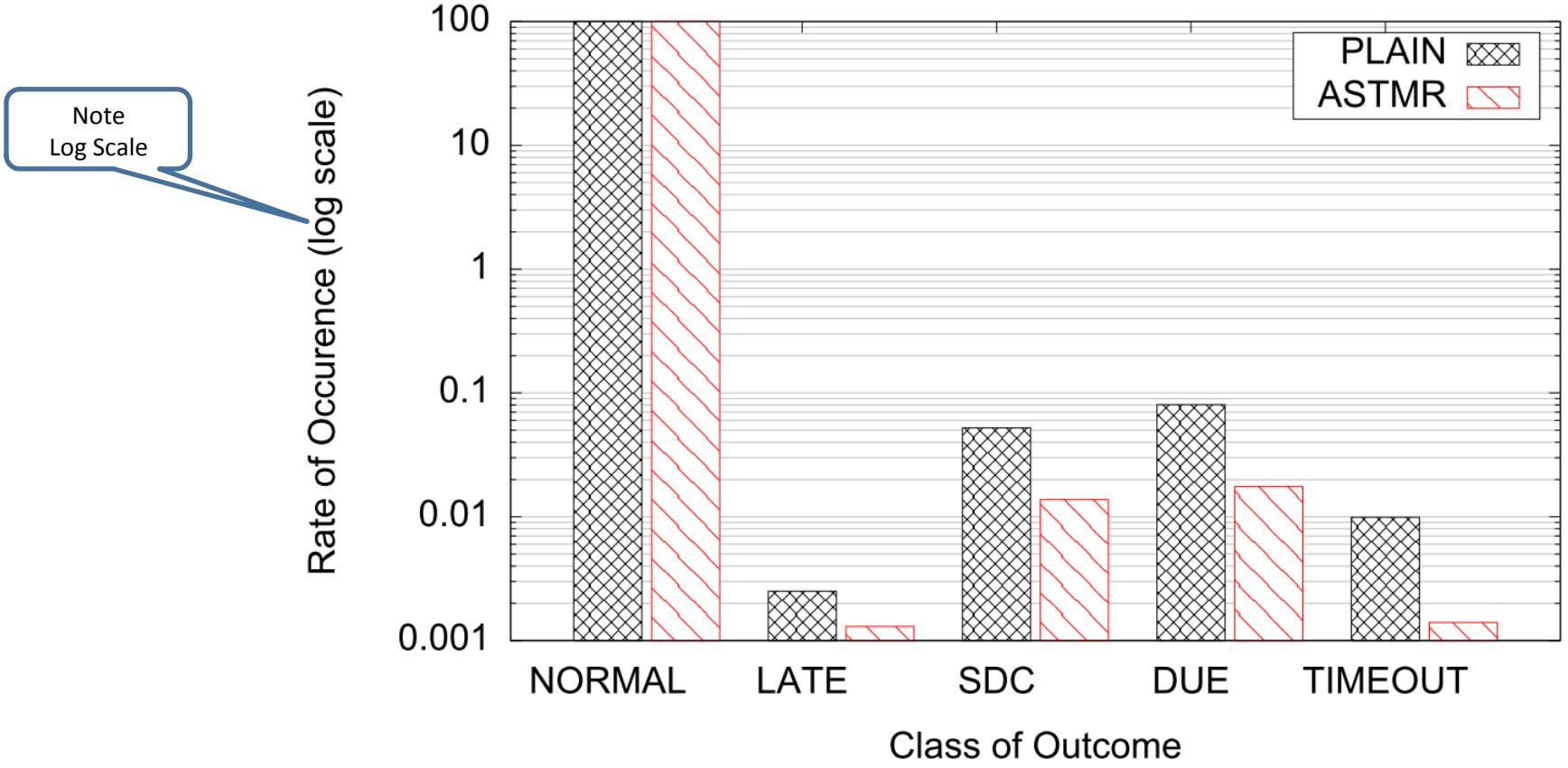
- SDC = **S**ilent **D**ata **C**orruption
- DUE = **D**etected **U**ncorrected **E**rror
- Timeout = Program does not complete

Category*	Memory Checksum	Start Message	Stop Message	SW Checks	HW Interrupts
Normal	Match	On-time	On-time	Pass	None
Late	Match	On-time	Late	Pass	None
SDC	No	On-time	On-time	Pass	None
SDC	-	On-time	On-time	Fail	None
DUE	--	On-time	--	--	Fire
Timeout	--	On-time	Missing	--	None

[1] C.T. Weaver. Reducing the soft-error rate of a high-performance microprocessor. Micro, vol. 24, no. 6, pages 30–37, 2004.

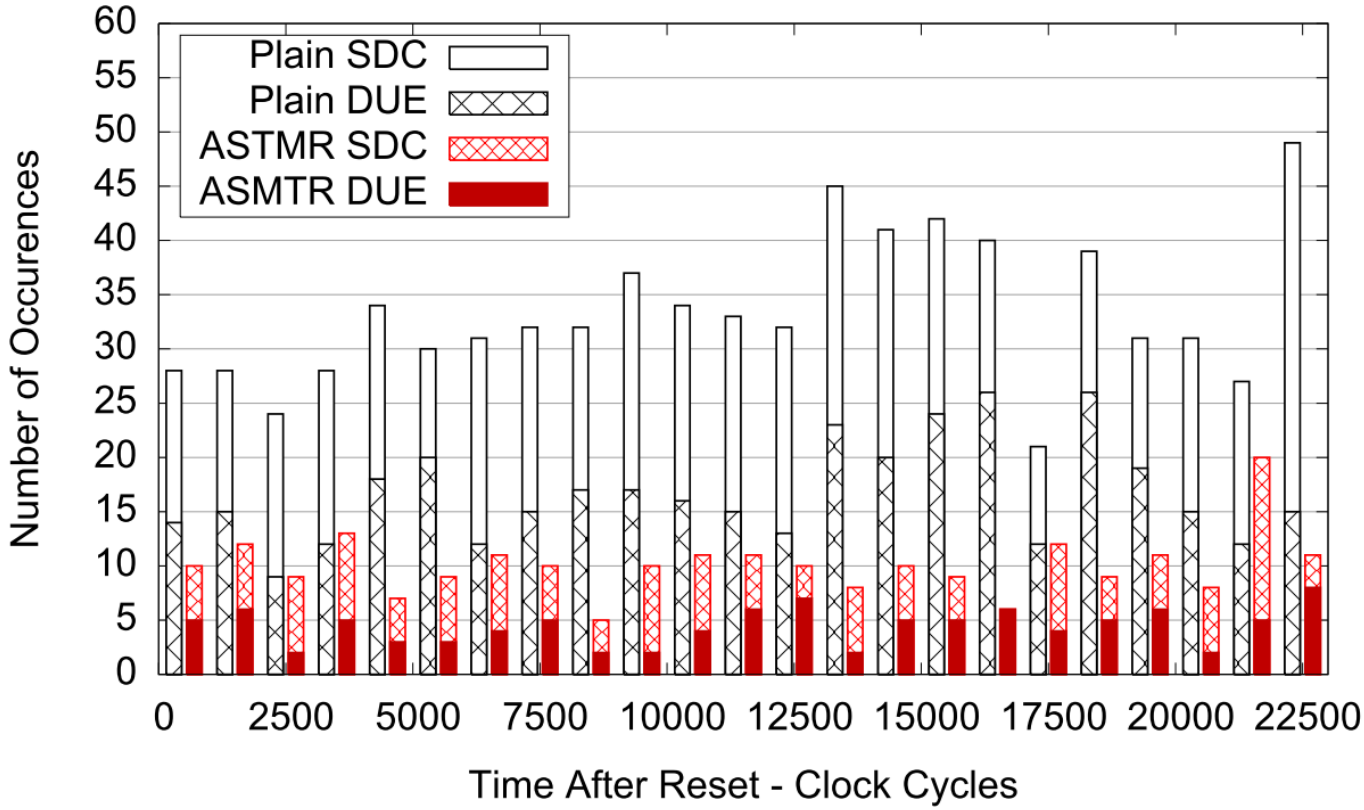
* - some very rare exception cases (e.g. missing start-message) have been excluded to simplify the presentation.

Aggregate Results Classification



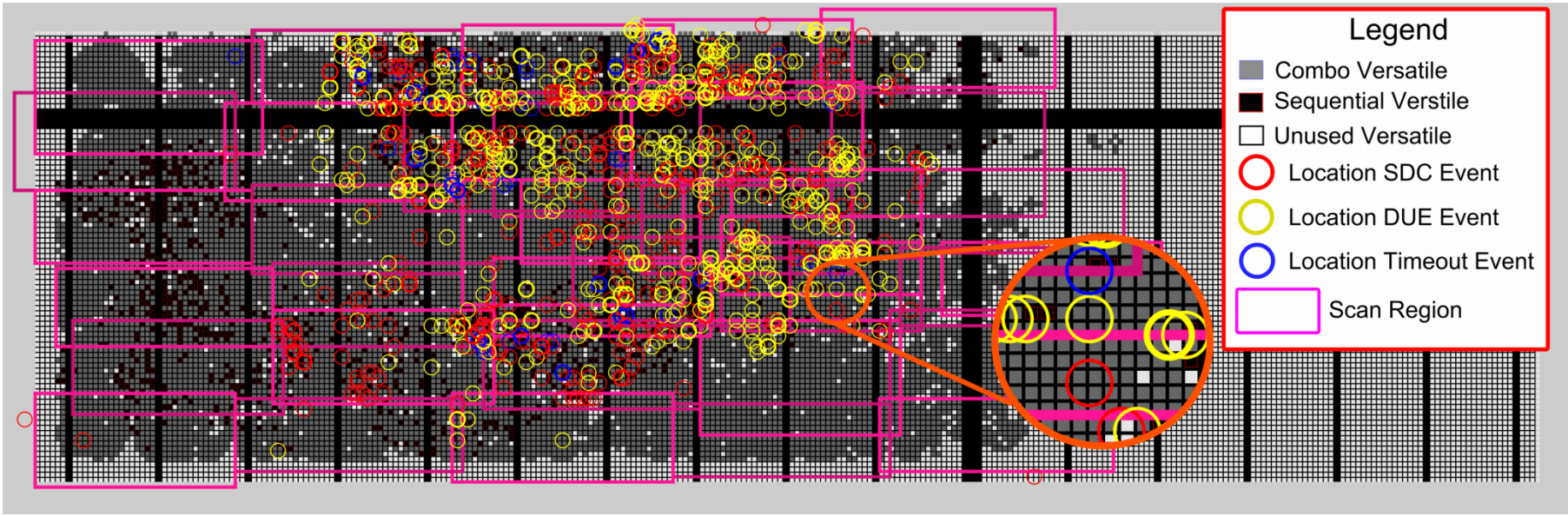
- Vast majority of ions have no impact (Normal)
- ASTMR : 5x reduction of DUE ; 2.5x reduction of SDC
- ASMR significantly reduces rate of time-outs

Temporal Analysis (DUE)



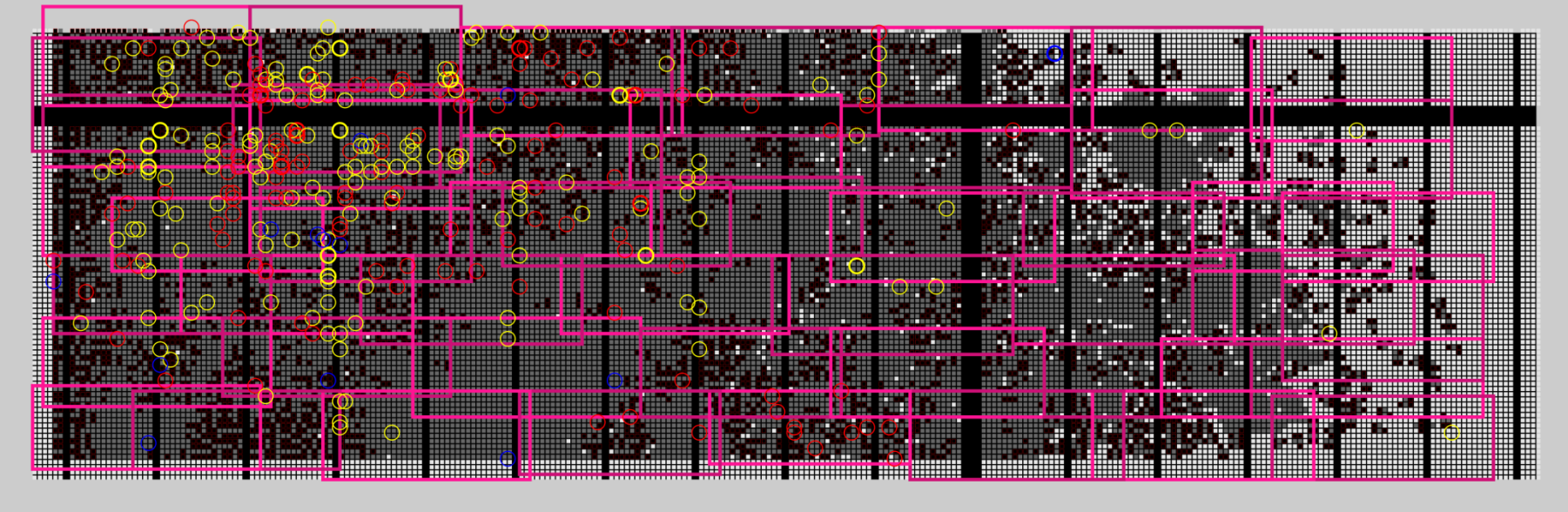
- Time of each ion strike is known (CPU clock cycle)
- Study of outcome versus time of ion strike (above)
- Program sensitivity is quite constant
  - Small peak in SDC at end of test (no masking)

Sensitivity Maps (Plain)



- Exact location **and** time **and** effect of each ion is known
- Produce a sensitivity map for the design
- There are clearly defined “hot” areas for SDC
- For each strike – designer knows the instance of the cell

Sensitivity Maps (ASTMR)



- Many fewer error locations (as expected)
- Still remain some “hot” regions for SDC
- Designers have detailed info for each failure event
- Are the remaining SDC/DUE events the results of SETs?

SETs – Back of the Envelope Analysis

- SETs in ProASIC3 have widths in the range of ≈3 ns [1,2]
- The design has logic paths with 39-44 layers of logic
  - Due to broadening SETs broadened by ≈2ns
- Based on 100 nsec clock period
  - Temporal SET masking : (2ns+3ns)/100ns=5%
- SEUs are also subject to temporal masking
  - Depends on slack analysis → about 50% in this design
- But 90% of the VersaTiles are combinatorial

	SEU	SET
Ratio of Cells	1x	10x
Temporal Masking	50%	5%
Logical Masking	comparable	comparable
Net Effect (a.u.)	**5**	**5**

- So – even at low frequency -> SET contribution can ne non-neglibible

[1] Rezgui. New methodologies for SET characterization and mitigation in Flash-based FPGAs. TNS 2007.
[2] Evans. New techniques for SET sensitivity and propagation measurement in Flash-based FPGAs. TNS 2014.

Simulation Analysis

- Using Modelsim to simulate post-layout gate-level netlist
- 100 randomly selected error cases were studied for **SEUs**
- X,Y co-ordinate and clock cycle are known – with some uncertainty
  - Each tuple (x,y,t) up to 27 simulations were performed : (x±1, y±1, t±1)
  - Only ran cases where target cell (x±1, y±1) is sequential (SEU)

These errors were likely caused by an SET rather than a SEU.

Simulation Category	%
Identical trace	31%
Close Match	23%
Classification Matched	14%
Not re-produced with SEU	32%

- Not yet performed SET fault injection simulations
  - Expect SET fault-injections to re-produce remaining cases

Future and Ongoing Work

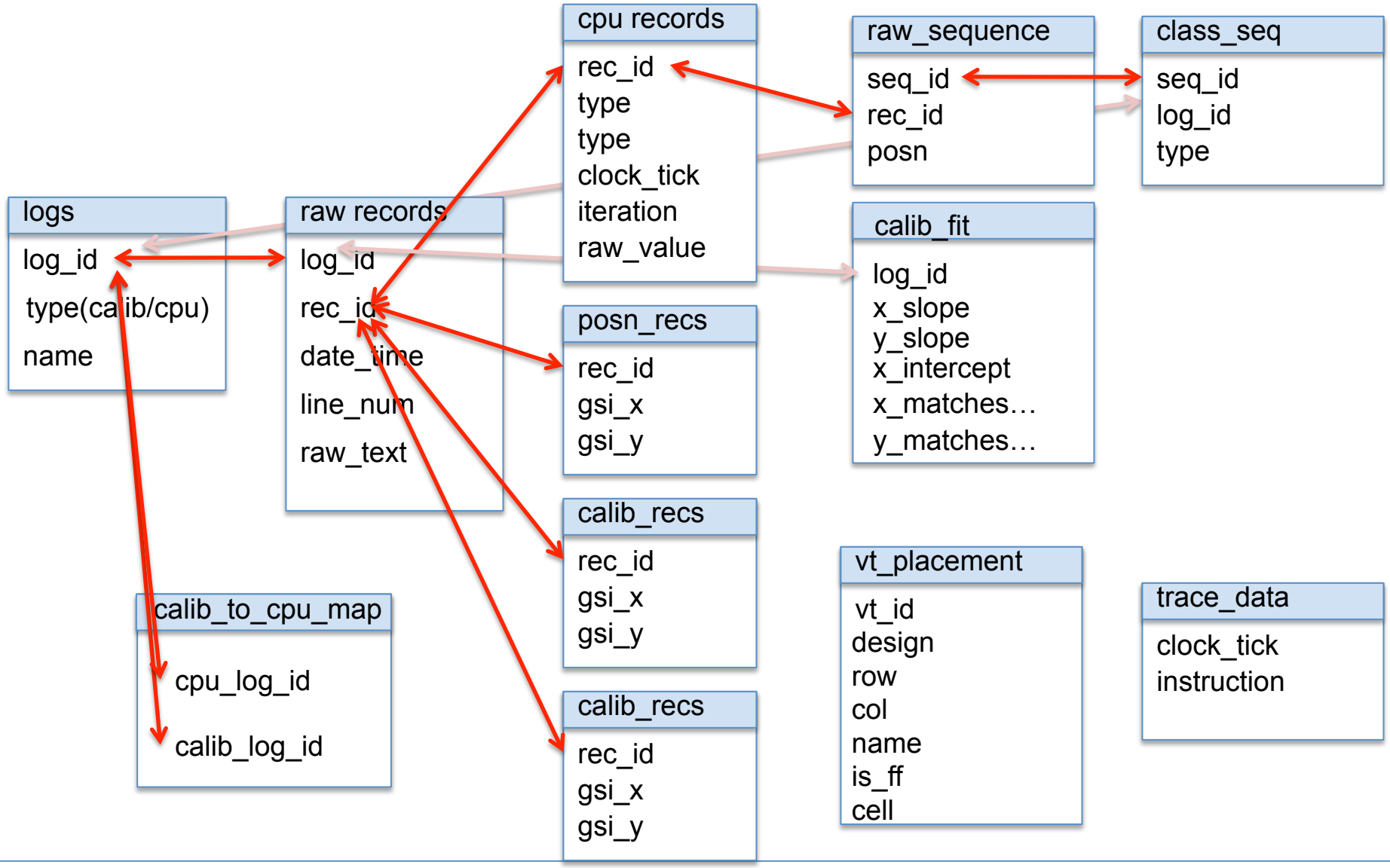
- Shown a detailed SDC/DUE/timeout analysis for a modern micro-controller
- Temporal and spatial location of each error case
- The specific weak points in the ASTMR design are fed to design team → improve protection
- SETs appear significant – even at low frequencies
- On-going work to perform SET fault-injections

Thank You!

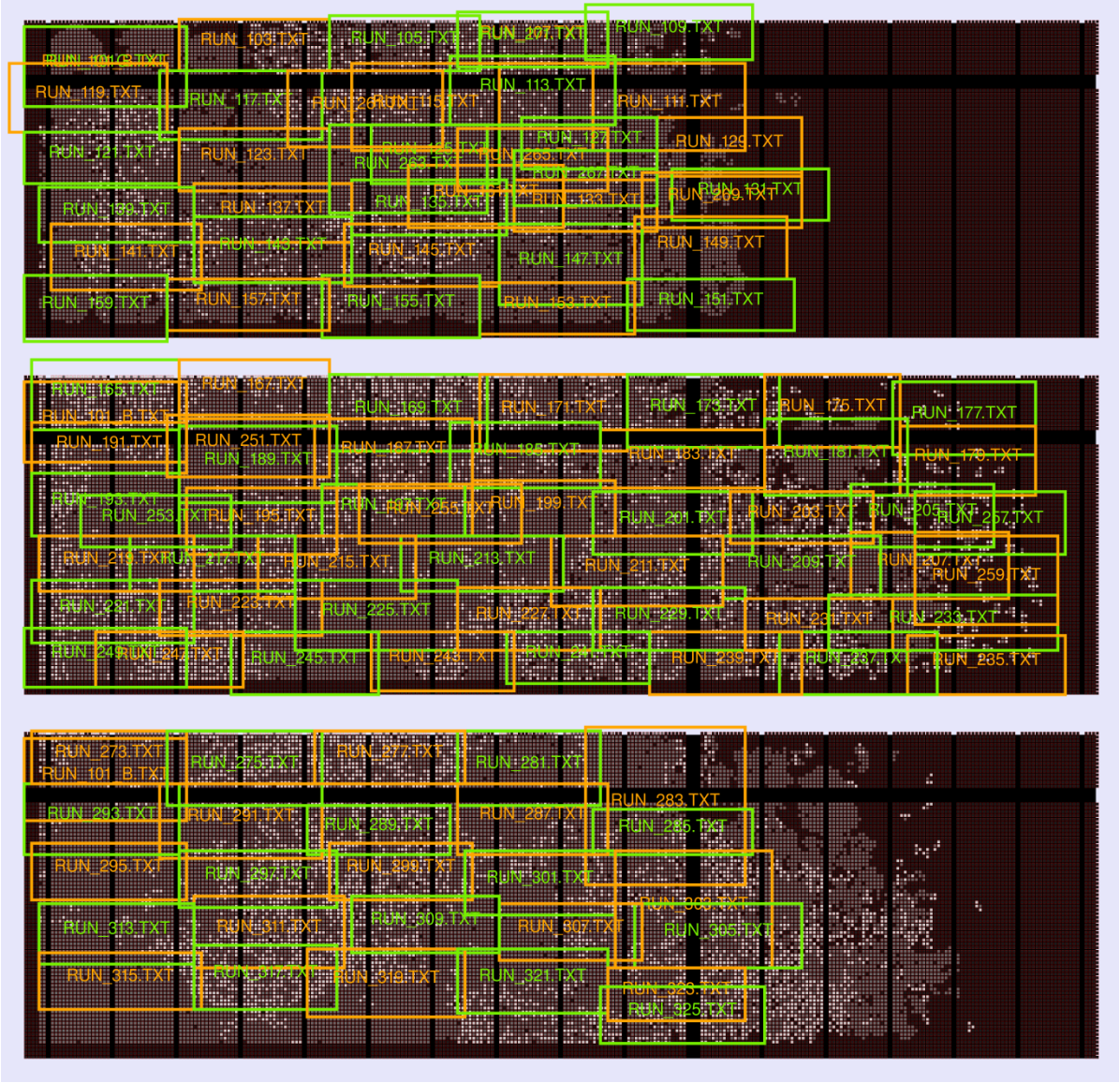
Questions?

Backup Slides

Data Base Schema



Tiling



Plain CPU
(15 297 cells, 2126 FF)

ATMR CPU
(21 378 cells, 5433 FF)

MTMR CPU
(19 291 cells, 4455 FF)

Note : FFs appear as brighter squares

Sample Error Trace

	A	B	C	D	E	F	G	H	I	J	K
1	sequence	class	log	tick	vt_x	vt_y	dx	dy	inst	type	is_ff
112	170845	DUE	RUN_116.TXT	13665	156	90	0	0	u_cmsdk_mcu/u_cmsdk_mcu_system/u_cm0pmtbintegration/u_cm0pintegration/u_imp/u_cortexm0plus	NOR3B	N
113							-1	-1	u_cmsdk_mcu/u_cmsdk_mcu_system/u_cm0pmtbintegration/u_cm0pintegration/u_imp/u_cortexm0plus	MX2	N
114							-1	0	u_cmsdk_mcu/u_cmsdk_mcu_system/u_cm0pmtbintegration/u_cm0pintegration/u_imp/u_cortexm0plus	MX2	N
115							-1	1	u_cmsdk_mcu/u_cmsdk_mcu_system/u_cm0pmtbintegration/u_cm0pintegration/u_imp/u_cortexm0plus	OR2A	N
116							0	-1	u_cmsdk_mcu/u_cmsdk_mcu_system/u_cm0pmtbintegration/u_cm0pintegration/u_imp/u_cortexm0plus	MX2	N
117							0	1	u_cmsdk_mcu/u_cmsdk_mcu_system/u_cm0pmtbintegration/u_cm0pintegration/u_imp/u_cortexm0plus	NOR2	N
118							1	-1	u_cmsdk_mcu/u_cmsdk_mcu_system/u_cm0pmtbintegration/u_cm0pintegration/u_imp/u_cortexm0plus	MX2	N
119							1	0	u_cmsdk_mcu/u_cmsdk_mcu_system/u_cm0pmtbintegration/u_cm0pintegration/u_imp/u_cortexm0plus	NOR2B	N
120							1	1	u_cmsdk_mcu/u_cmsdk_mcu_system/u_cm0pmtbintegration/u_cm0pintegration/u_imp/u_cortexm0plus	NOR2	N
121											
122	1671490	SDC	RUN_264.TXT	664	152	68	0	0	u_cmsdk_mcu/u_cmsdk_mcu_system/u_cm0pmtbintegration/u_cm0pintegration/u_imp/u_cortexm0plus	NOR2B	N
123							-1	-1	u_cmsdk_mcu/u_cmsdk_mcu_system/u_cm0pmtbintegration/u_cm0pintegration/u_imp/u_cortexm0plus	AX1B	N
124							-1	0	u_cmsdk_mcu/u_cmsdk_mcu_system/u_cm0pmtbintegration/u_cm0pintegration/u_imp/u_cortexm0plus	AO1	N
125							-1	1	u_cmsdk_mcu/u_cmsdk_mcu_system/u_cm0pmtbintegration/u_cm0pintegration/u_imp/u_cortexm0plus	AO1	N
126							0	-1	u_cmsdk_mcu/u_cmsdk_mcu_system/u_cm0pmtbintegration/u_cm0pintegration/u_imp/u_cortexm0plus	AO1	N
127							0	1	u_cmsdk_mcu/u_cmsdk_mcu_system/u_cm0pmtbintegration/u_cm0pintegration/u_imp/u_cortexm0plus	AO1	N
128							1	-1	u_cmsdk_mcu/u_cmsdk_mcu_system/u_cm0pmtbintegration/u_cm0pintegration/u_imp/u_cortexm0plus	NOR2B	N
129							1	0	u_cmsdk_mcu/u_cmsdk_mcu_system/u_cm0pmtbintegration/u_cm0pintegration/u_imp/u_cortexm0plus	AO1	N
130							1	1	u_cmsdk_mcu/u_cmsdk_mcu_system/u_cm0pmtbintegration/u_cm0pintegration/u_imp/u_cortexm0plus	XO1A	N
131											
132	174409	DUE	RUN_116.TXT	13303	156	81	0	0	u_cmsdk_mcu/u_cmsdk_mcu_system/u_cm0pmtbintegration/u_cm0pintegration/u_imp/u_cortexm0plus	DFN1E1P0	Y
133							-1	-1	u_cmsdk_mcu/u_cmsdk_mcu_system/u_cm0pmtbintegration/u_cm0pintegration/u_imp/u_cortexm0plus	NOR2B	N
134							-1	0	u_cmsdk_mcu/u_cmsdk_mcu_system/u_cm0pmtbintegration/u_cm0pintegration/u_imp/u_cortexm0plus	AO1	N
135							-1	1	u_cmsdk_mcu/u_cmsdk_mcu_system/u_cm0pmtbintegration/u_cm0pintegration/u_imp/u_cortexm0plus	NOR2B	N
136							0	-1	u_cmsdk_mcu/u_cmsdk_mcu_system/u_cm0pmtbintegration/u_cm0pintegration/u_imp/u_cortexm0plus	OR2	N
137							0	1	u_cmsdk_mcu/u_cmsdk_mcu_system/u_cm0pmtbintegration/u_cm0pintegration/u_imp/u_cortexm0plus	MX2	N
138							1	-1	u_cmsdk_mcu/u_cmsdk_mcu_system/u_cm0pmtbintegration/u_cm0pintegration/u_imp/u_cortexm0plus	OR2	N
139							1	0	u_cmsdk_mcu/u_cmsdk_mcu_system/u_cm0pmtbintegration/u_cm0pintegration/u_imp/u_cortexm0plus	DFN1E1P0	Y
140							1	1	u_cmsdk_mcu/u_cmsdk_mcu_system/u_cm0pmtbintegration/u_cm0pintegration/u_imp/u_cortexm0plus	MX2	N
141											

Neighbouring cells

SET

SEU?