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AEROSPACE & DEFENSE

Xilinx Virtex-5QV Update and Space Roadmap

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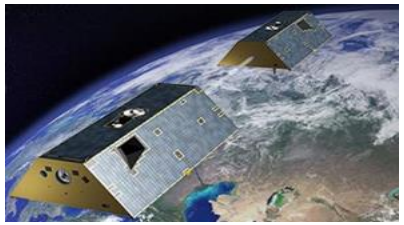
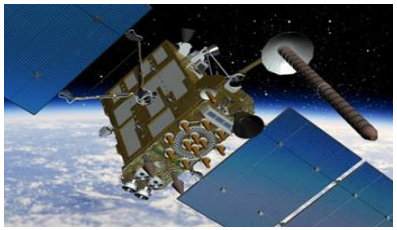
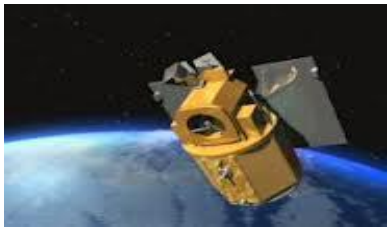
Space Marketing – Aerospace & Defense
17th, March, 2016

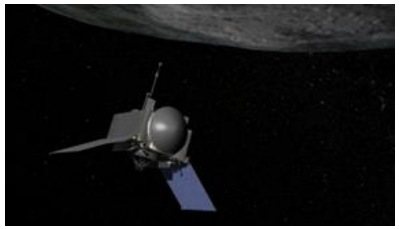
Status of V5QV

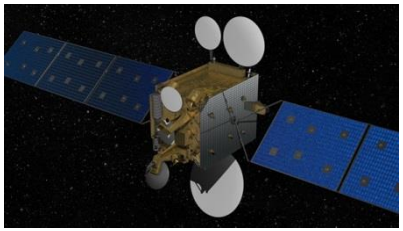
- **Many programs have built hardware and integrated into Spacecrafts – awaiting for launch**
  - Lots more V5QV implementations in progress spreading among Commercial, Civil, and Military applications
- **Silicon functionality, IPs, radiation, reliability, tool chains all validated by extensive user testing and qualifications**
  - All functional blocks validated with radiation, upset rate published
  - Mechanical implementation and manufacturing processes well established and qualified by many users
- **Major flight heritages accumulate since 2014**
- **QML-Y certification targeted by e/2016**
- **V5QV is now a mature product in stable production while accumulating heritages**
  - Life cycle has extended to late 2020s











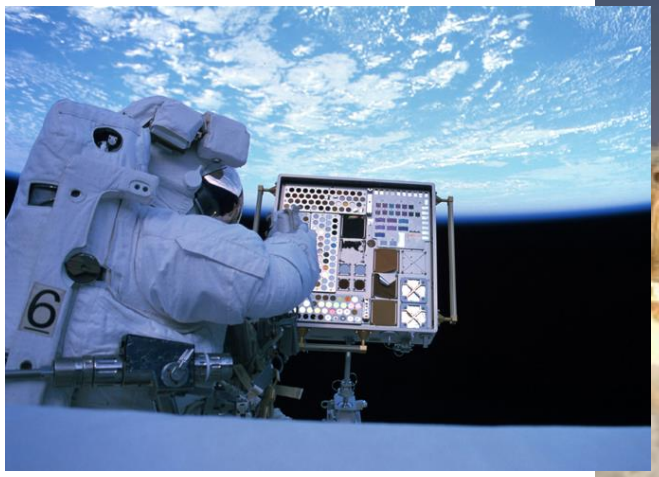
V5QV Reliability Demonstration

- **Qualification of V5QV completed**
  - 800,000+ device-hours established with lifetest @125ºC
  - Silicon wear-out mechanism qualification has already shown 30+ years non-stop operation @100ºC
  - Qualification report (RPT150) available upon request
- **Virtex-5QV completed 10K-Hour life test with no failures (43 units)**
  - 10,000 hours = 1.14 years non-stop operations @125ºC
  - or, equivalent to 4.48 years non-stop operations @100ºC
  - or, equivalent to 11.14 years non-stop operations @85ºC
- **Radiation total dose guaranteed to 1 MegaRad**
  - Timing/Power degradation due to total dose are ignorable
- **Radiation data validated by multiple parties – multi-year efforts**
  - SEL immune (tested to 135 LETs at 125ºC)
  - Configuration Memory Orbital Upset Rate at 2 upsets per year (GEO-Minimum), can be further reduced with Readback/Scrub Solutions
  - SEFI Orbital Upset Rate < 1 SEFI per every 4,000 years (GEO-Minimum)

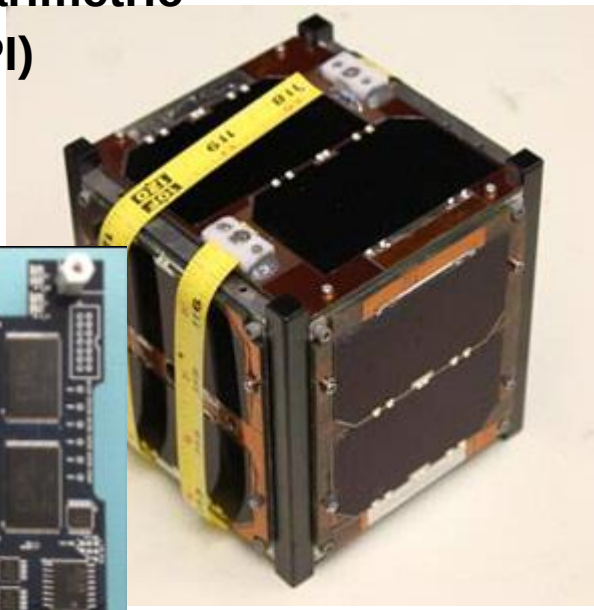
V5QV In-Orbit Validations since 2011

- *In-Orbit validation missions are critical for complex new FPGAs*
- *Ratified in-orbit prior to commitment to major asset programs*

- **MISSE-8 SEUXSE-II (Sandia)**
  - **Radiation Performance Validation by US Government**
  - **Launched May 2011**
  - **XQR4VFX60 & XQR5VFX130**

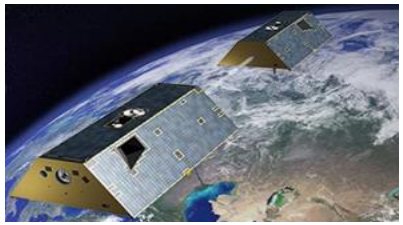
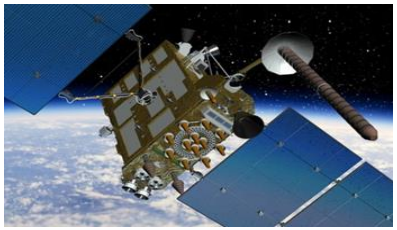
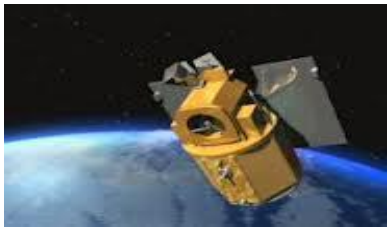
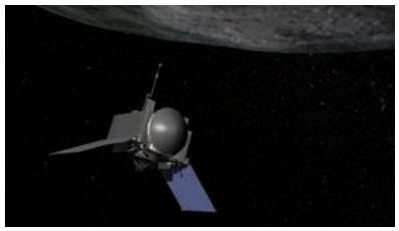
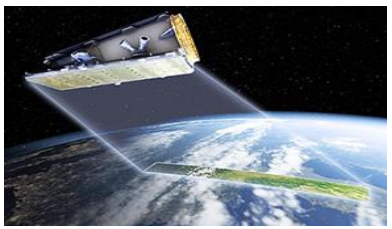


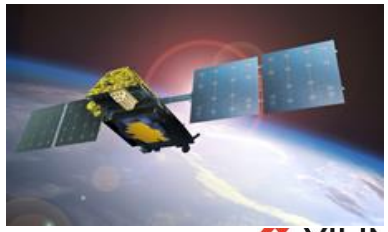
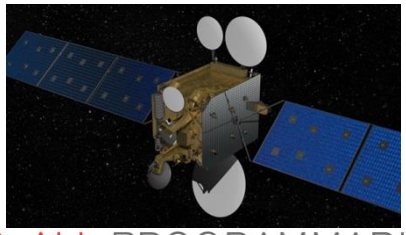
- **NASA JPL Mcubed/COVE-2**
  - **Validate V5QV for On-Board Processing with Multi-angle Spectro Polarimetric Imager (MSPI)**
  - **Launched Dec. 2013**



Typical Applications for V5QV - OBP

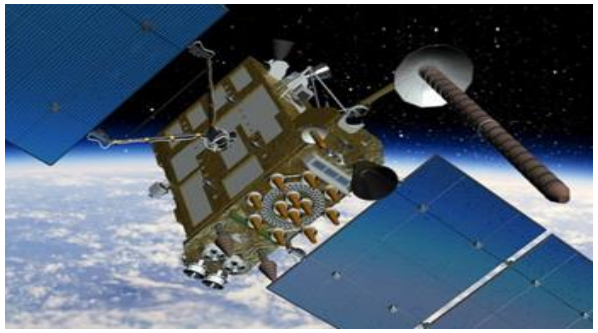
- **Communication Payload:**
  - Channelizer – RX/TX module, DSP Switches
  - High frequency down converter, Modulation, De-Modulation
  - Beamforming Modems & Crypto Unit, Ethernet Routers/Switches
  - Payload frequencies reconfiguration - defeating jamming threats
- **Imaging (remote sensing, space telescopes):**
  - ADC data conversion, Imaging data processing & compression
- **Synthetic Aperture Radar (SAR)**
  - High Speed Digitizer, Timing Generator Module, Baseband data processing, data compression, mass memory storage
- **GPS –** Digital Waveform Generators
- **Manned Crew Capsules**
  - Video processor and Displays for Crew Capsules avionics
  - C&DH (Command and Data Handling)

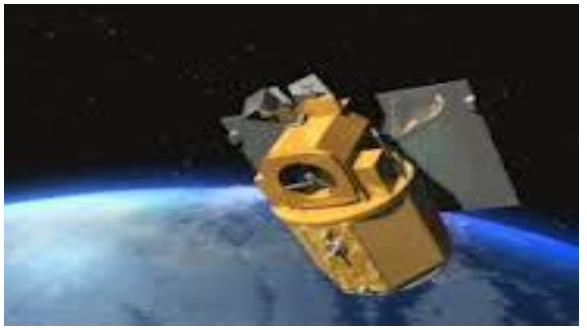



Missions with Virtex-5QV – *More in Pipeline*

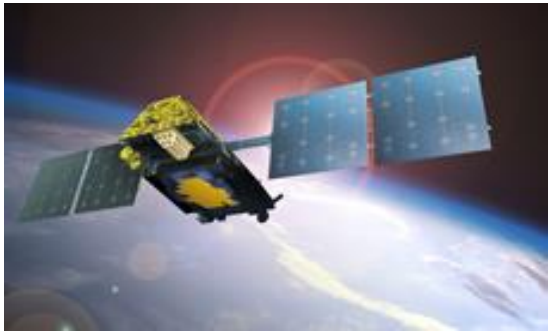
MISSE-8 ISS
(2011 Launch)



Glonass-K
(2014 1st Launch)

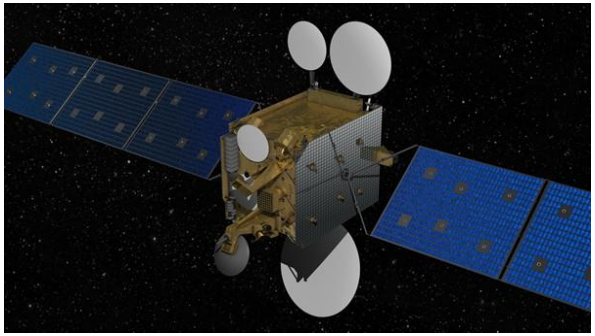


Formosat-5
(June 2016 Launch)

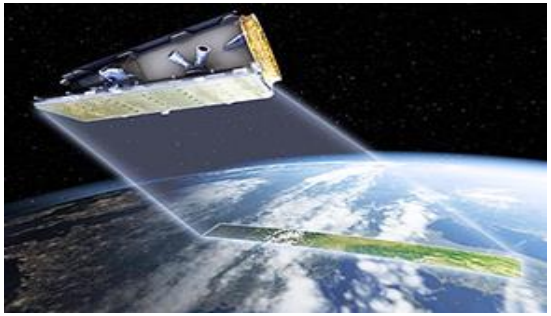


Iridium Next (66+6+9)
(July 2016 1st Launch)

US Classified
(Multiple Programs)

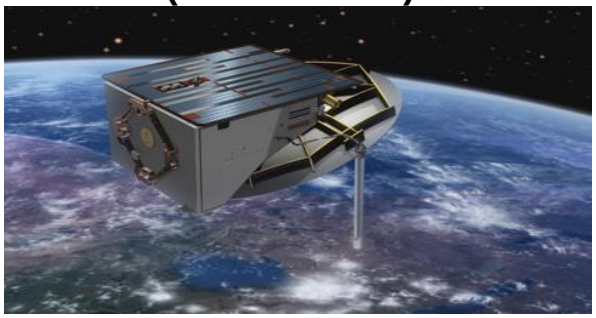


DLR H2 Comm. Sat.
(2020 Launch)



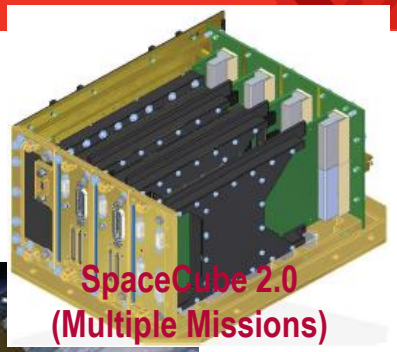
NovaSAR
(2017 Launch)

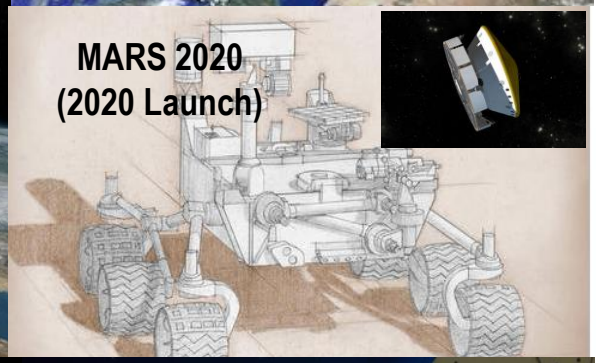
Cosmo Skymed NextGen
(2017 Launch)



SAR-Lupe NextGen
(2019 Launch)

NASA Missions with Virtex-5QV CCGAs
– V5QV utilized in many major programs





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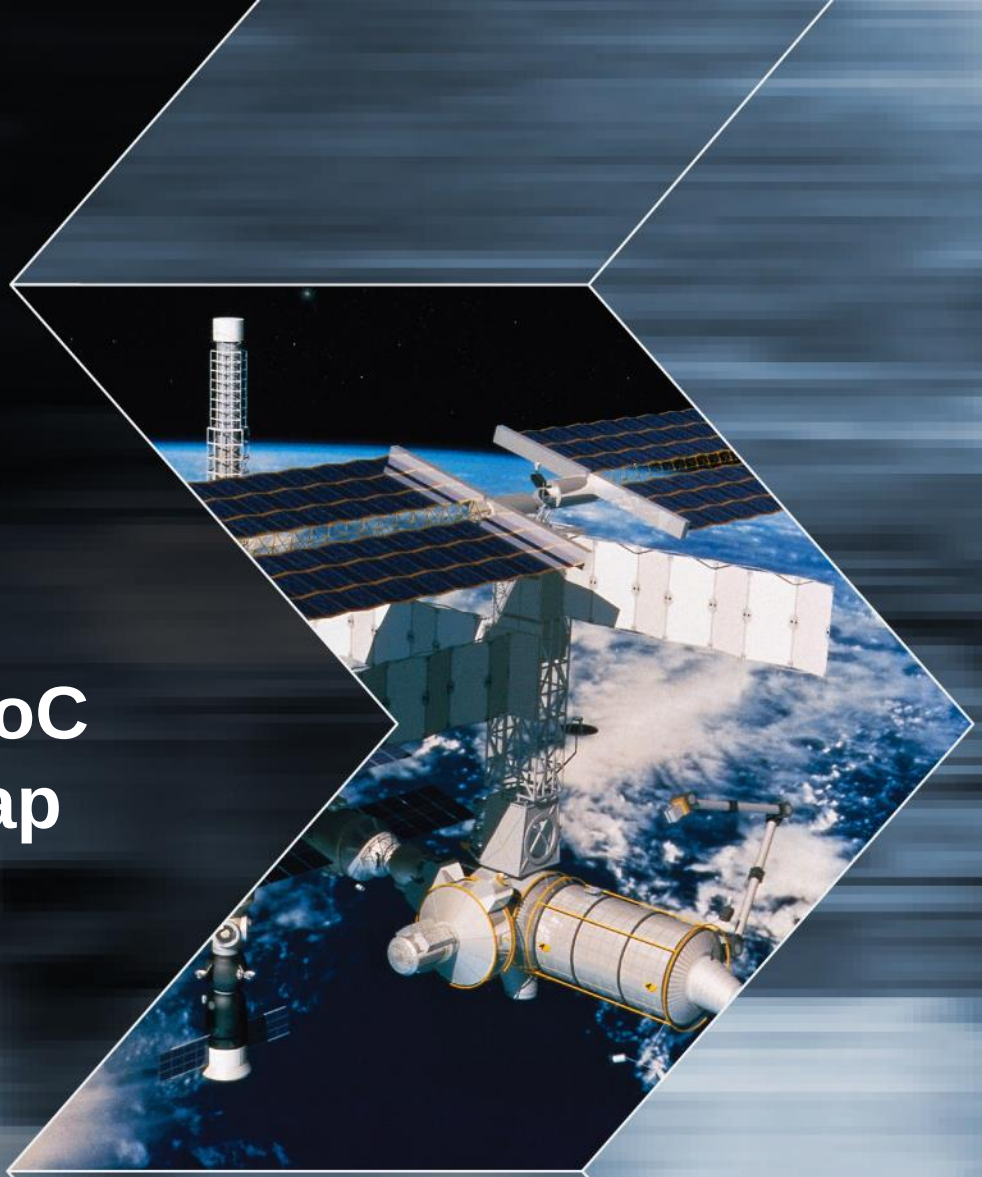
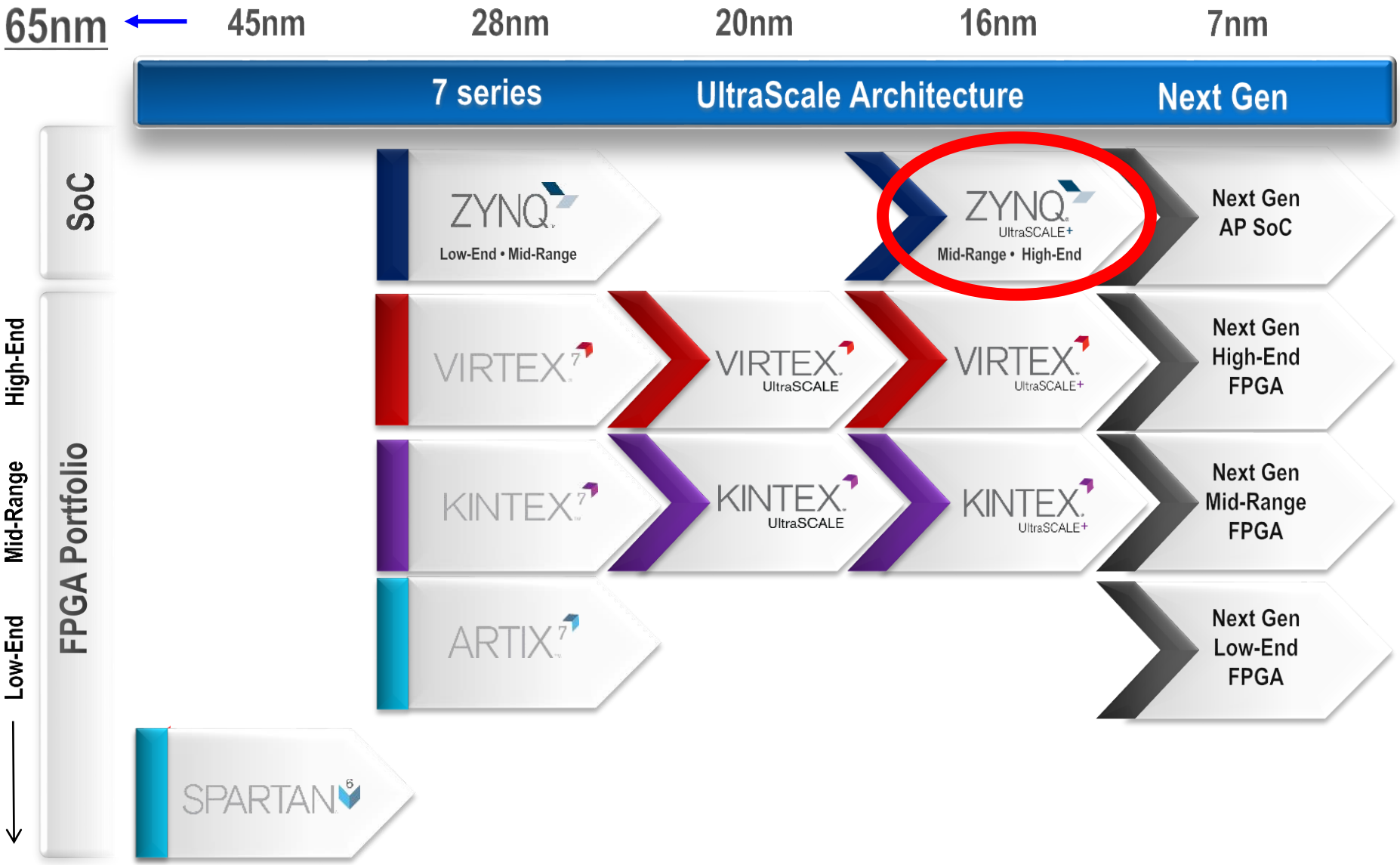


Zynq UltraScale+ MPSoC - Space Grade Roadmap

Xilinx All Programmable Portfolio



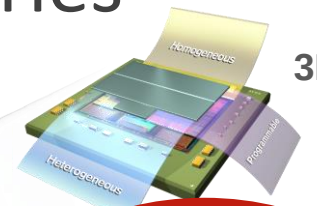
Generational Advancements – Since 7-Series

V5QV at 65nm Remains the most advanced
Space FPGA Offering since 2011
Based on 65nm V5 technology introduced in 2006

Programmable Systems Integration

Surpassing Moore's Law
Unprecedented Capacity & Performance
System Intelligence & Integration
Silicon + Architecture for Price/Performance/Watt

Break Out



3D IC

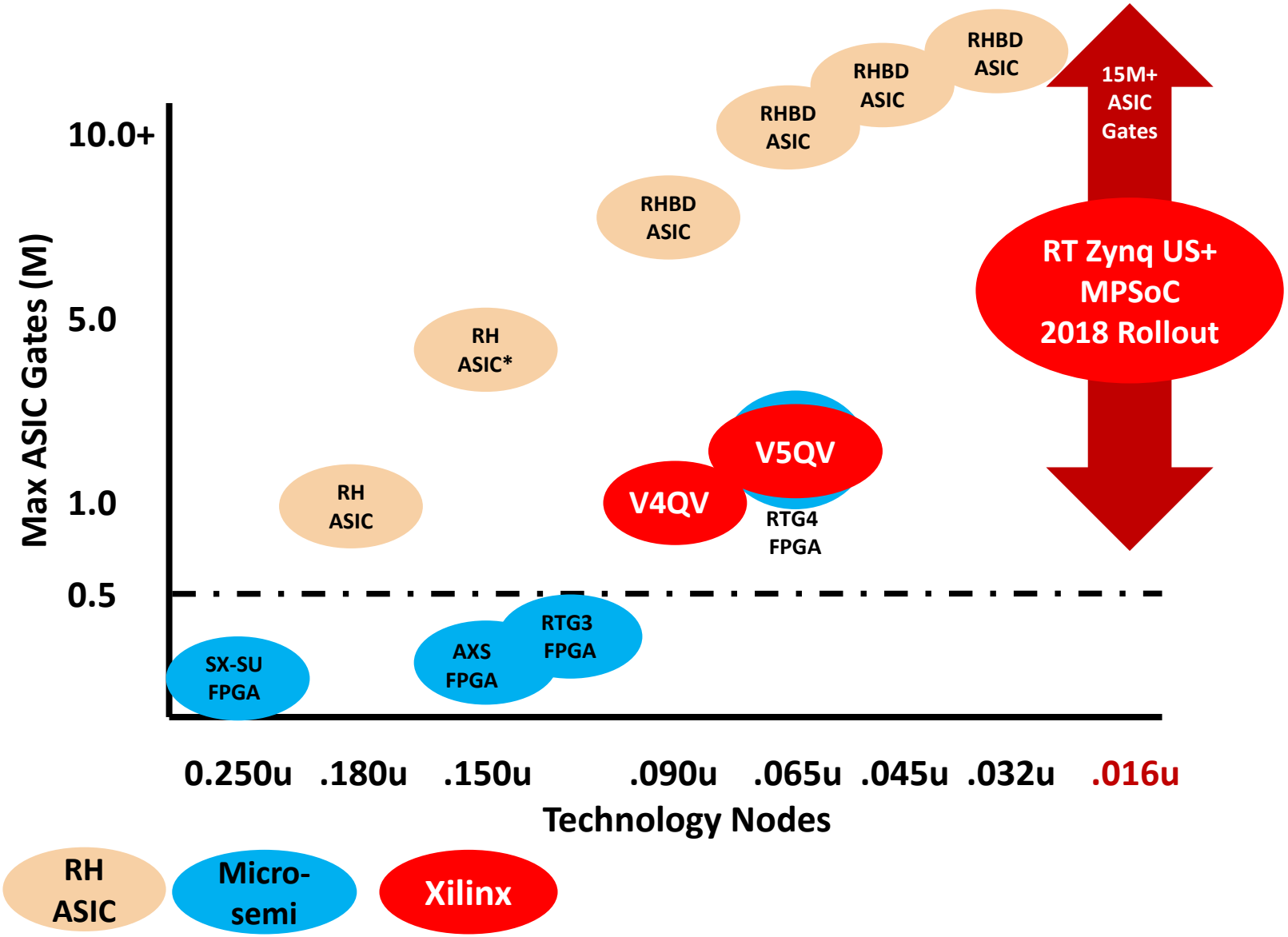
SoC

FPGA

Target for Next Generation Space

Tools	VIVADO	UltraFAST Design Methodology	SDx Environments	
Architecture	7 Series	UltraScale™ Architecture		
Process	28 nm HPL	20 nm SoC	16 nm FinFET+	7 nm

Space FPGA/ASIC Landscape



RT Zynq UltraScale+ MPSoC Product Roadmap

- **First RT to rollout is ZU19EG with 45mm CCGA package**
  - RT-ZU19EG rollout in 2018, one year after the completion of all US+ commercial rollout in 2017
- **Advantage of Zynq UltraScale+ MPSoC for Space Applications**
  - Zynq UltraScale+ MPSoC is the most capable FPGA family for Space PLDs
    - Abundant resources (LCs, SRAMs, DSPs, SERDES, etc.)
      - ZU19EG has ~1M LC, provides ~10x resources of V5QV + Processors
  - Second generation Zynq Multi-Processing SoC (MPSoC) implementation
    - Same Zynq tool flow and same device programming flow
    - Minimum overhead for applications don't need Processors (Turn-off after power up)
  - 2X performance per watt to equivalent 7-Series devices
  - Similar silicon design as commercial parts
    - Initial radiation test data is satisfactory for Space – *No need for RHBD re-design*
  - Take full advantage of Vivado/HLS/SDx and IPs
  - Early assessment for 16nm Zynq US+ MPSoC technology available now
    - Vivado software for Zynq US+ MPSoC available now
    - Initial Zynq US+ MPSoC device (ZU9EG) and evaluation kit available in 2016
    - Pin compatible ZU19EG commercial device available in 1H2017

XQR5VFX130 vs RT-ZU19EZ

	XQR5VFX130	RT-ZU19EG
Technology Node	65nm	16nm
Rollout	2011	2018
Process	Planar CMOS	3D FinFET
Radiation Hardening	RH-BD	Rad Tolerant
Logic Cell (LC)	131k	1,143k
Total On-Chip Memory	12.3 Mb	80.4 Mb
DSP Slice	320	1,968
SERDES Lines/Speeds	18 / 4.5 Gbps	52 6/16/33 Gbps
Processors	Soft IP cores	Quad-A53 Dual-R5 Mali-GPU Soft IP cores
Package	45mm, 1mm pitch, 1752 pin CCGA	

Zynq US+ MPSoC Device Portfolio Summary

			Smarter Control and Vision					Smarter Network					
		Device Name[1]	ZU2EG	ZU3EG	ZU4EV	ZU5EV	ZU7EV	ZU6EG	ZU9EG	ZU15EG	ZU11EG	ZU17EG	ZU19EG
Processing System (PS)	Application Processor Unit	Processor Core	**Quad-core** ARM® Cortex™-A53 MPCore™ up to 1.5GHz										
		Memory w/ECC	L1 Cache 32KB I / D per core, L2 Cache 1MB, on-chip Memory 256KB										
	Real-Time Processor Unit	Processor Core	**Dual-core** ARM Cortex-R5 MPCore™ up to 600MHz										
		Memory w/ECC	L1 Cache 32KB I / D per core, Tightly Coupled Memory 128KB per core										
	Graphic & Video Acceleration	Graphics Processing Unit	Mali™-400 MP2 up to 667MHz										
		Memory	L2 Cache 64KB										
	External Memory	Dynamic Memory Interface	x32/x64: DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 with ECC										
		Static Memory Interfaces	NAND, 2x Quad-SPI										
	Connectivity	High-Speed Connectivity	PCIe® Gen2 x4, 2x USB3.0, SATA 3.1, DisplayPort, 4x Tri-mode Gigabit Ethernet										
		General Connectivity	2xUSB 2.0, 2x SD/SDIO, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO										
	Integrated Block Functionality	Power Management	Full / Low / PL / Battery Power Domains										
		Security	RSA, AES, and SHA										
		AMS - System Monitor	10-bit, 1MSPS - Temperature, Voltage, and Current Monitor										
PS to PL Interface			12 x 32/64/128b AXI Ports										
Programmable Logic (PL)	Programmable Functionality	System Logic Cells (K)	103	154	192	256	504	469	600	747	653	926	1,143
		CLB Flip-Flops (K)	94	141	176	234	461	429	548	682	597	847	1,045
		CLB LUTs (K)	47	71	88	117	230	215	274	341	299	423	523
	Memory	Max. Distributed RAM (Mb)	1.2	1.8	2.6	3.5	6.2	6.9	8.8	11.3	9.1	8.0	9.8
		Total Block RAM (Mb)	5.3	7.6	4.5	5.1	11.0	25.1	32.1	26.2	21.1	28.0	34.6
		UltraRAM (Mb)	-	-	14.0	18.0	27.0	-	-	31.5	22.5	28.7	36.0
	Clocking	Clock Management Tiles (CMTs)	3	3	4	4	8	4	4	4	8	11	11
	Integrated IP	DSP Slices	240	360	728	1,056	1,728	1,973	2,520	3,528	2,928	1,590	1,968
		Video Codec Unit (VCU)	-	-	1	1	1	-	-	-	-	-	-
		PCI Ex					2	-	-	-	4	4	5
							-	-	-	-	2	2	4
		100G Eth					-	-	-	-	1	2	4
							1	1	1	1	1	1	1
	Speed Grades									-1 -2L -3			
		Industrial	-1 -1L -2							-1 -1L -2			

Target is the ZU19EG as the 1st Space Grade Device (Largest Monolithic part)

Notes:
1. For full part number details, see the Ordering Information section in DS891, *Zynq UltraScale+ MPSoC Overview*.
2. -2LE (Tj = 0°C to 110°C). For more details, see the Ordering Information section in DS891, *Zynq UltraScale+ MPSoC Overview*.

RT Zynq UltraScale+ MPSoC Benefits

- **Solution for the next 15+ years**
  - Highest performance SoC with rich features support long term evolving needs
  - Long product life cycle protects users' R&D investments
- **Extend V5QV implementation experience to RT US+ MPSoC**
  - ZU19EG provides ~10x capabilities at similar level of power as V5QV
  - Same size 45mm CCGA package at 1mm pitch
  - Similar thermal mechanical and PCB fabrication/assembly/reliability
- **Extend 16nm investments to both terrestrial and space applications**
  - Same design tools, IPs, and FPGA architectures
  - Use XC/XQ for terrestrial applications and RT for space
- **16nm Zynq US+ MPSoC ready for customer assessments**
  - 2016: Software, Evaluation Kit, ES parts, etc.
  - 2017: All 16nm commercial devices available and qualified
  - 2018: RT-ZU19EG available
    - RT-ZU19EG will qualify the entire Zynq US+ MPSoC family for space applications

Xilinx Space Advantages

- **V5QV is proven and well adopted by Space community**
  - Rich resource of Logic Cells, DSPs, and Connectivity IPs
  - All key Prime Users have established V5QV based Flexible Onboard Computing Platform for payload processing
    - Re-use single hardware design for all missions with minimum modifications
- **RT-ZU19EG provides upgrade path for V5QV platform to achieve another 10x performance enhancements**
  - Only Xilinx FPGA has the resources and performance capable of addressing next generation wide bandwidth communication data processing and high definition imaging data compression
  - Hardware/thermal/assembly/reliability infrastructure for V5QV based systems equally applicable to RT-ZU19EG
- **Xilinx Space is the only in-orbit reconfigurable solution provider with long history of proven reliability and heritages**
  - Virtex, Virtex-II, Virtex-4, Virtex-5, … plus up coming RT Zynq US+ MPSoC
  - Path to accomplish system level reduction of BOM and SWaP
  - Capable for in-orbit design updates, optimizations, and repairs

Thanks,