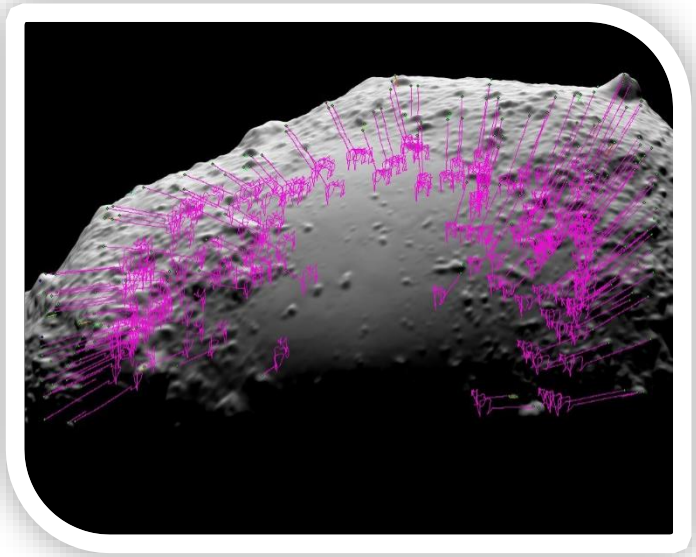
SEFUW Workshop 2016 - ESTEC

FPGA Acceleration for Space Vision-Based GNC Systems

17th March 2017



David González-Arjona
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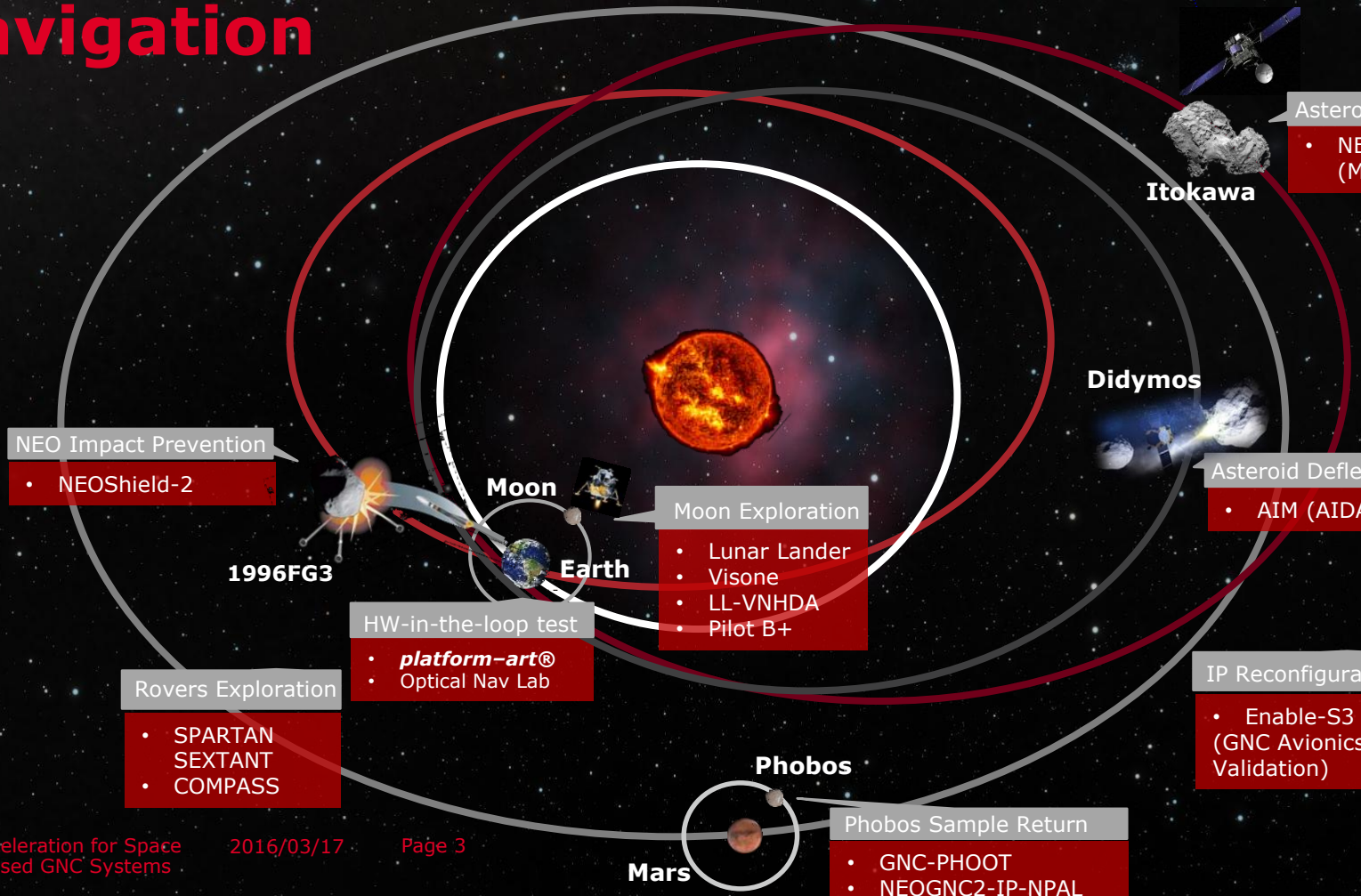
gmv INNOVATING SOLUTIONS

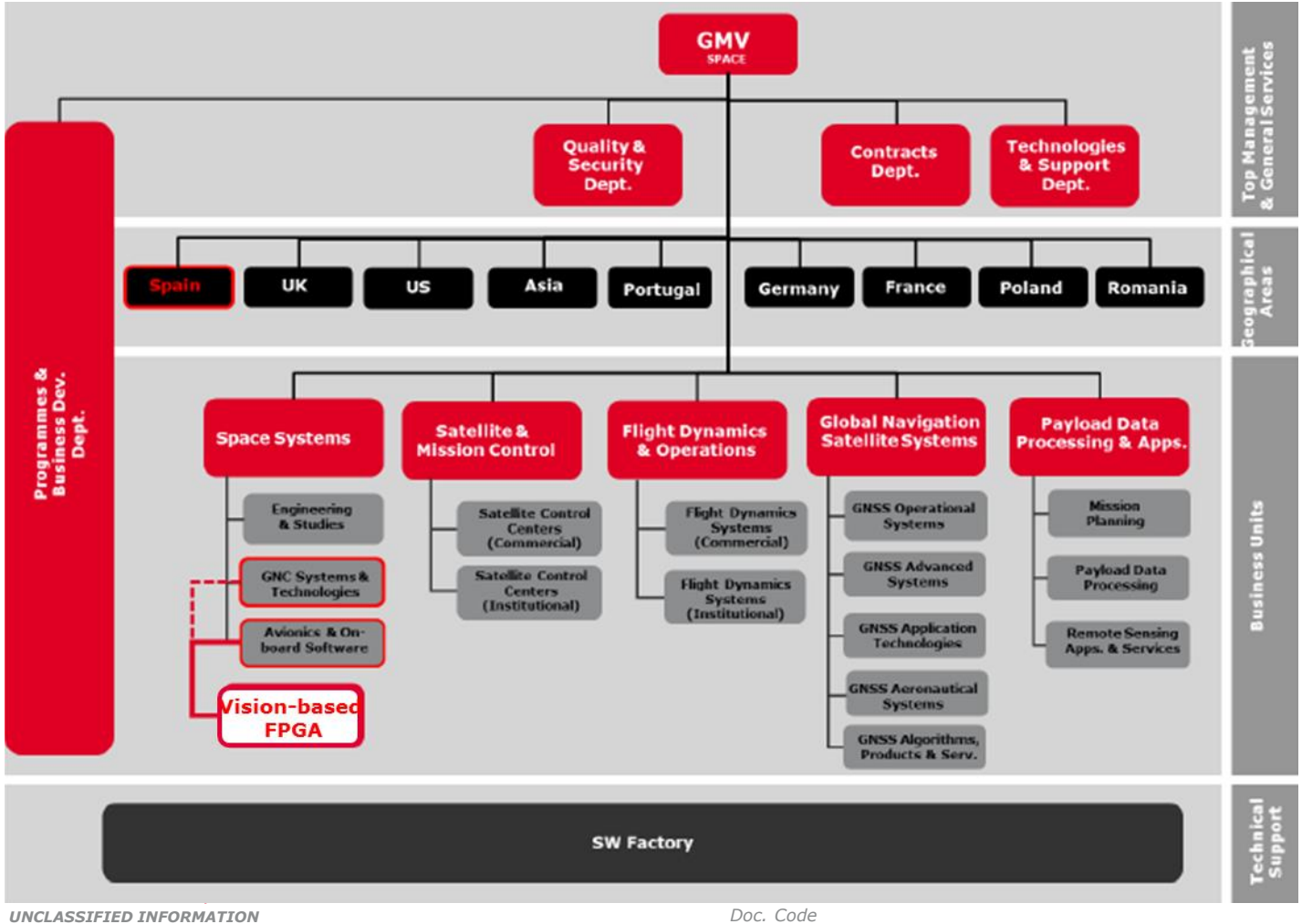
FPGA Acceleration

GMV IN THE WORLD (and beyond)

GMV FPGA projects for Vision-Based Navigation



GMV Aerospace & Defense



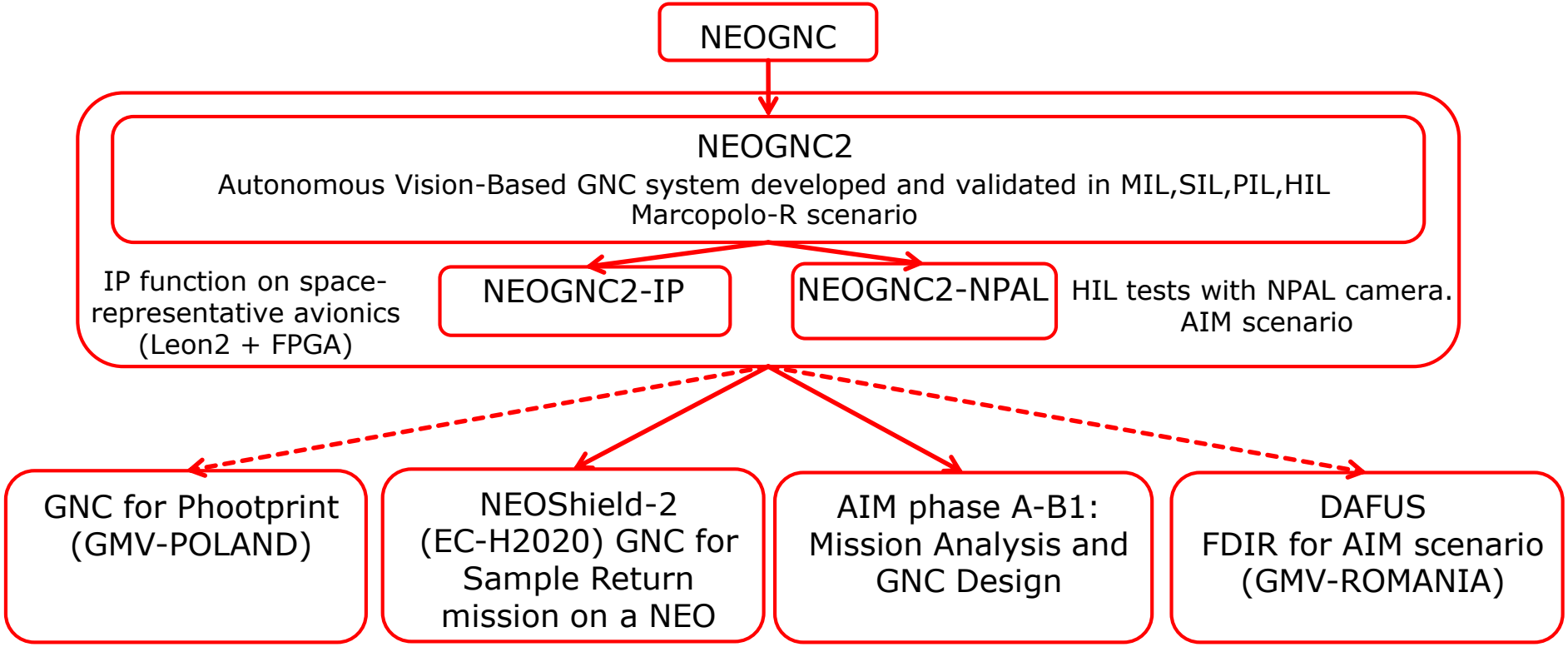
Founded in 1984

GMV Headquarters in Tres Cantos, Madrid (Spain)

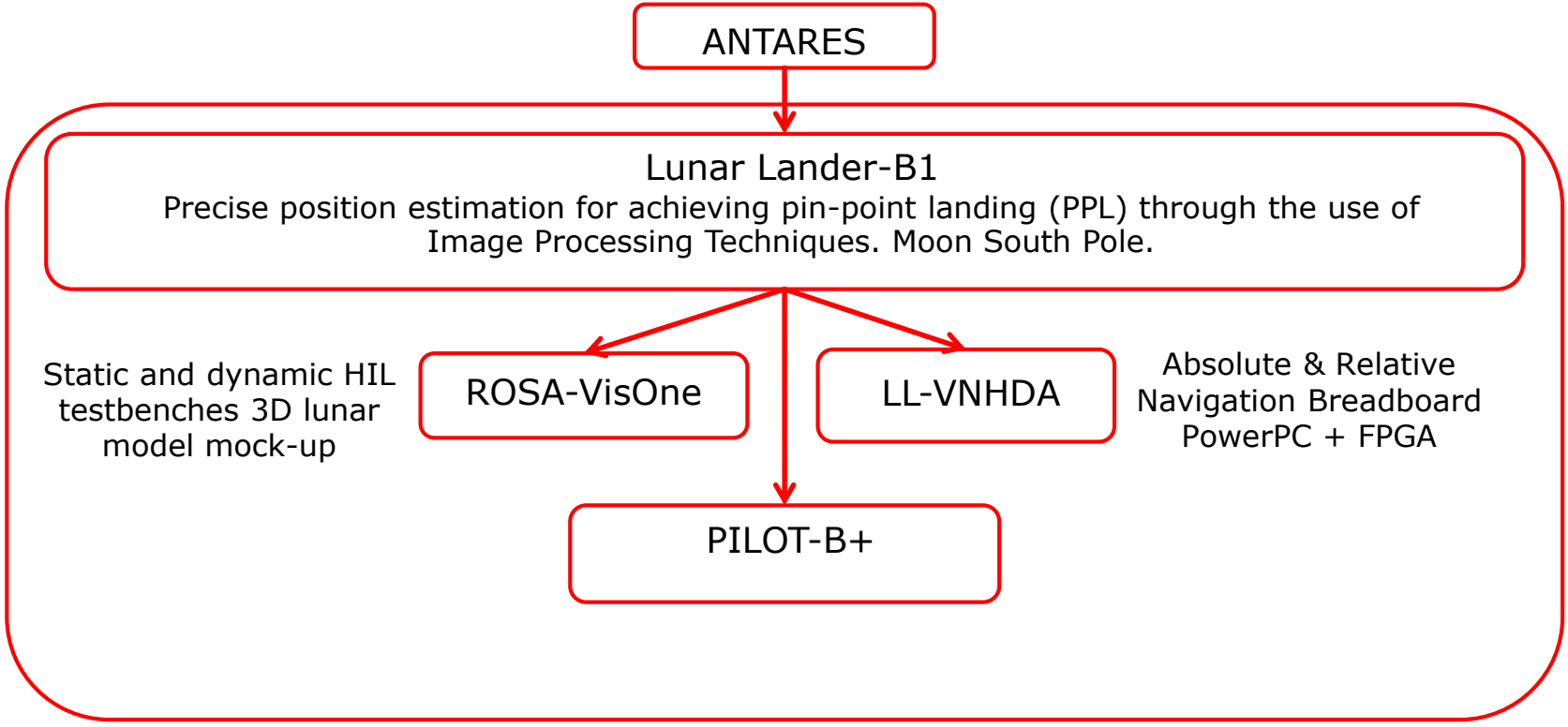
GMV employs more than 1400 staff.

Its Space business generates about 62% of the total turnover and employs over 500 people.

GMV's Related Activities I



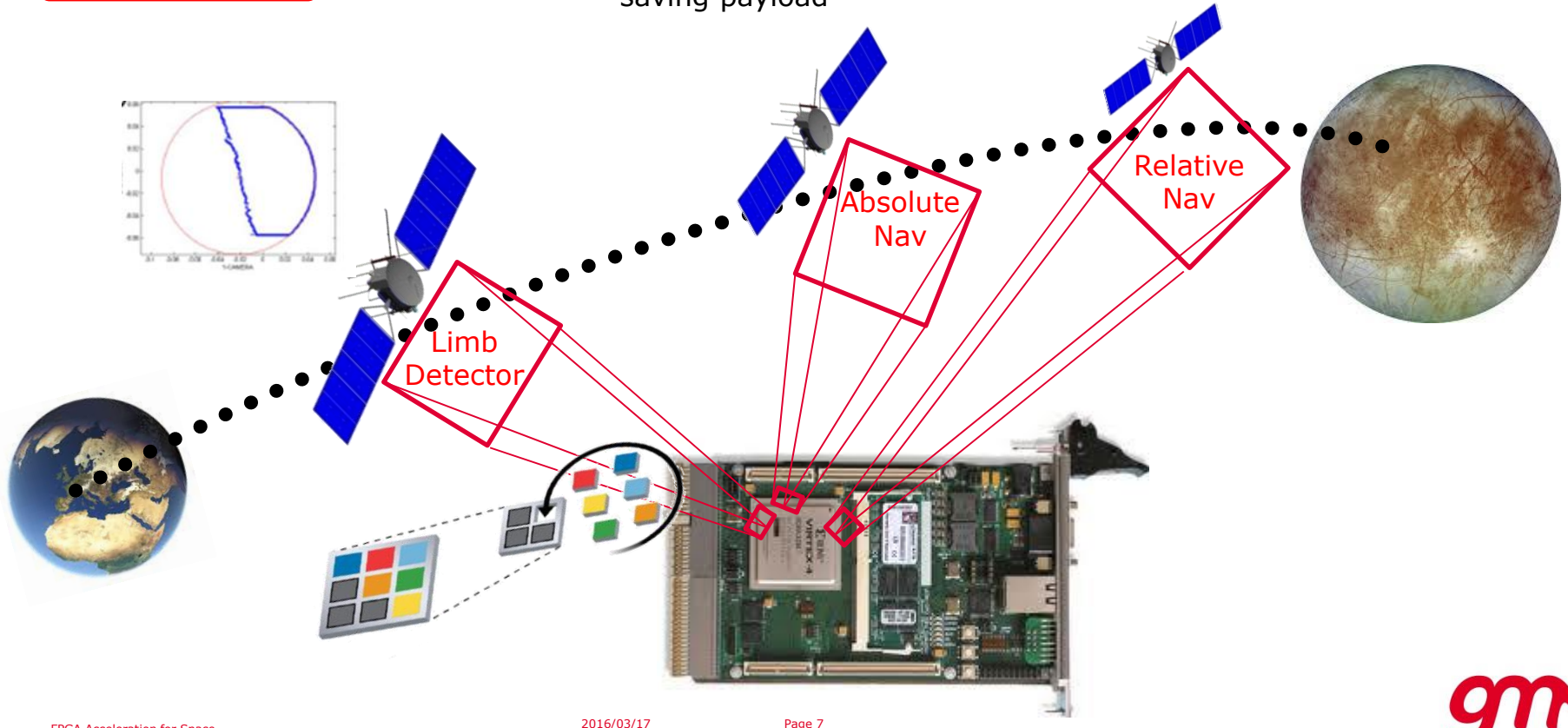
GMV's Related Activities II



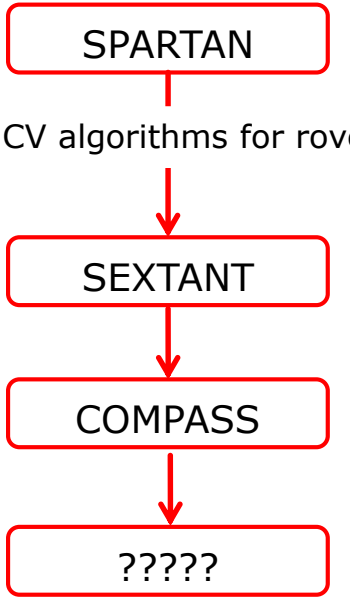
GMV's Related Activities III

ENABLE-S3

In-Flight Reconfiguration for different mission phases saving payload



GMV's Related Activities IV

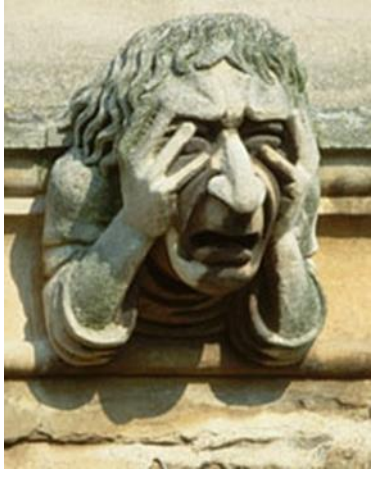


FPGA Acceleration

High-Performance Development

Avionics Development

John F. Wakerly: “If it wasn’t hard, they wouldn’t call it Hardware”



Gargoyle on the bell-tower of New College, Oxford: symbol of students suffering in HW labs

Design Metrics

The best solution is not the most complex, is the one that optimizes the tradeoff between all the different design metrics

Cost

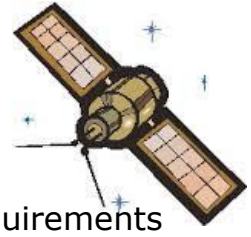
- Unit cost: The cost of manufacturing each unit (just the component and assembly costs)
- NRE (Non-Recurring Engineering Cost): The one-time cost of designing the system (includes prototyping)

Performance

- Most important: Ability to work in real time
- Time to give a response to the user (e.g. navigation system)

Physical Constraints

- Size
- Power
- Weight



Interfaces and Communication Requirements

Development time

- Time-to-protoype: The time needed to build a first working version of the system
- Time-to-market: The latter time, plus the time to manufacture the product and distribute it to the resellers

Radiation/Fault Tolerance

- Rad-hard components
- Mitigation techniques
- Fault-tolerant designs

Other design issues

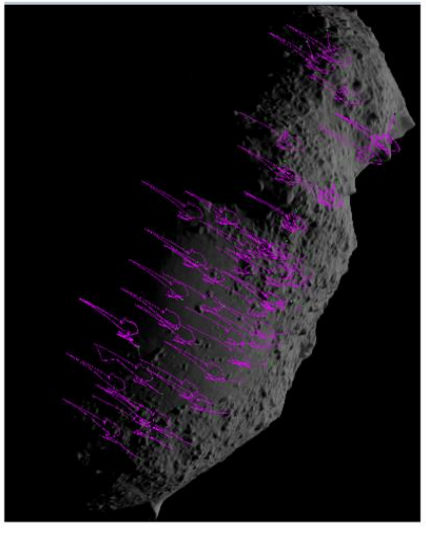
- Flexibility: the system can be used for different tasks without significantly increasing the NRE or the unit costs
- Maintainability: the system can easily be updated and/or repaired
- Fail-safe operation: Necessary in mission-critical systems, like life support

Relative Navigation as Example

- 20º FOV, 1024x1024 10-bits / Spacewire / 10Hz
- 100-200 detected/tracked features

Detection carried out over first fmage.
100 good features to track selected&sorted in IP
10 features selected as input for Navigation Filter

Tracking of Features List after n iterations



HW/SW co-design at GMV

Concurrent development approach for both hardware and software considerations at the same time

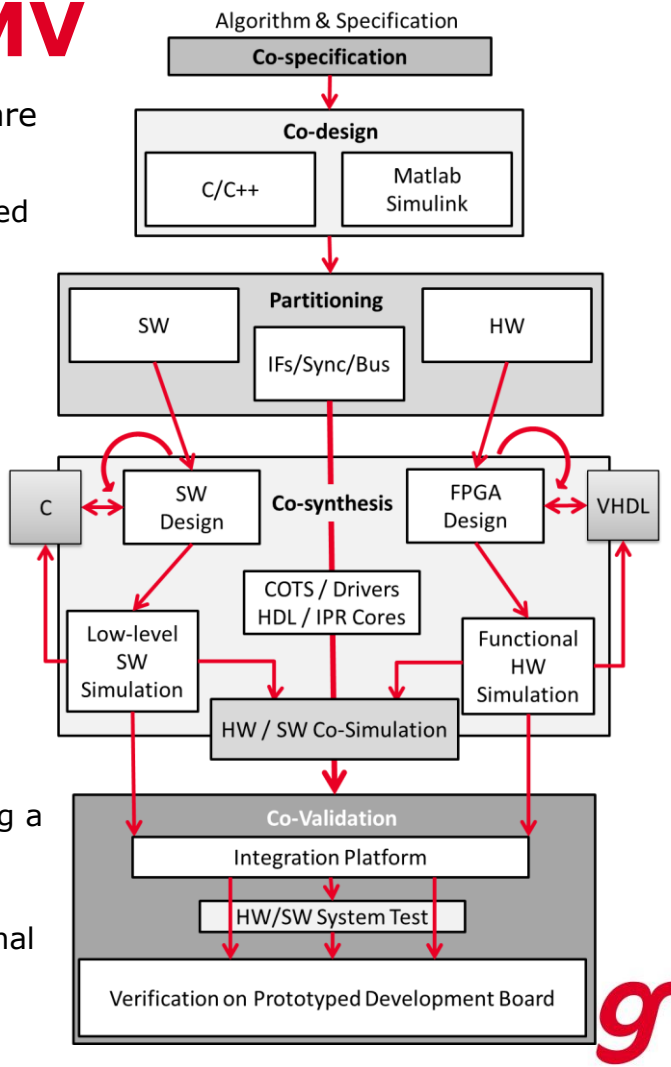
- **Partitioning:** defines the subdivision of modules to be implemented in HW, trading-off different HW platforms, and the ones to be implemented in SW running on a processor.
- 4 Phases:

  Co-specification describes the system *functionality* independently of the system architecture. Extraction of requirements considering interfaces and *non-functional* constraints, as performance, power consumption, physical constraints, mass …

  Co-design process refines previous approach to synthesize the system specification onto the HW and SW implementations mapping system functions and several parameters estimations. Provides to **Partitioning** with representative and functional SW models which are profiled.

  Co-synthesis starts development point of both HW and SW components as well as HW/SW interfaces into the platform using a proper tool. Validation of each component is performed.

  Co-validation checks that baseline requirements are met by means of formal validation, simulation or validation on target final architecture system (breadboarding)



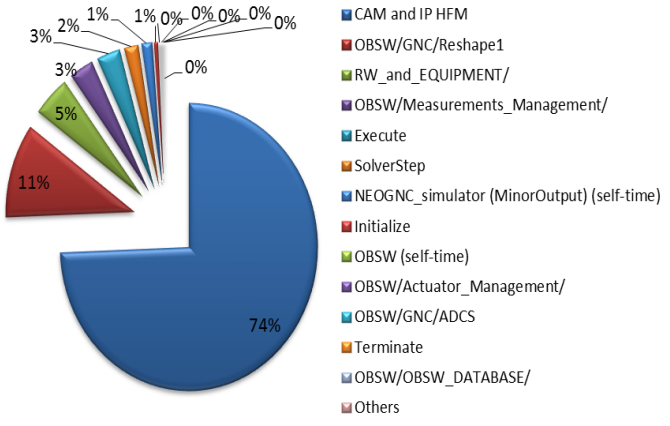
HW acceleration

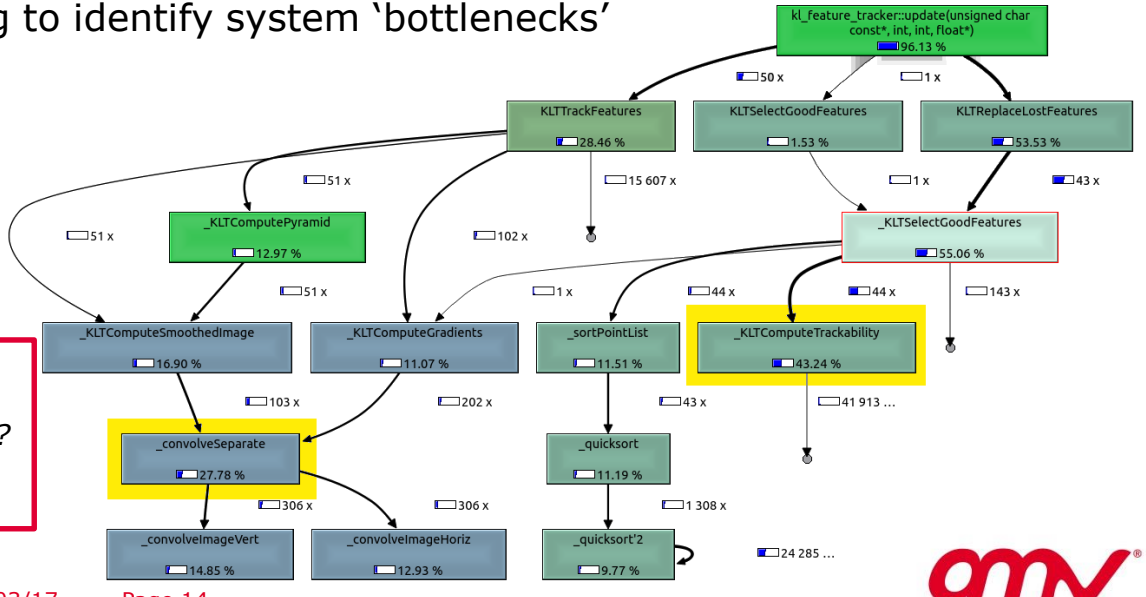
- Profiling execution of Image Processing C-code (time per each frame processed)
  - Leon2 (86 DMIPS): **60-80 seconds**.
  - PowerPC750 (1800 DMIPS): **27 seconds**
- 1Hz-2Hz mission GNC requirement
- HW acceleration is a must. Profiling to identify system 'bottlenecks'
- Most of the time spent in different type of convolutions
- Intensive use of memory
- Save time/memory target

Is it possible to speed-up the algorithm?

Is it possible to paralellize parts of the algorithm?

Paralellism, Pipeline, Synchronization





Justification for HW Implementation

Autonomy is really needed:

- **Delay in communications due to the distance to the SC;**
- **Delay in performing on-ground navigation using both images and RARR measurements and manoeuvre optimization by an operator/operators;**
- **Further pointing constraints of HGA (high gain antenna) and camera at the same time**

Example of expected performances for GNC systems projects:

Performances required at the moment of lander release (200m altitude starting from 4km altitude for 1.5 h trajectory duration, with nav at 1Hz):

- [0.3 0.03 0.03] cm/s LVLH (1-sigma)
- [10 5 5] m LVLH (1-sigma)

Performances required at the moment of landing (20m last manoeuvre from 500m altitude for 0.3h trajectory duration, with nav at 1Hz):

- [1 0.1 0.1] cm/s LVLH (1-sigma)
- [0 25 25] m LVLH (1-sigma) (we are landing, so zero at the end in X)

Avionics Architectures

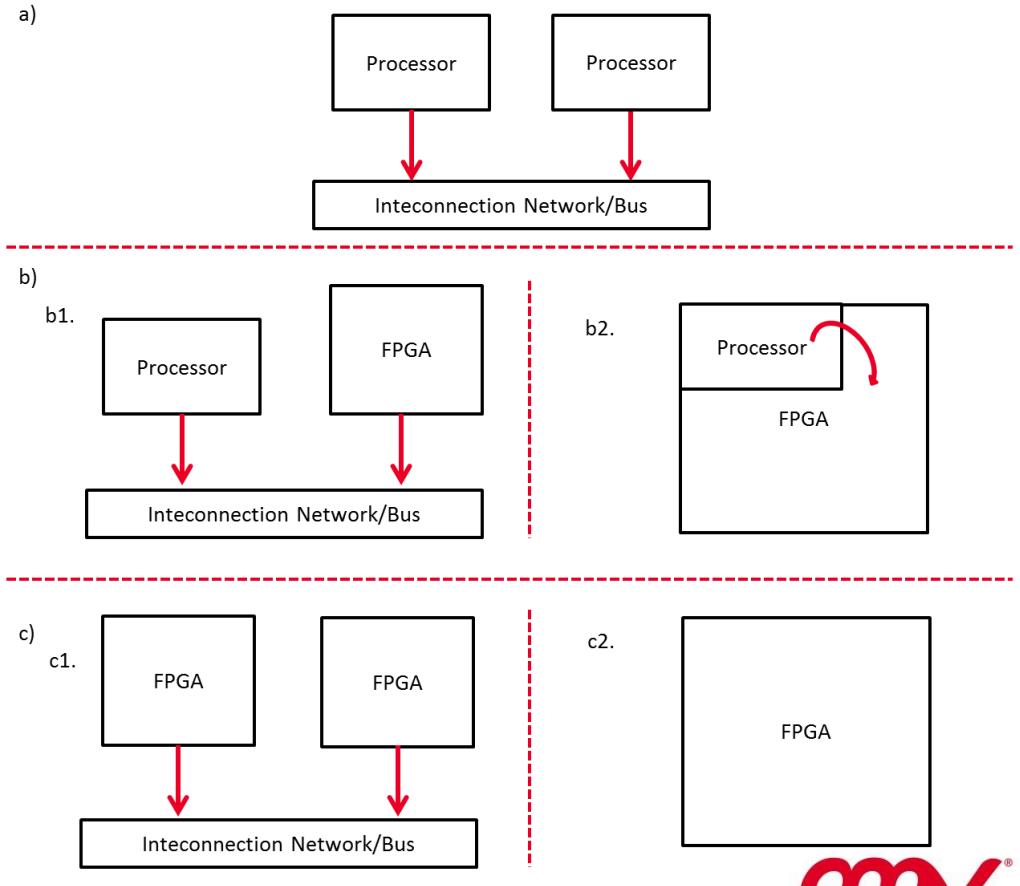
FPGA: solution between MCUs and ASICs

– The best of the two worlds:

off-the-shelf components (like MCUs) where to create own logic (like ASICs)

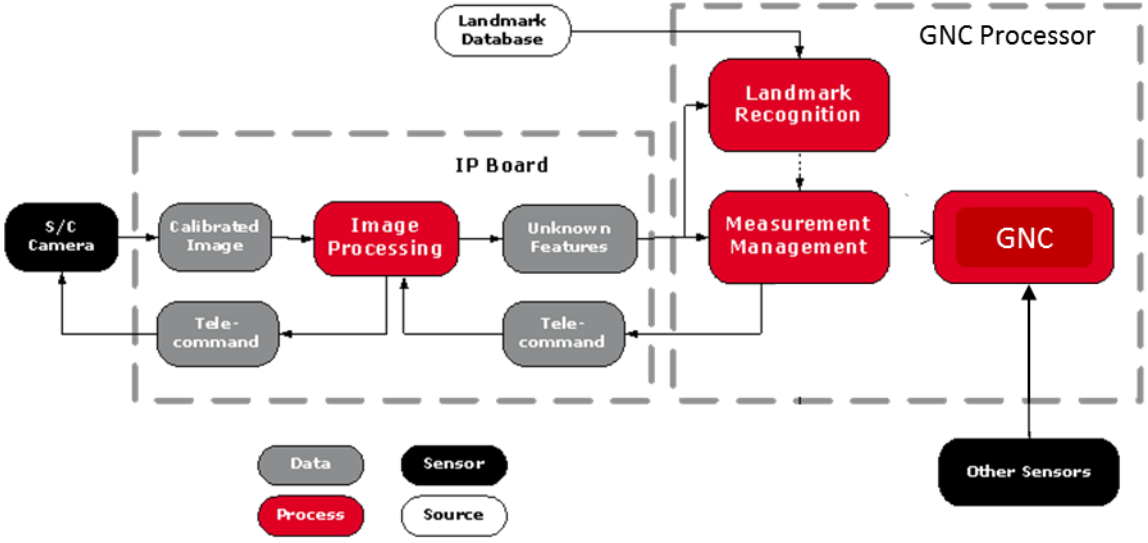
FPGA as accelerator co-processor

- A good alternative for creating SoCs
- Reduced synchronization
- Delays in communication



Vision-Based Navigation System

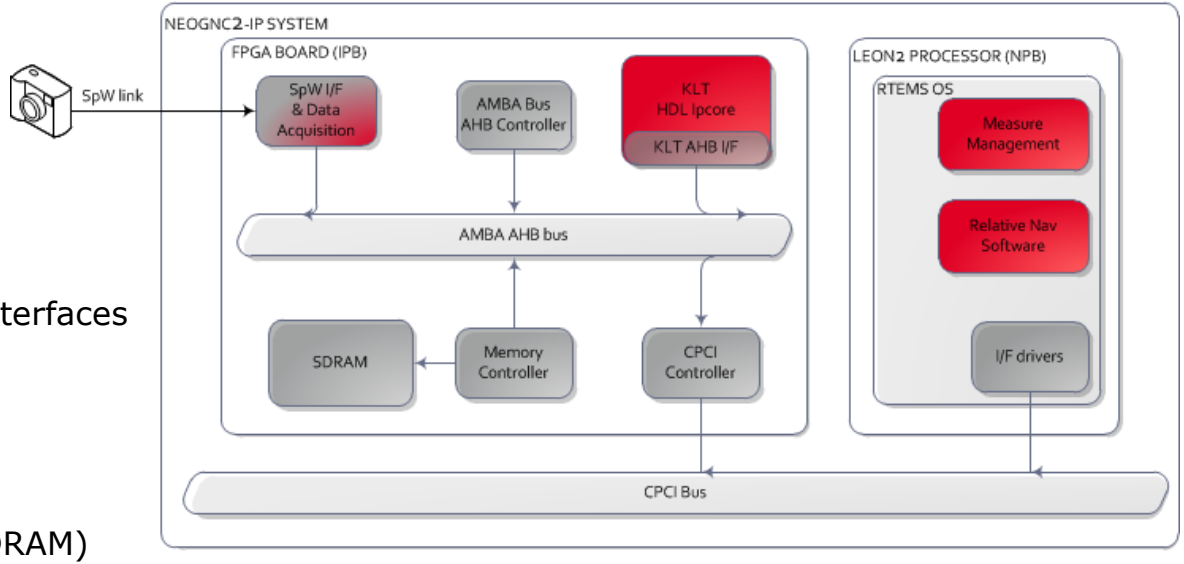
- IP algorithm implemented in VHDL into the FPGA as a co-processor. Embedded solution. Note: ECSS-Q-ST-60-02C
- VHDL Independent Technology, No high-level or autocoding tools.
- GNC implemented in C into Leon/PowerPC processor. RTOS (RTEMS / VxWorks)



FPGA Architecture

HW/SW architecture definition.

Implementation of Computer-Vision Algorithms as **VHDL IP-core blocks**
Absolute/Relative Navigation



Adaptation and Implementation of interfaces
- cPCI controller
- AMBA bus [AHB/APB]
- SpW I/Fs
- SDRAM controller
- IPcores AMBA I/Fs
- DataFlow Optimitation (SpW-AMBA-SDRAM)

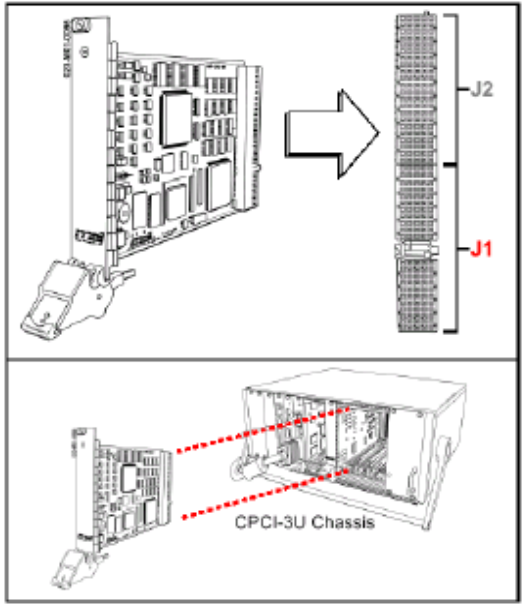
VHDL blocks based on the defined FPGA architecture

Integration of HW elements as the COTS IP-core to develope a System Environment for the Vision-Based GNC.

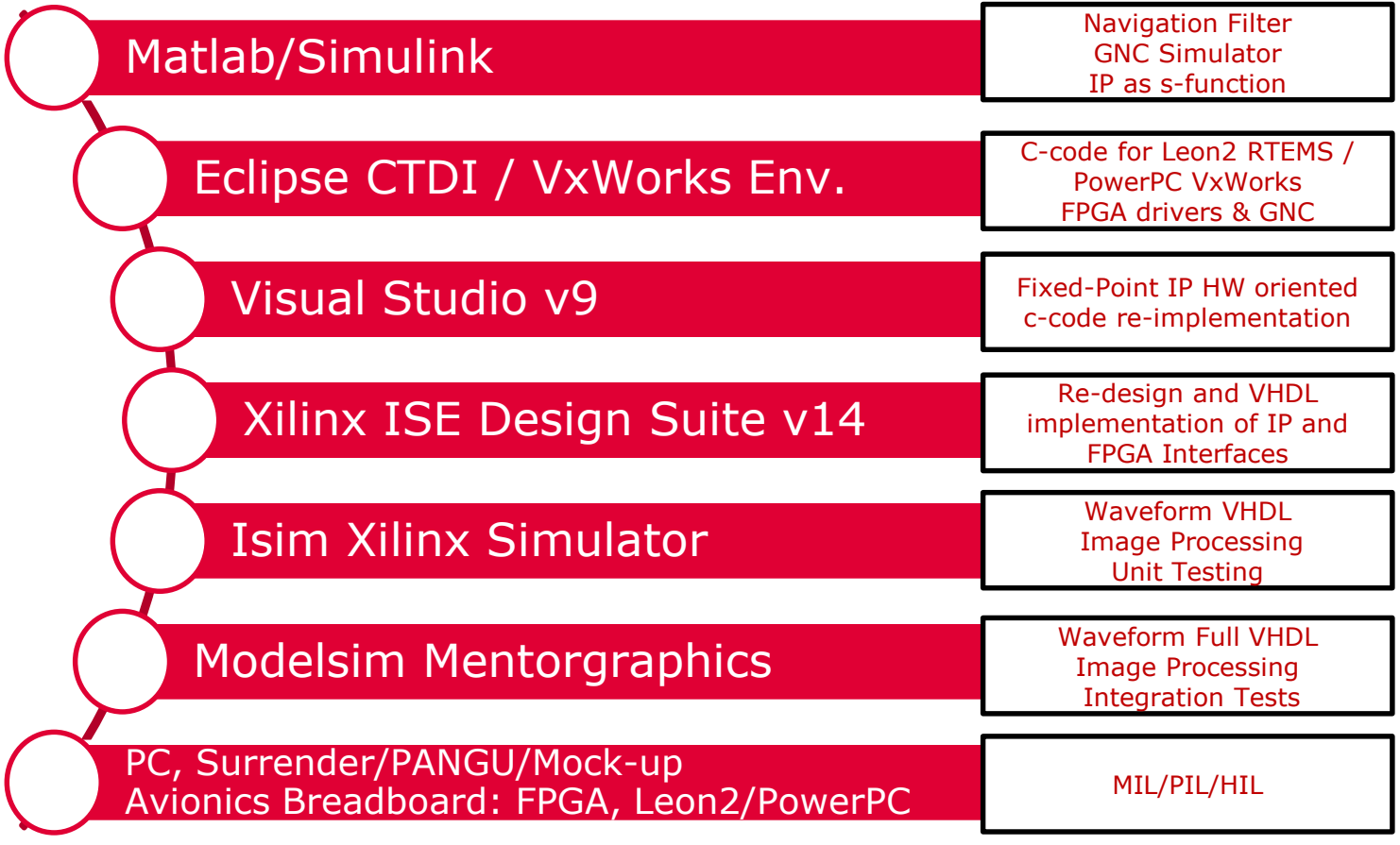
Selected FPGA

	LUTs	DSPs	BRAMs	DCMs	TID	SEL	I/O
Xilinx Virtex-4QV XQR4VLX200	178,176	96	6,048 Kb (400MHz)	12	300 krad(Si)	100 LET (MeV-cm2/mg)	960
Xilinx Virtex-4 XC4VLX200	178,176	96	6,048 Kb (500MHz)	12	N/A	N/A	960
Xilinx Virtex-4 XC4VLX100	98,304	96	4,320 Kb (400MHz)	12	N/A	N/A	960

- Re-usable / Scalable System through bus cPCI
- LVDS FPGA pins and mezzanine board for SpW physical connectors
- SO-DIMM socket for SDRAM/SRAM (256 MB external SDRAM)
- 98K to 178K LUTs
- 96 DSPs 18x18
- Gaisler Board encapsulation **GR-CPCI-XC4V**
- **Virtex4QV XQR4LX200 equivalent space-grade version**
  - Space-grade, radiation-tolerant Virtex-4QV FPGAs are based on commercial Virtex-4QV technology.
  - Manufactured on an UMC 90 nm copper CMOS process tech.
  - Size is 40x40 mm, package CF1509 / CN1509



Development Steps & Tools

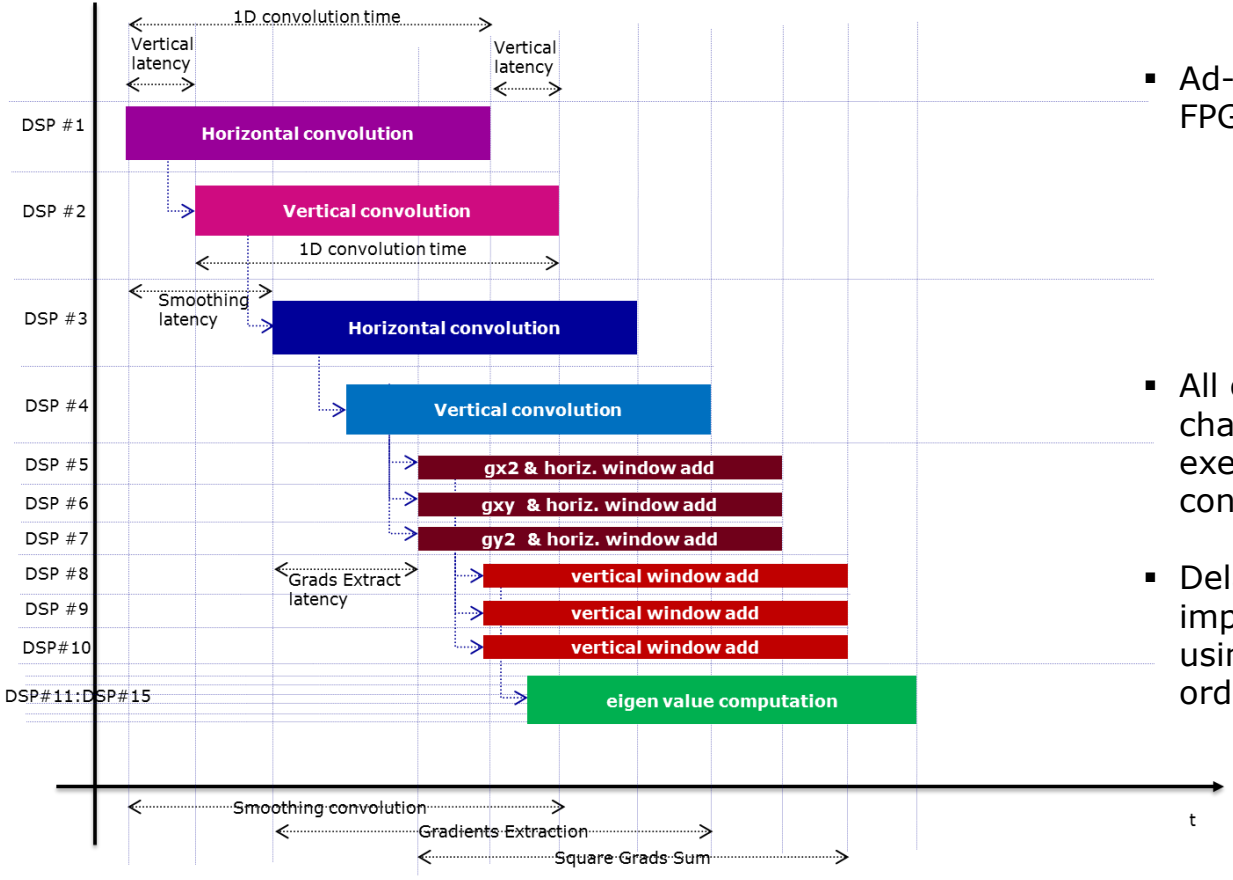


FPGA designing concepts

HW acceleration is provided by introducing key concepts of FPGA development advantages

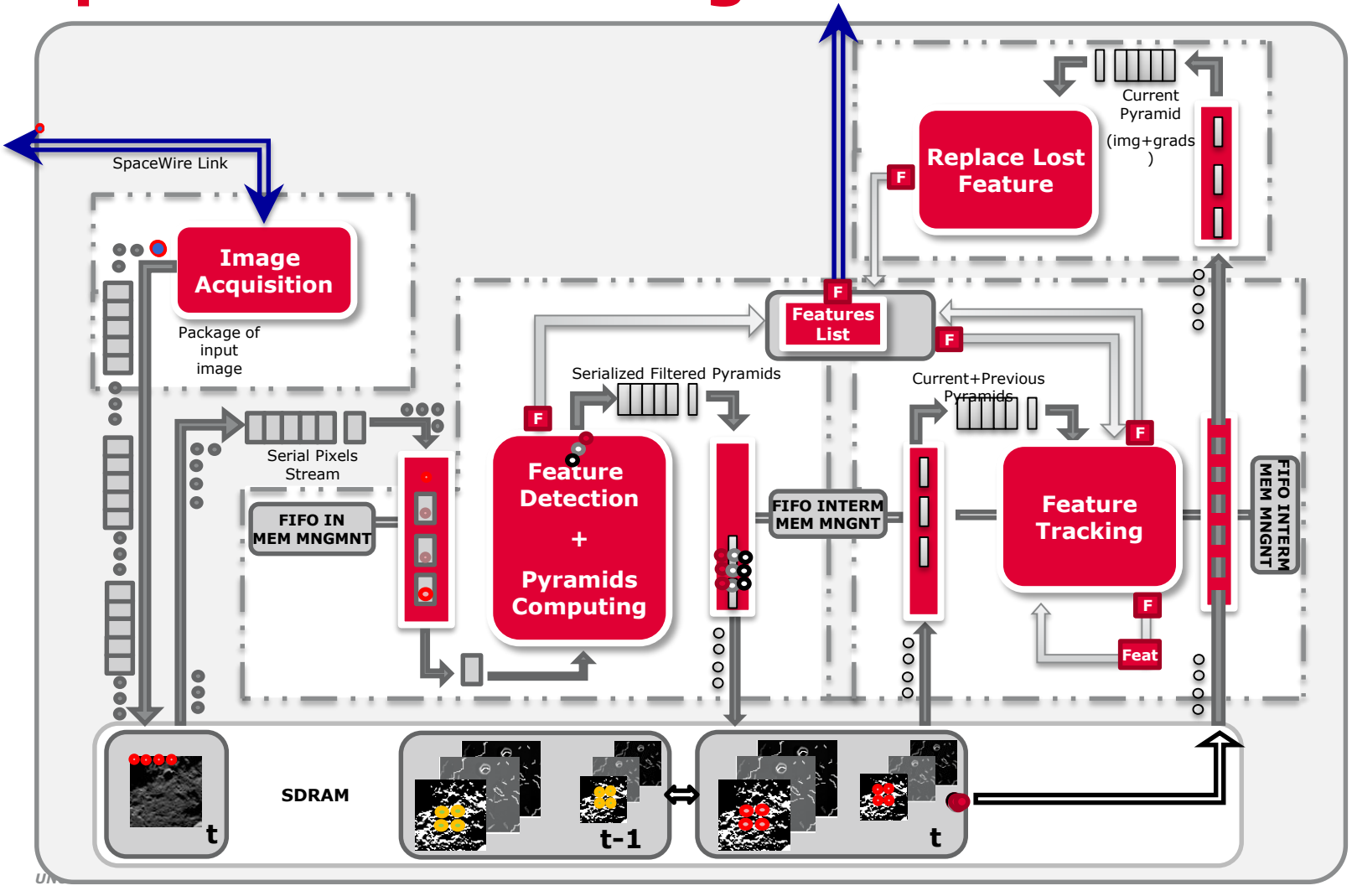
- Parallel Implementation
- Data streaming processing and Pipelining
- Avoid división/multiplication (take a lot of cycles) → shift
- Trees of comparisons
- Loops unrolling
- Multiply-accumulate (MAC)
- Specific HW (DSPs embedded into FPGA architecture)
- Convolutions separation
- Specific Memory Control
- Fixed-Point Arithmetic Operations (no FPU unless implementing one using logic area)
- Ad-hoc implementation of basic operations (No divisions, No square-roots unless user implement them)
- DCM design including different system clocks
- FPGA allocation and resource optimization → **Trade-off: AREA VS SPEED**
- FPGA embedded block RAMs design

Pipelining and Streaming processing



- Ad-Hoc multipliers using DSPs slices of FPGA to implement:
  - multiplications, square roots and MAC operations
  - accumulation or sums where speed is driven a design constraint
- All convolutions functions which are in chain are designed in pipeline and executed in parallel. Separable convolutions into 2stages 1D filtering
- Delays and memory banks are implemented as BRAMs instead of using FPGA logic as distributed RAM in order to save FPGA resources

Pipeline & Streaming Flow



FPGA verification and validation

Behavioural Simulation / Post-Synthesis Simulation / Post-P&R Simulation (FPGA **simulation is slow)**

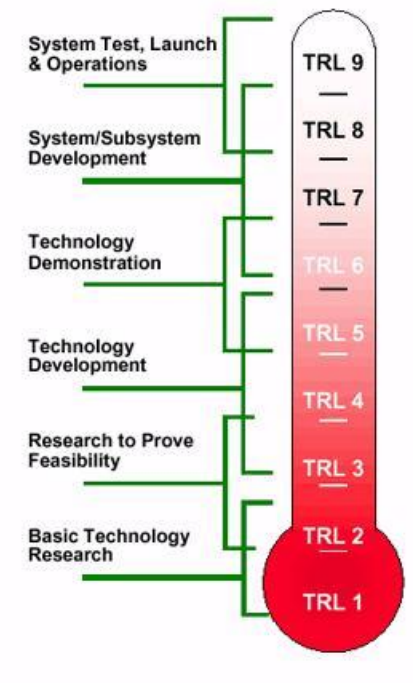
- Integration tests → TCL scripts to prepare VHDL batch testbenches and data for a subset of Descent and Landing trajectory (about 1000 images)

- Additional VHDL code to support collecting FPGA data to be sent to a Monitoring computer. (Waveform Simulation on-board). Breadboard output connected by means of a processor or PC to collect data using standard interfaces (ETH, RS232).

- Command Shell Console on top of the RTOS for debuging purposes

Validation of Algorithms:

- Comparison vs SW Models
- Comparison vs VHDL Simulation
- MIL tests using PC, dSPACE
- Optical Laboratory (dark room) for vision based algorithms
- PlatformART® HIL in simulated environment
- Outside test on-board of UAV / drone
- Aerostatic balloon
- Free fall from helicopter
- IOD – in orbit demonstration, cubesat, satellite



RelNav FPGA Performances & Resources

- Huge **Speed-up**, IP FPGA implementation takes <**300ms** including acquisition
  [Note: remember 80 seconds in Leon2 SW / 24 second in PPC750]
  - **acceleration of 267x (Leon2) / 90x (PPC750)**
  - SDRAM @ 133 MHz, aligned with AMBA bus to access memory @ 100MHz.
  - AMBA-AHB Burst mode internal data transmission instead of random access.
  - Writing of the input image (new_image) from SpaceWire to external SDRAM memory takes 50 ms (DMA)
  - Total amount of 15,6 MB of external RAM used for image processing data
- Processing Timeline: IP does not need feedback from GNC, then both task can be parallelized

Relative Navigation Breadboard XC4VLX200 FPGA Utilization Summary			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	37,418	89,088	42%
Number of Slice Flip Flops	22,462	178,176	13%
Number of 4 input LUTs	59,626	178,176	33%
Number of FIFO16/RAMB16s	96	336	29%
Number of GCLKs	2	32	6%
Number of DSP48s	57	96	59%

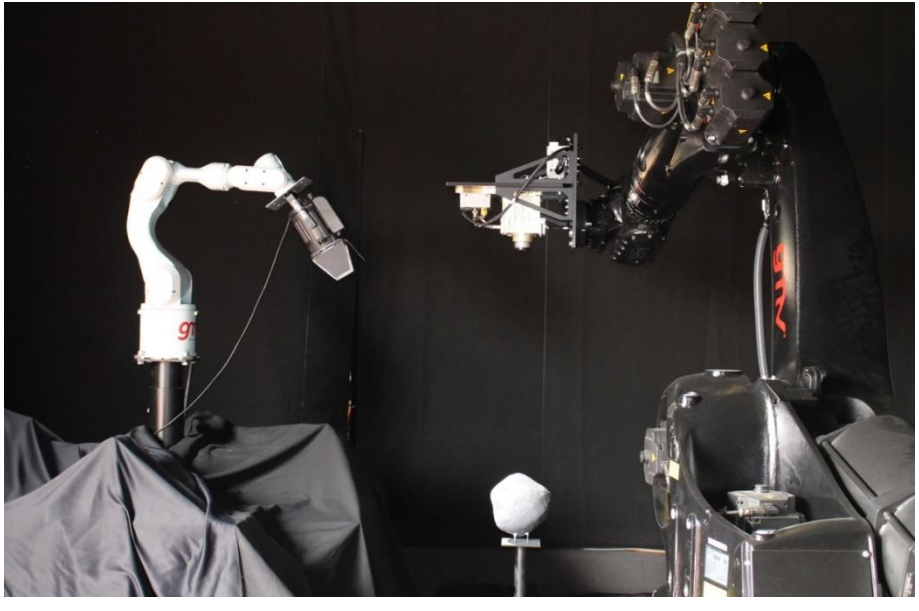
AbsNav FPGA Performances & Resources

- Edge Detector VHDL implementation takes 220 ms
  - **acceleration of 168x (PPC750)**
  - Same FPGA architecture as Relative Navigation System in terms of VHDL interfaces
  - Initially, Xilinx Spartan6 was targeted, with tight FPGA resources (mostly BRAMs)
    - Larger number of filtering coefficients to reach expected accuracy (more multipliers and BRAMs)
    - Virtex4vlx100 is then selected (reusability, available resources, space qualified version)

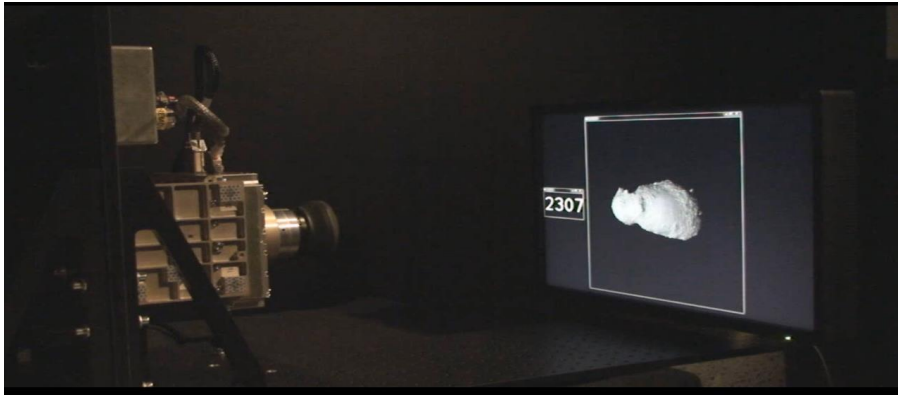
Absolute Navigation Breadboard XC4VLX100 FPGA Utilization Summary			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	10,324	49,152	21%
Number of Slice Flip Flops	11,505	98,304	11%
Number of 4 input LUTs	9,293	98,304	9%
Number of FIFO16/RAMB16s	183	240	76%
Number of GCLKs	1	32	3%
Number of DSP48s	54	96	56%

GNC & IP Validation

HW-in-the-loop in platform-ART® facilities

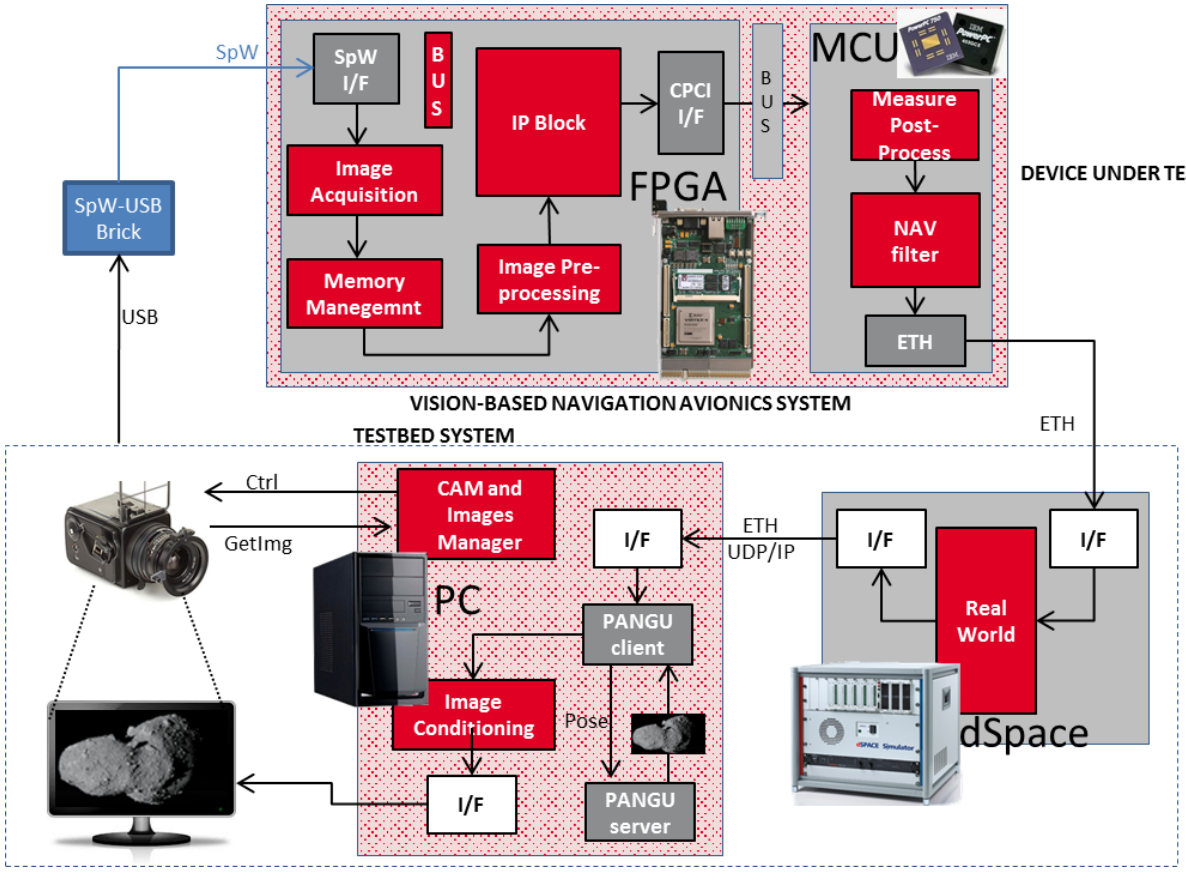


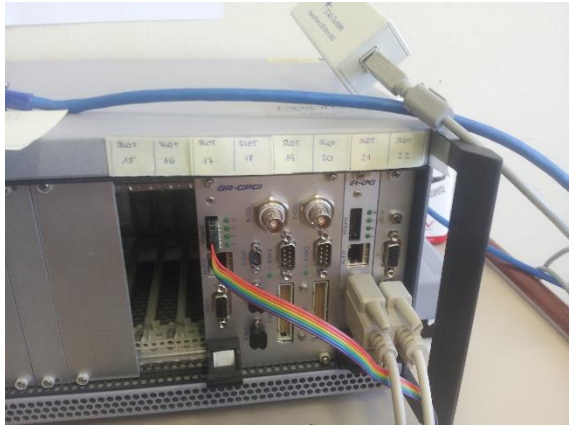
PIL/HIL in Optical Laboratory



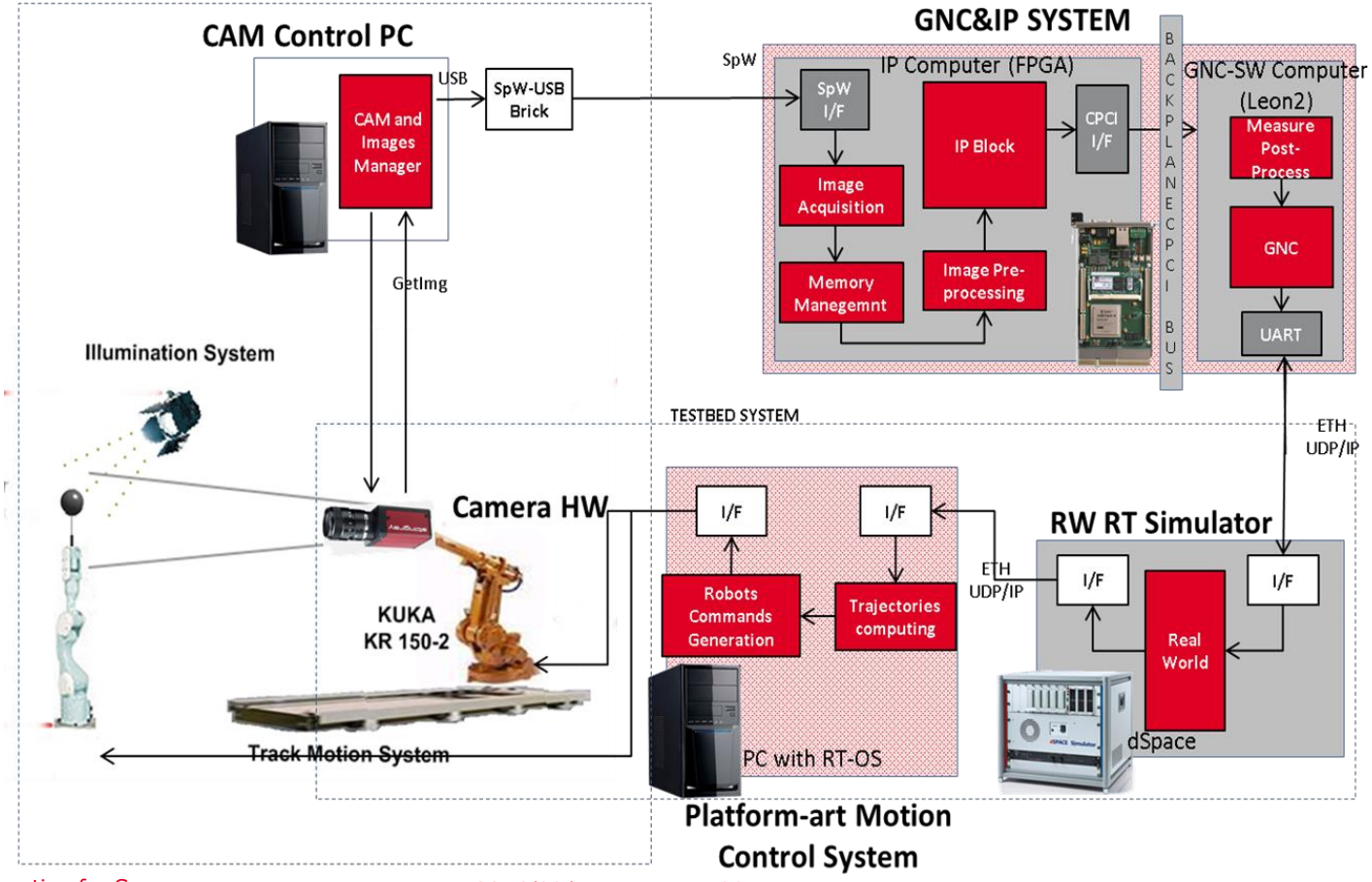
http://www.esa.int/spaceinvideos/Videos/2015/12/Testing_camera-based_navigation_software_for_asteroid_mission

Vision-Based Navigation Optical Lab Tests



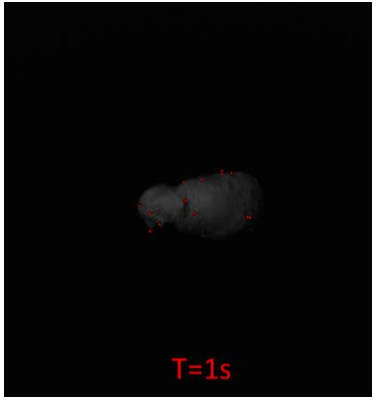


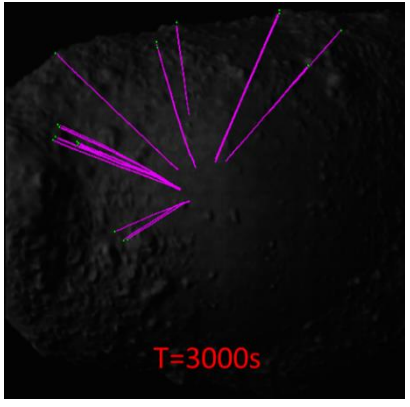
Vision-Based Navigation platform-art® tests

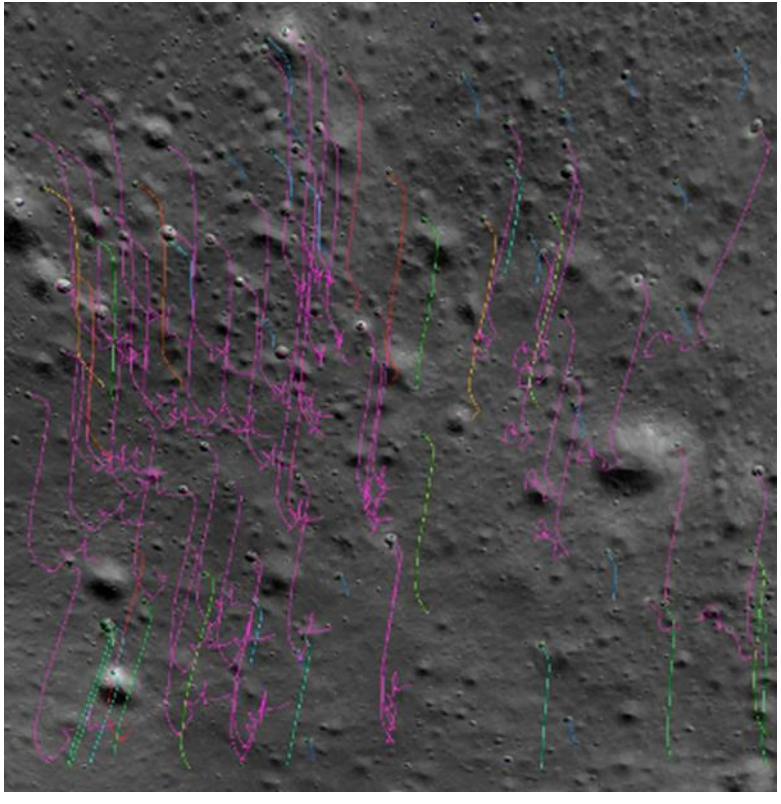


Results in Images/Videos

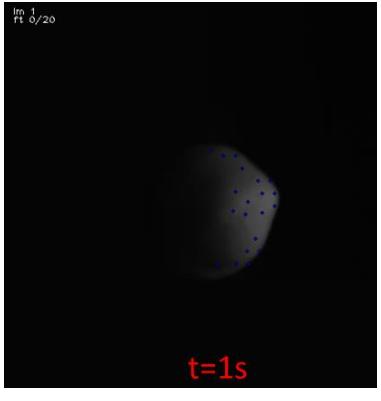
HIL in NEOGNC2-IP-NPAL Optical Laboratory (Itokawa)

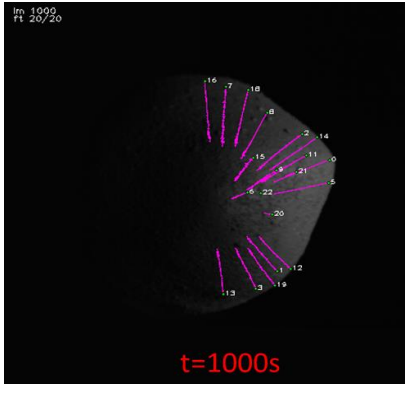






HIL in NEOGNC2-IP-NPAL platform-ART® (AIM)





Results in NEOGNC2-IP Phootprint Scenario

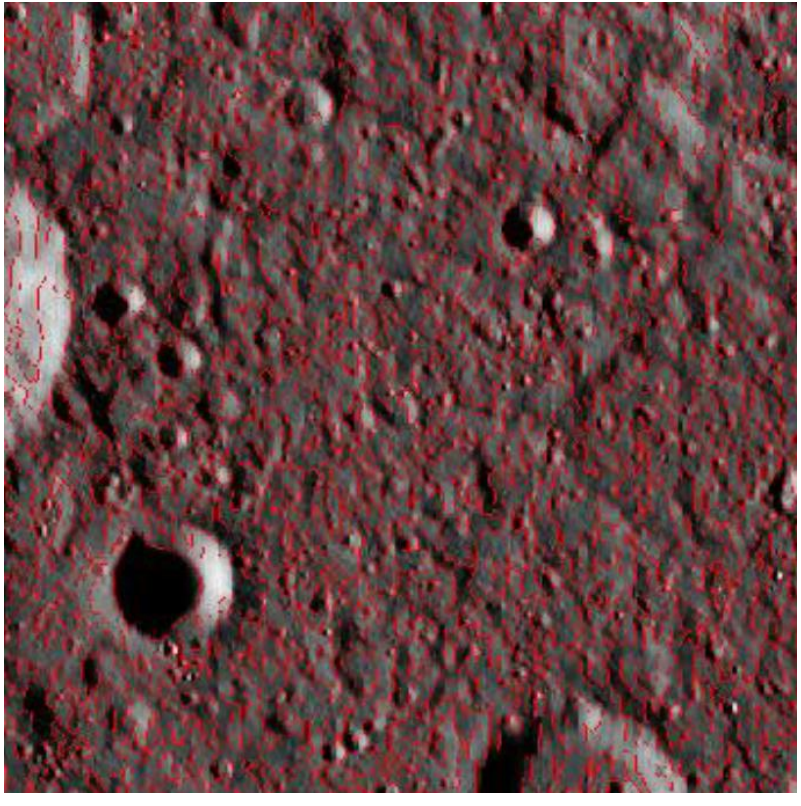
- **PHOOT-NOM-HILROB-1:** Single run results

Final Position Performances	HIL-ROB	SIL	SIL MC avg.	SIL MC sigma	SIL MC max	SIL MC min
Horizontal Position Error [m]	7.51	7.13	6.69	1.83	9.28	2.09
Vertical Velocity [cm/s]	122.4	133.1	118.41	10.41	141.41	99.51
Horizontal Velocity [cm/s]	6.3	6.0	5.86	0.58	7.06	4.64

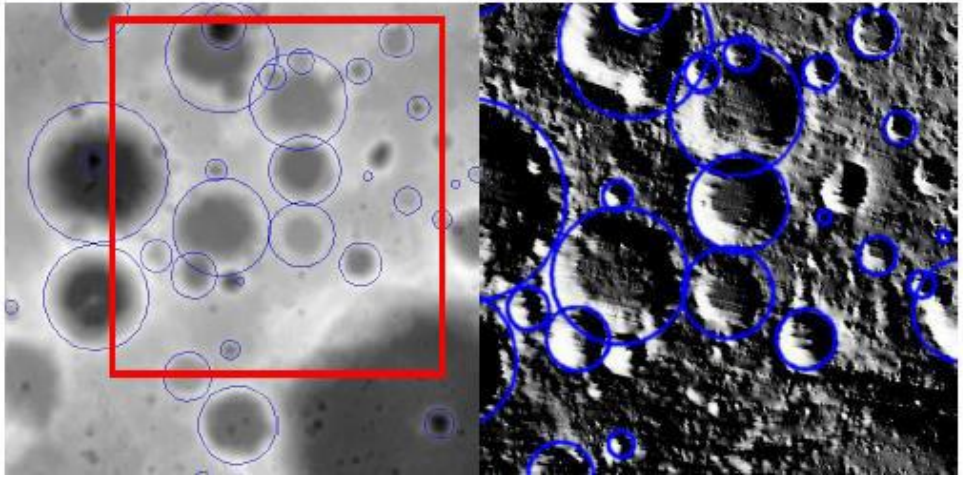
- **PHOOT-NOM-HILROB-2:** Single run results

Final Position Performances	HIL-ROB	SIL	SIL MC avg.	SIL MC sigma	SIL MC max	SIL MC min
Horizontal Position Error [m]	3.95	4.09	6.69	1.83	9.28	2.09
Vertical Velocity [cm/s]	101.2	105.5	118.41	10.41	141.41	99.51
Horizontal Velocity [cm/s]	9.0	8.9	5.86	0.58	7.06	4.64

Results in Images II



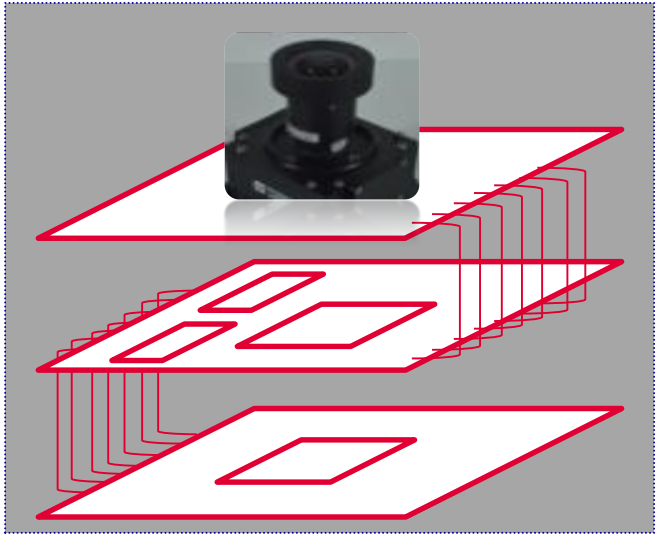
edge image obtained running FPGA implementation over moon surface images

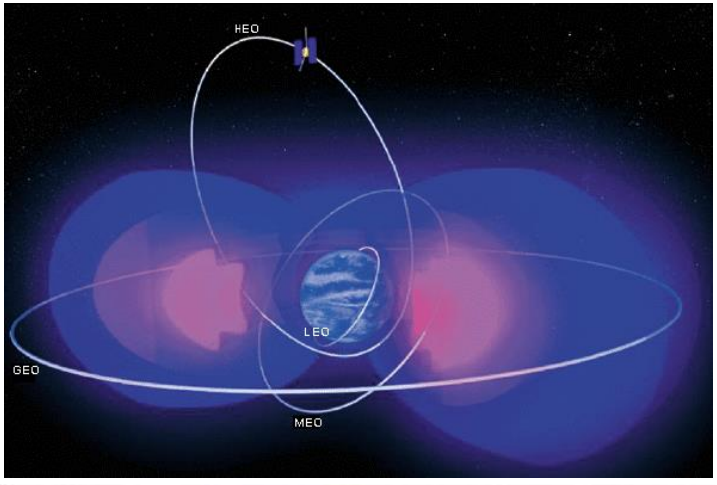


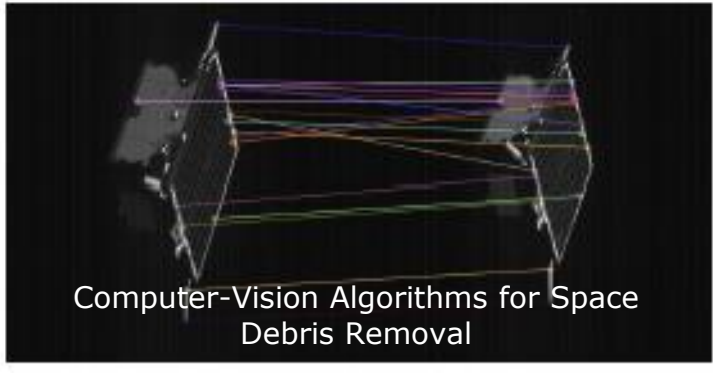
LRO DEM and identified craters (left), projection of the craters of DEM section using PANGU (right)

RoadMap

- FDIR
- Scrubbing memory (Leon/PPC)
- Margin of resources for TMR
- Moving to Virtex5QV, analysis of MultiFPGA
- Road to Flight Model → HW including camera detector
  → Navigation Camera Embedded/Clean Solution







- LEO orbits / soft radiation&lifetime missions
- COTS System-on-Chip
- In-Orbit Demonstration, Cubesats Experiments

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THANK YOU

Any question?

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