

# **Experience gained in Flash-based FPGA for InSight**

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*Stéphane Humbert / SYDERAL SA*

**GAIA PDHU**

(Mass Memory)



**EarthCare MMFU**

(Mass Memory)



**Insight SEIS-EBOX**

(Payload Controller)



# SYD-RAL

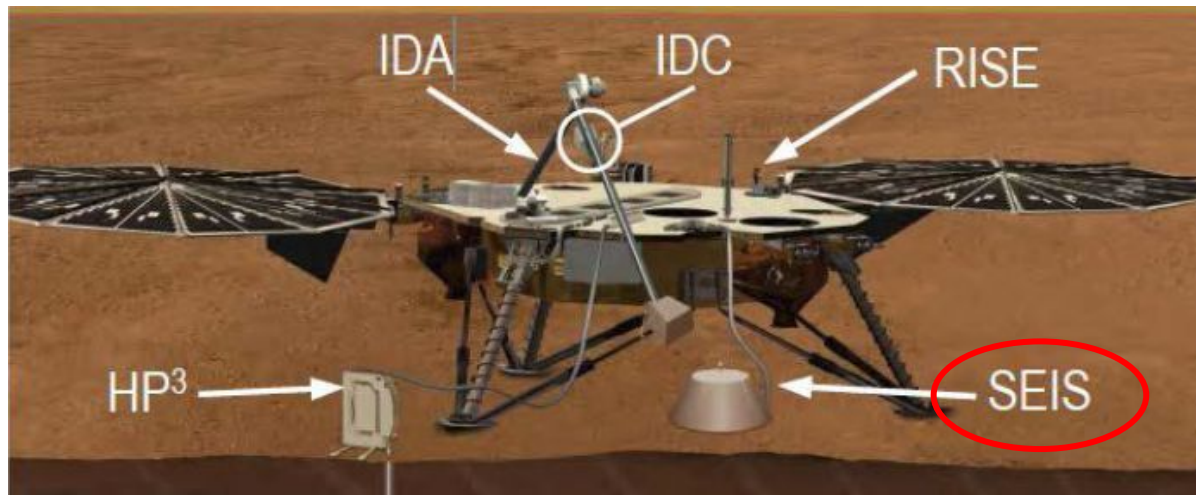
- ❖ **Introduction**
- ❖ **State of the art**
- ❖ **Constraints**
- ❖ **Solutions**
- ❖ **Results**
- ❖ **Conclusions**

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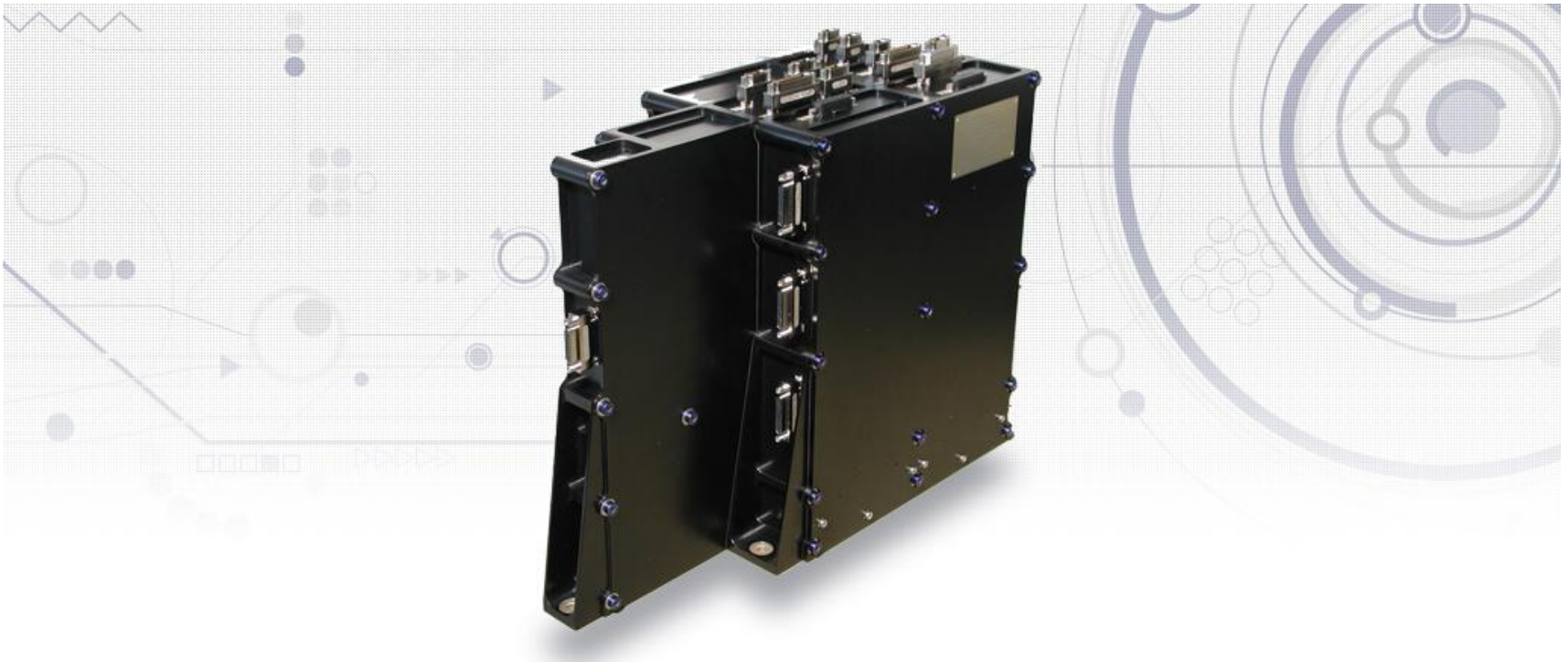
## Insight Mission

Interior exploration using Seismic Investigations,  
Geodesy and Heat Transport



## Seismometer Electronic Box (SEIS-Ebox)

The Seis E-Box (Seismometer Electronic Box) is located in the main lander and includes all functions needed to control the seismometer. The software, developed by CNES (National Centre for Space Research), is located in the main computer (Command and Data Handling (C&DH) unit).



## Two FPGA Designs:

### Acquisition FPGA

- Acquisition and sensor re-centring
- 10 scientific channels acquisition
- Scientific data filtering (programmable coefficients FIR filters)
- 3 VBB and 3 SP sensors velocity acquisition and control

### Controller FPGA

- TM/TC Low-speed serial interface
- Scientific data High-speed serial interface
- Flash Controller including bad block management

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### State of the art

#### Using Microsemi RTAX-S

- ★ Excellent space heritage and Syderal experience
- ★ Radiations hardened
- ★ Native Triple Module Redundancy (TMR) on all D-FlipFlop

#### Drawbacks

- ❖ Antifuse technology (OTP)
- ❖ Prototyping phase

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## Project main constraints

- Tight schedule from Requirement Review to Flight Model delivery
- Partner board integration
- Parallel development
- Potential changes identified

⇒ Need for a re-programmable FPGA ⇐  
as RTAX-S alternative  
with rollback plan

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## Re-programmable FPGA considered

**Xilinx (External SRAM configuration)**

**ATMEL (External PROM configuration)**

**Microsemi (Embedded Flash configuration)**

**⇒ Xilinx & Atmel reprogrammable FPGAs excluded due to:**

- Low heritage at Syderal for Space application**
- Performances / ressources not compliant to project needs**

**⇒ Microsemi RTProASIC3 selected for trade-off vs RTAX-S**

## Microsemi RTProASIC3

- ★ Design & use heritage at Syderal (ProASIC3)
- ★ Same design tools as for RTAX-S
- ★ Flash based configuration ⇒ Live at power-up
- ★ RT device uses same die as commercial one
  
- ❖ Reduced flight heritage vs RTAX-S
- ❖ No native rad-hardened Flip-Flops
- ❖ Lower radiation robustness wrt RTAX-S
- ❖ No re-programmable FPGA heritage for flight at Syderal

## Physical Aspects

Device	Actel ProASIC3 <b>RT3PE3000L</b>	Actel Axcelerator <b>RTAX 2000SL</b>
Config Memory	Internal Flash	N/A (Anti-fuse)
Package	CQ 256 <b>CG 484 (23mm<sup>2</sup>)</b> CG 896	CQ 352 <b>CG 624 (32.5mm<sup>2</sup>)</b>
User I/O count	166 (CQ 256) <b>341 (CG 484)</b> 620 (CG 896)	198 (CQ 352) <b>418 (CG 624)</b>

## Radiations Aspects

Device	Actel ProASIC3 <b>RT3PE3000L</b>	Actel Axcelerator <b>RTAX 2000SL</b>
Total Dose	>58.5kRad	>300kRad
SEL Immunity	> <b>68</b> MeVcm <sup>2</sup> /mg	> <b>117</b> MeVcm <sup>2</sup> /mg
Qualification Level	MIL-STD-883 Class E (Extended flow)	MIL-STD-883 class V QML Class V qualified
Native TMR (Triple module redundancy)	<b>No</b> <b>Radiation mitigation required to meet specs</b>	Yes. All instantiated flip-flops embed native TMR.



## Performances & Resources

Device	Actel ProASIC3 RT3PE3000L	Actel Axcelerator RTAX 2000SL
Speed Compatibility	Yes (350MHz) but radiation mitigation has to be implemented so timing degradation foreseen.	Yes (350MHz) Embeds a native TMR.
Modules	75 264 Tiles 1 TMR DFF = 4 tiles. 12'544 Flip-flops 25'088 Combinatorials	10'752 R-cells 21'504 C-cells

⇒ RTProASIC3 device fits (RT3PE3000L-1CG484)

## Design/FPGA radiations mitigation

Of course standard design mitigation applies (EDAC, FSM encoding, ...)

But registers have to be protected

- What kind of mitigation scheme to implement ?
- At which development stage the mitigation has to be applied ?
- How to ensure mitigation has been well implemented ?
- Is the design behaviour still the same after TMR insertion ?

And what are the consequences due to TMR insertion ?

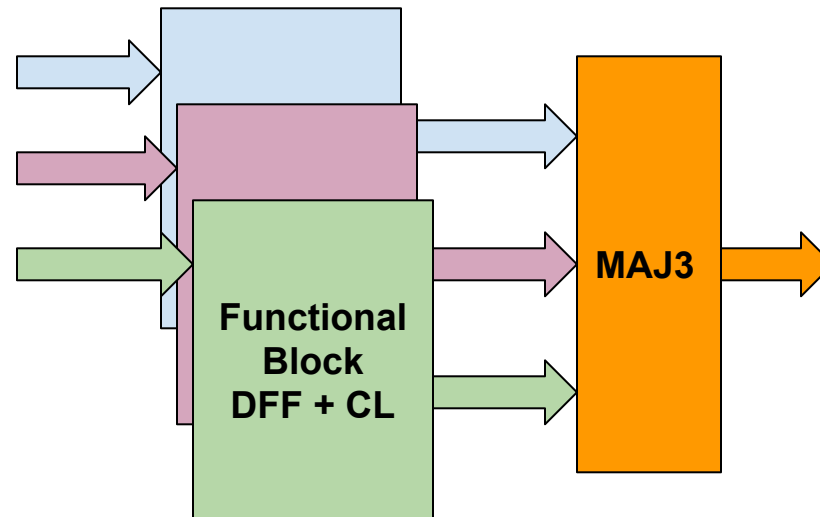
⇒ Reduced design performances

⇒ I/Os timings degradation

## What kind of mitigation scheme to implement and when to implement it ?

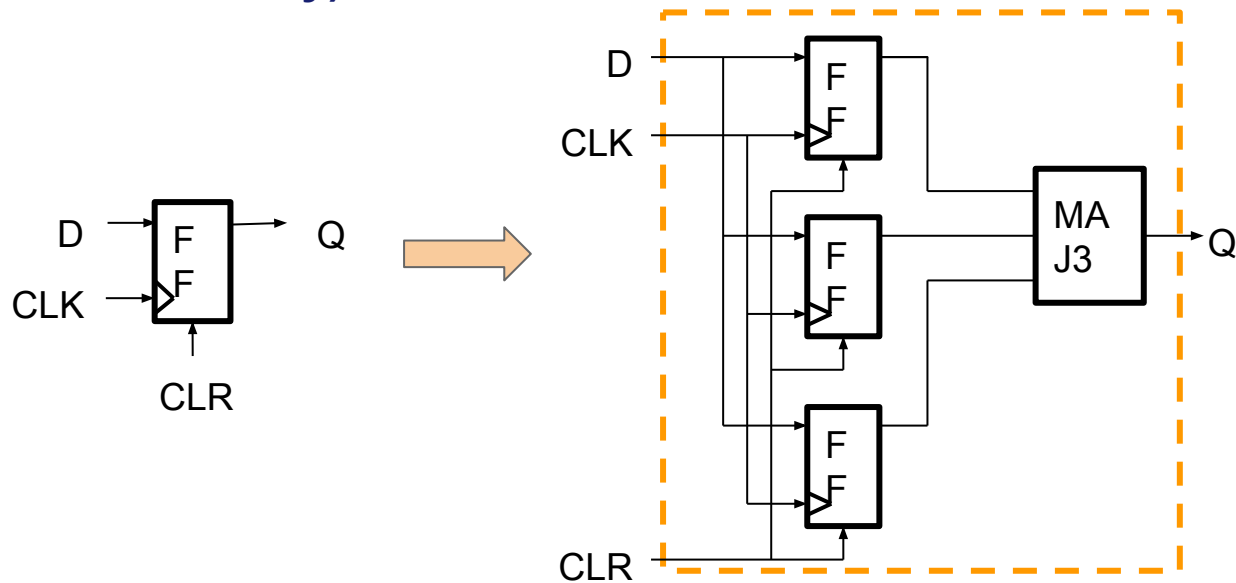
### A) Coding Phase (Block TMR)

Functional block (CC + FF) is triplicated as three black boxes; majority voters are placed at the outputs



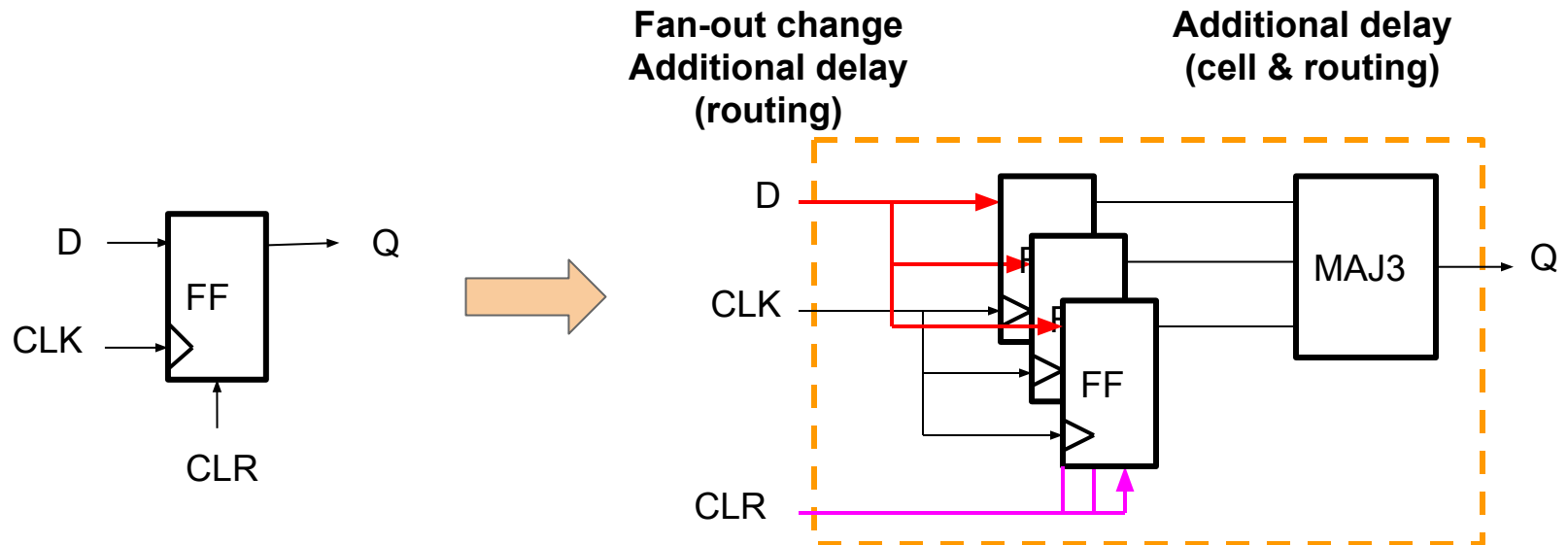
## What kind of mitigation scheme to implement and when to implement it ?

- B) Synthesis phase (Microsemi Recommended solution)**  
**Synthesizers supporting Microsemi RTProASIC3**
- Mentor Precision Synthesis (hi-rel) ⇒ Not available (ITAR)
  - Synopsys Synplify Pro ⇒ Provide automatic TMR insertion (Local TMR only)



## What kind of mitigation scheme to implement and when to implement it ?

- C) Post-synthesis (gate-level netlist)  
Custom tool to infer mitigation  
⇒ DRC violation & performances risks ⇒ Not acceptable



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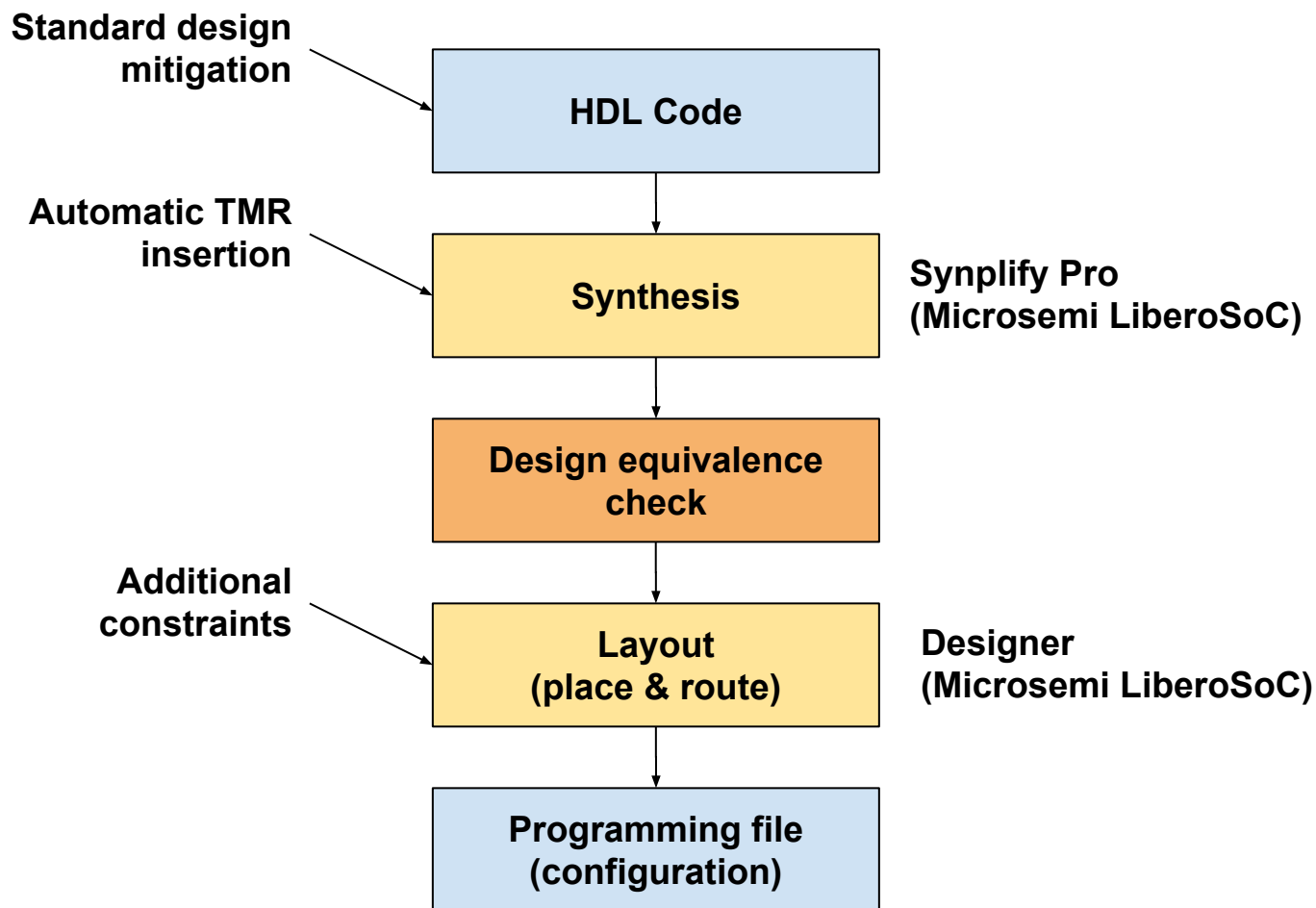
**Functional equivalence between RTL and gate-level has to be checked**

- **Equivalence checking**
- **Post-layout simulations**
- **Enhanced tests on HW**

**How to ensure mitigation has been well implemented ?**

**No solution identified at this stage ⇒ Rely on synthesizer tool**

## Selected solution





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## Implementations Results - Post-layout

	Non-TMR	TMR	Ratio
<b>Core Tiles</b>	32'348 43%	<b>60'392 80%</b>	x 1,87
<b>Combinatorial</b>	24'655	<b>37'676</b>	x 1,53
<b>Registers</b>	7'693	<b>22'716</b>	x 2,95
<b>Performance</b>	30 MHz	<b>22 MHz</b>	x 0,73
<b>Core Tiles</b>	35'104 47%	<b>66'077 88%</b>	x 1,88
<b>Combinatorial</b>	26'720	<b>41'371</b>	x 1,55
<b>Registers</b>	8'384	<b>24'699</b>	x 2,95
<b>Performance</b>	20 MHz	<b>17 MHz</b>	x 0,85

## Verification Aspects

### A) Functional Verification

As usual:

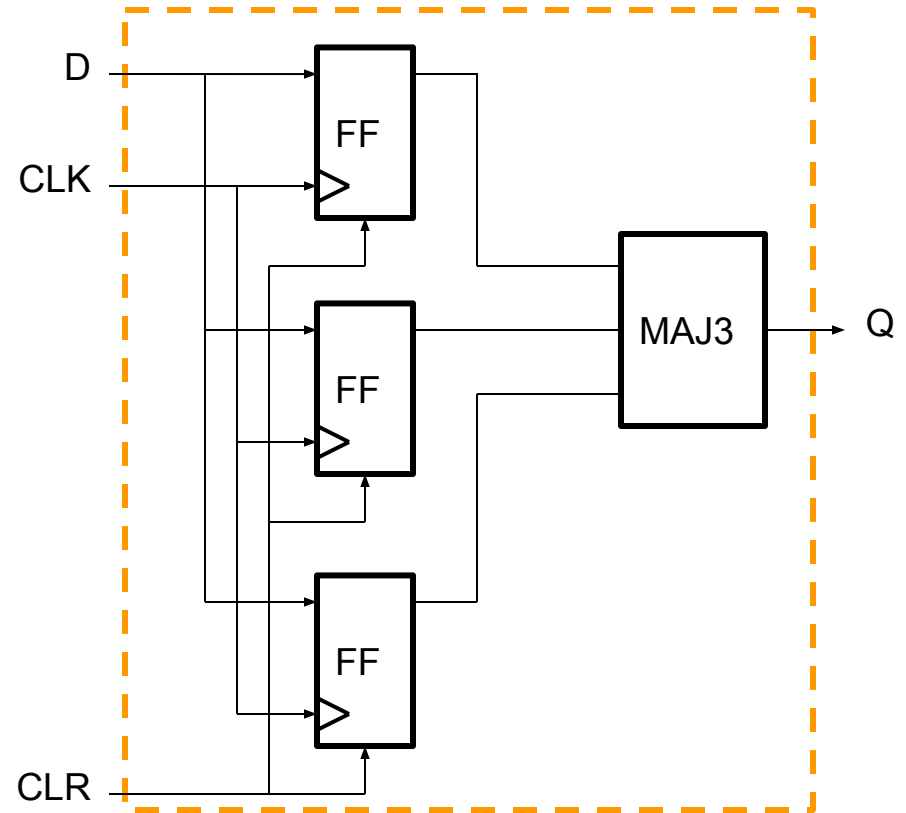
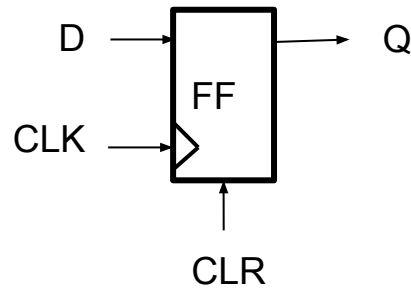
RTL Verification + Code Coverage  $\Rightarrow$  99.7%

Additional tests performed on breadboard

### B) Verifications required related to TMR

- Formal Verification (equivalence checking) by ESTEC
- Verified on post-synthesis netlist (gate level)
- Verification that TMR insertion has no functional impact  $\Rightarrow$  OK

Verification that TMR structure has been inserted for every flip-flop



A tool, *Steffi* (Synthesis TMR Examiner For Formal Inspection), has been produced by ETHZ to perform the TMR topology verification.



Verification performed on post-synthesis & post-layout netlist

The tool has shown TMR on flip-flops is implemented properly on both  
FPGA ⇒ TMR verification successful

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→ Conclusions (Insight SEIS Equipment)

- ◆ Equipment planning optimization possible
- ◆ Flight Equipment delivered on-time
- ◆ Late change & bug fix on Flight Equipment

⇒ FPGA Implementation Successful

- Conclusions using re-programmable FPGA
  - ◆ FPGA device flight representative from BB to FM
  - ◆ Risk reduction
  - ◆ Difficulties to stick to ECSS
  - ◆ Use of versioning system mandatory
  - ◆ Requires a strict database & programming files configuration



- Conclusions for future projects using re-programmable FPGAs
  - ◆ ECSS-Q-ST-60-02C update to take into account FPGA re-programmability aspects
  - ◆ Open the door to (very) late changes...

SYD-RAL

**Thanks for your attention**

Special thanks to Jan ten Pierick (ETHZ) for its support.

Any question ?