

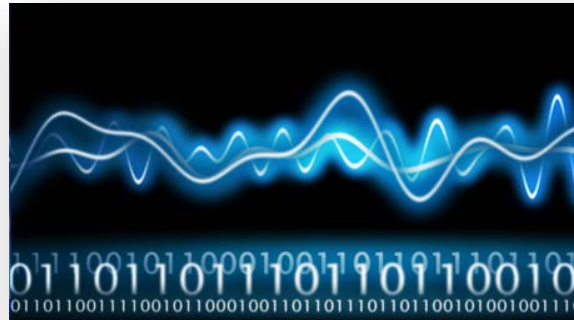
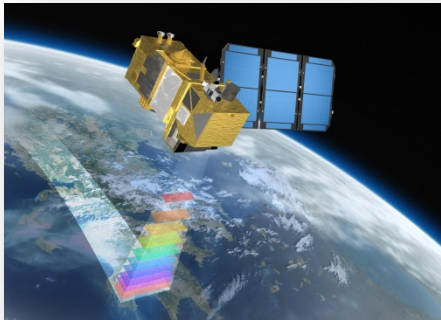


# RTG4 High-Speed RT FPGAs and Space System Managers

Ken O'Neill  
Director of Marketing, Space and Aviation

# Satellite Signal Processing Congestion

- Sensor resolution increasing faster than downlink bandwidth
- Satellites required to perform more on-board processing
- Requires high-density, high-performance payload processing electronics



## 1. Radiation-Hardened ASICs

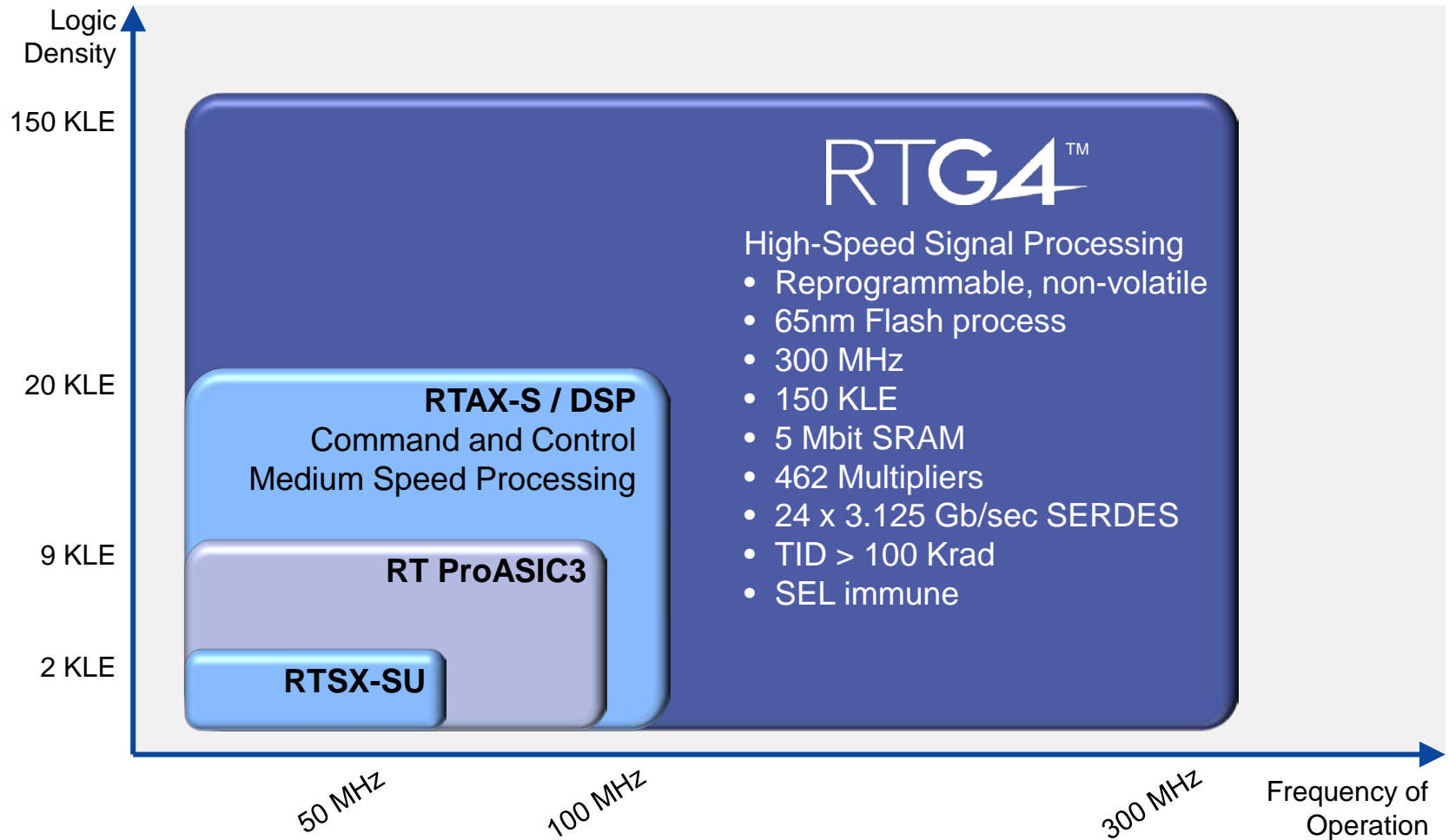
- ✓ High speed, high density, low power
- ✗ Large NRE, relatively low volumes
- ✗ Long development time, long fabrication cycle time
- ✗ High risk of schedule and cost over-runs

## 2. SRAM FPGAs

- ✓ Easy prototyping, reprogrammable
- ✗ Configuration SEU effects require cumbersome mitigation, increases Size, Weight and Power

***Existing solutions for satellite on-board processing have high risks***

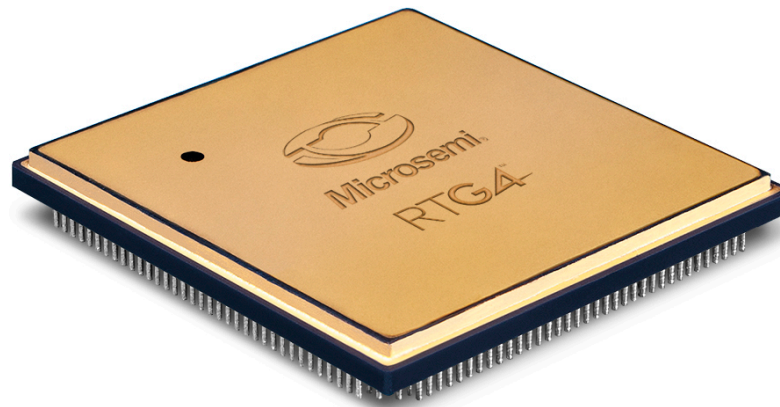
# Introducing RTG4 High-Speed RT FPGAs



***RTG4 mitigates risks of ASICs and SRAM FPGAs, and has 20X improvement in signal processing throughput***

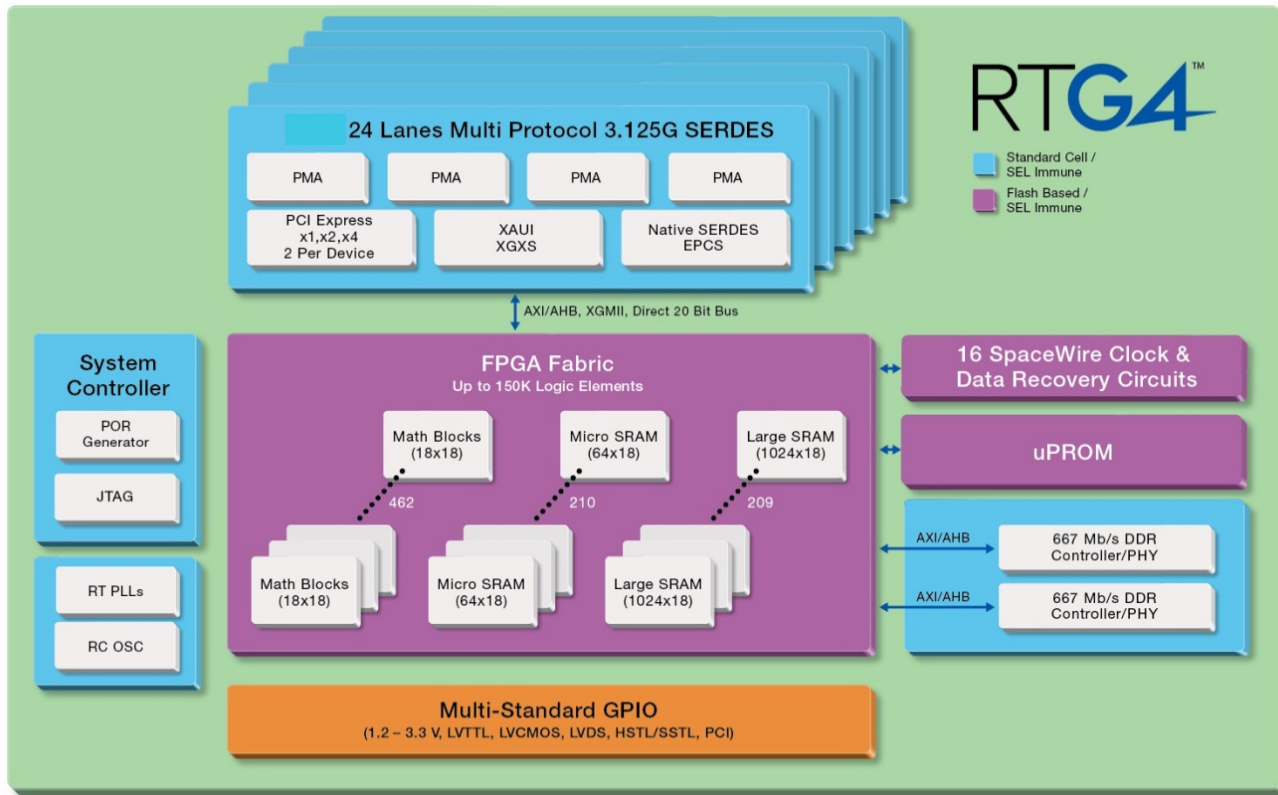
# Why RTG4 is Compelling

- More flexible than an RH ASIC
  - Reprogrammable, no NRE, no cost and schedule risk
- More signal-processing features than any other RT FPGA
  - More registers, combinatorial logic, multiply blocks, and transceivers
  - Lower power, live at power-up, no external boot memory needed
- Radiation enhanced for Geosynchronous Earth Orbit and deep space
  - RTG4 65nm Flash has complete immunity to configuration upsets (SEU)
  - Total ionizing dose (TID) and single event effects (SEE) hardened by design



***RTG4 offers groundbreaking features for satellite applications***

# RTG4 Radiation-Mitigated Architecture



- Total-dose hardening of Flash cells
- Single-event hardening of registers, SRAM, multipliers, PLLs

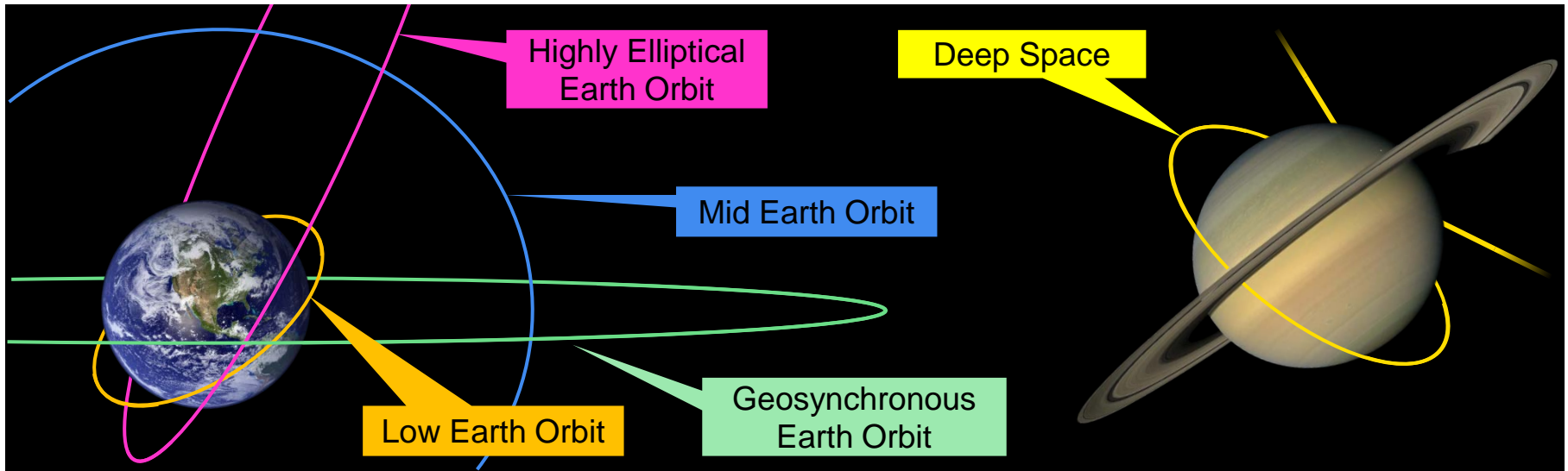
***Comprehensive radiation-mitigated architecture  
for signal processing applications***

# RTG4 Resources

Resources	RT4G150
Logic Elements (TMR Register + 4-Input C Logic)	151,824
18x18 Multiply-Accumulate Blocks	462
RAM Mbits (1.5 Kbit and 24 Kbit Blocks, with ECC)	5.2
UPROM Kbits	381
DDR2/3 SDRAM Controller (with ECC)	2x32
PCI Express Endpoints	2
Globals	24
PLLs (Rad Tolerant)	8
SpaceWire Clock & Data Recovery Circuits	16
User IO (excluding SERDES)	720
SERDES lanes (3.125 Gbit/sec)	24
<b>Hermetic, Ceramic Packages</b>	
CG1657 (Column Grid Array, Six Sigma Columns)	<b>Available Now</b>
CQ352 (Ceramic Quad Flat Pack)	TBD

# RTG4 Radiation Mitigation

- Total ionizing dose (TID) immune to > 125 kRAD
- Single event latch-up (SEL) and configuration upset (SEU) immune
  - Tested to 103 MeV-cm<sup>2</sup>/mg (facility limit) at 100°C
- SEU in FPGA flip-flops < 1x10<sup>-11</sup> errors/bit/day (GEO solar min)
- SEU in non-EDAC LSRAM < 4 x10<sup>-8</sup> errors/bit/day (GEO solar min)
  - No multi-bit upset (MBU) was observed
  - LSRAM with EDAC will be tested



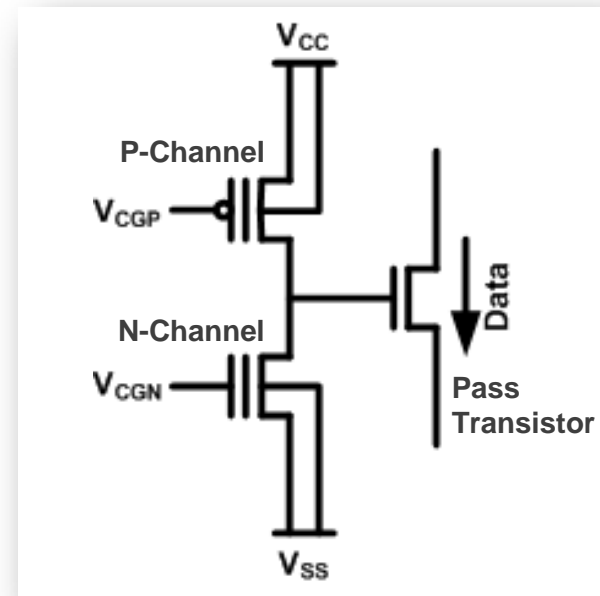
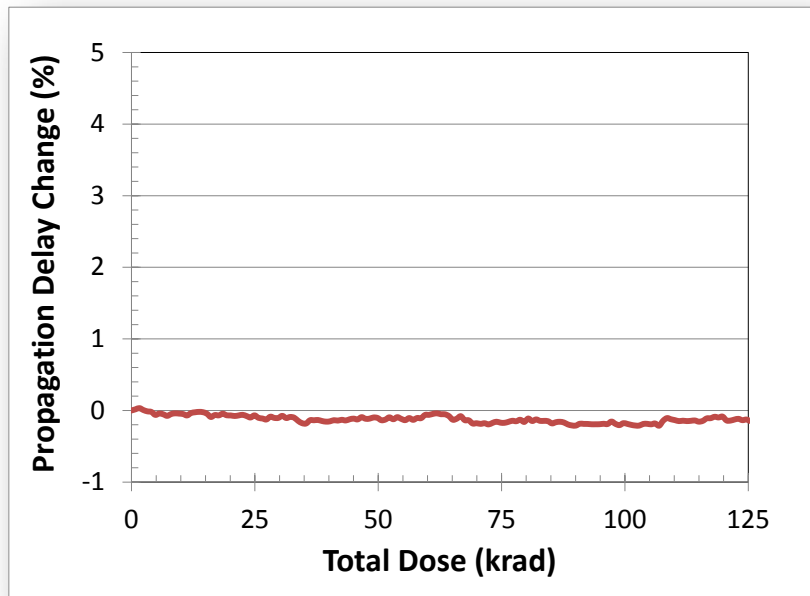
# RTG4 Radiation Updates

- [WP0191: Mitigation of Radiation Effects in RTG4 Radiation-Tolerant FPGAs](#)
- [Space Forum: RTG4 Radiation Test Results and Test Plans](#)
- Conference Papers:
  - [A Novel 65 nm Radiation Tolerant Flash Configuration Cell Used in RTG4 Field Programmable Gate Array](#)
    - This paper describes the flash cell used for RTG4 configuration and its impact on RTG4 TID performance beyond 100 Krad.
  - [TID and SEE characterization of Microsemi's 4th generation radiation tolerant RTG4 flash-based FPGA](#)
    - This paper includes RTG4 TID and SEE test results in heavy ion: configuration SEU, SEL, flip-flop SEU and LSRAM/uSRAM SEU
- In-orbit reconfiguration testing ongoing
  - Preliminary data shows parts can be reprogrammed successfully after being irradiated up to 106 Krad of heavy ion
  - High priority item for further radiation testing
- Planned SEE testing in 2016:
  - SEU: LSRAM/uSRAM with EDAC
  - SET: Fabric, DSP, clocks, SpaceWire, MSIO, MSIOD
  - SEFI: PLL, SERDES, PCIe, DDR controllers, System Controller

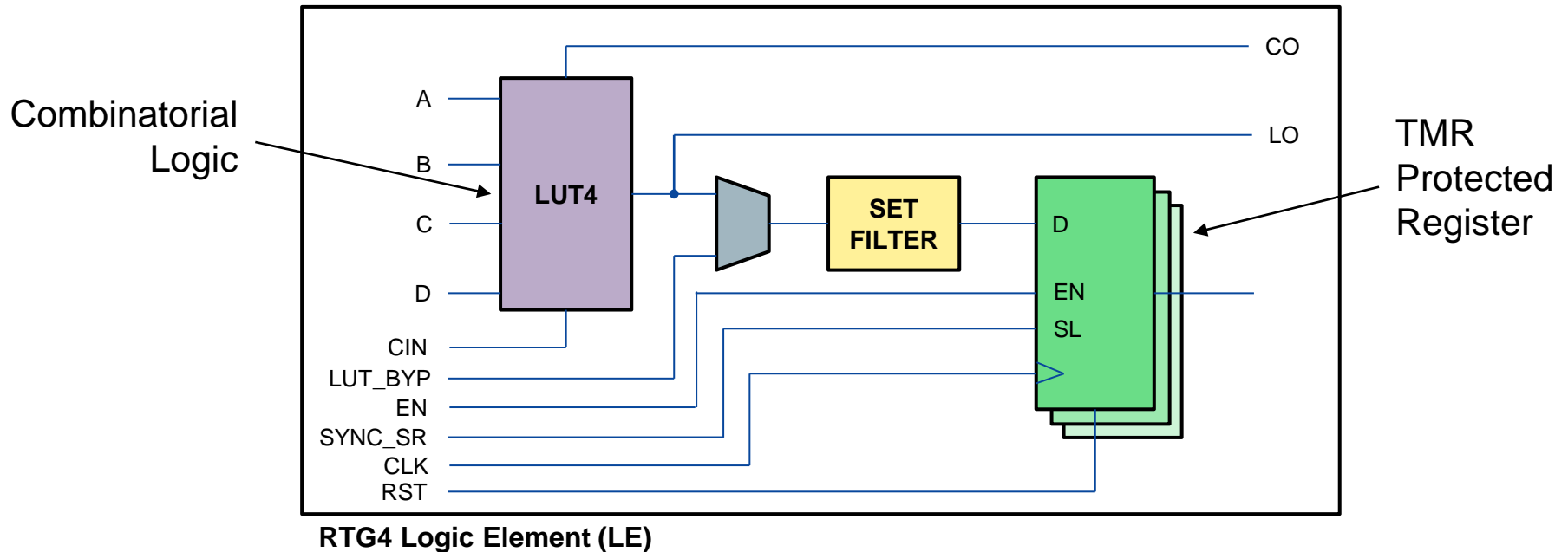


# TID Mitigation in RTG4 Flash FPGAs

- RTG4 TID-tolerant interconnect
  - RTG4 FPGAs functional after TID > 125 Krad
  - Change in propagation delay ~ 0% after TID > 125 Krad
  - Pass transistor is indirectly coupled to floating gate devices
  - $V_T$  changes in Flash cells don't change pass transistor prop. delay



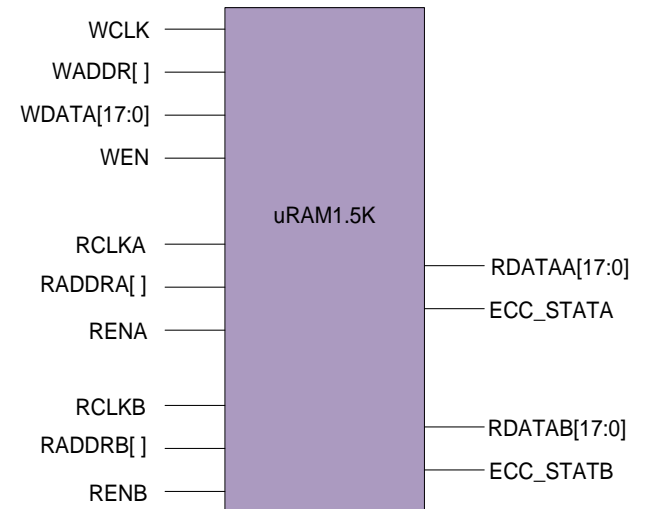
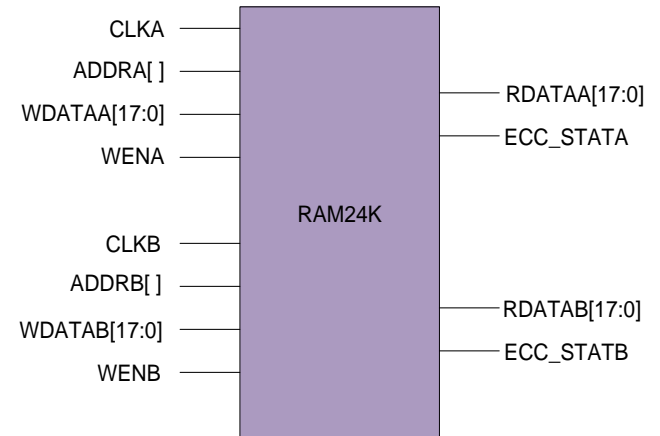
# RTG4 Logic Element Radiation Mitigation



- Dedicated register with efficient triple module redundant (TMR) hardening
- Single event transient (SET) filter mitigates radiation glitches from comb. logic
- Hierarchical routing architecture enables >95% module utilization

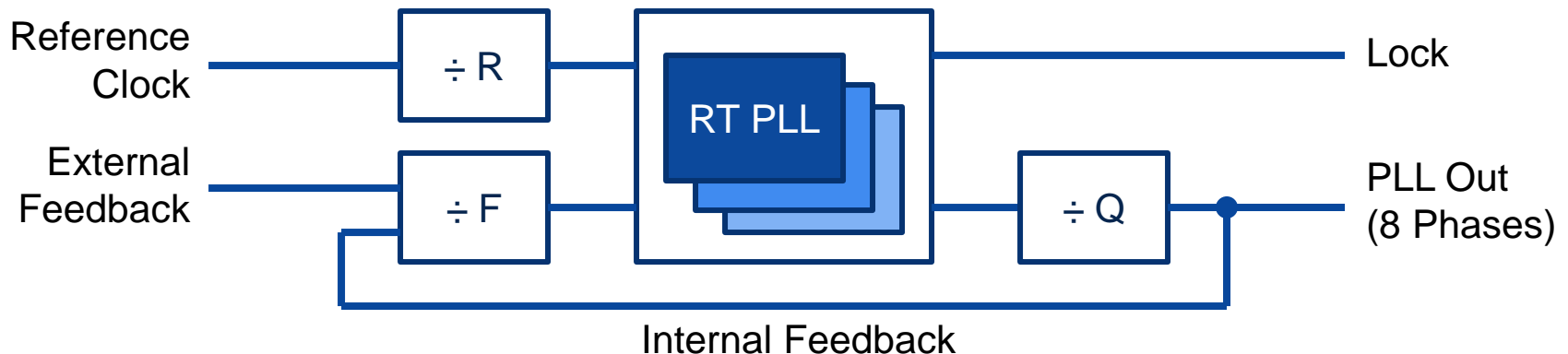
# RTG4 Memory Blocks

- Radiation Tolerant
  - Resistant to multi-bit upset
  - Built-in optional EDAC (SECDED)
- LSRAM – up to 24 KBit
  - Dual-port and two-port options
  - High performance synchronous operation
  - Example usage
    - Large FFT memory
- uRAM – up to 1.5 KBit
  - Three Port Memory
    - Synchronous Write Port
    - Two Asynchronous or Synchronous Read Ports
  - Example usage
    - Folded FIR filters and FFT twiddle factors

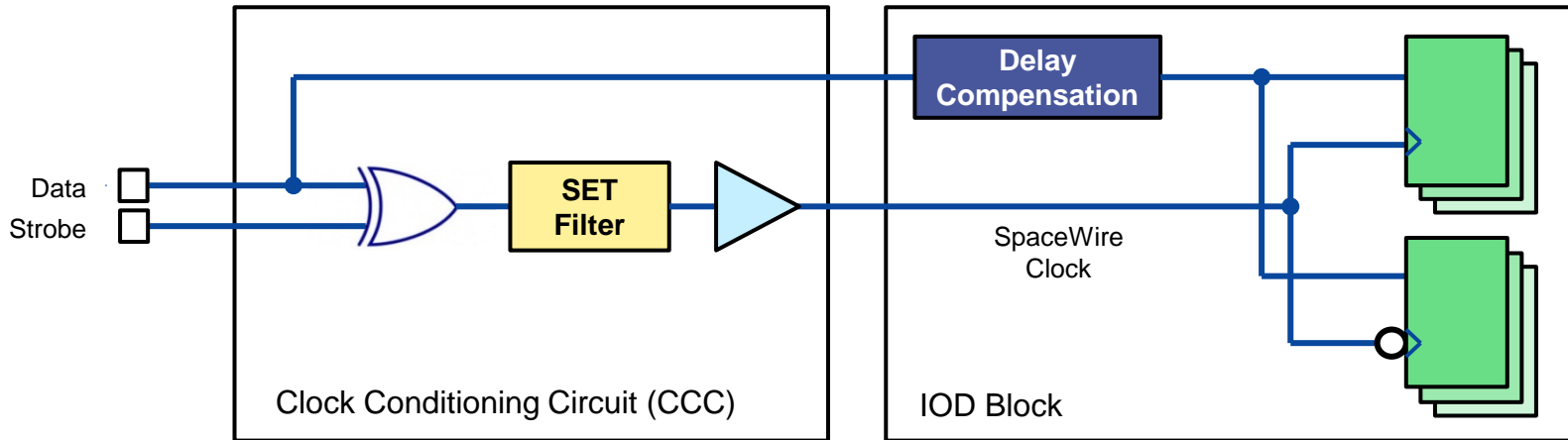


# RTG4 Radiation-Tolerant PLL

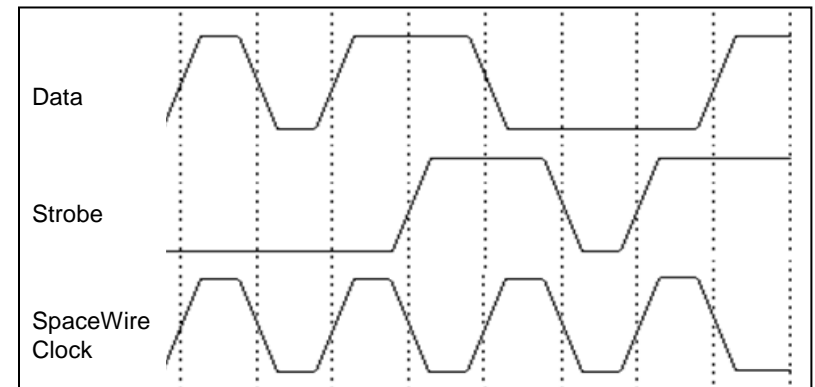
- Radiation-Tolerant PLLs are used in CCC, SERDES and DDR blocks
- Triple module redundant (TMR) PLL in internal feedback mode
  - Reference clock is fed back to all 3 sub-PLLs independently
  - Sub-PLL is SEL immune
- Single PLL in external feedback mode
  - PLL output travels through clock network and is fed back to PLL
  - Common mode used for clock network delay compensation
  - Only 1 sub-PLL is enabled in this mode
  - Sub-PLL is SEL immune



# Hardened SpaceWire Clock Recovery



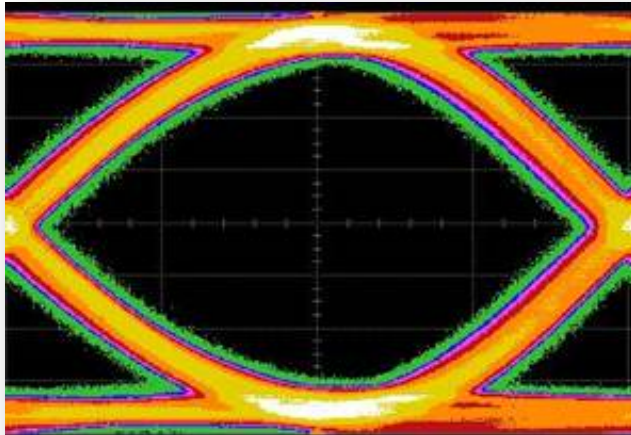
- SpaceWire interface used for command-and-control and data
  - Data and Strobe are XORed to recover SpaceWire clock
  - Hardwired and SET protected
  - Delay compensation available to align data and SpaceWire clock
  - 16 SpaceWire Clock Recovery circuits on each RTG4



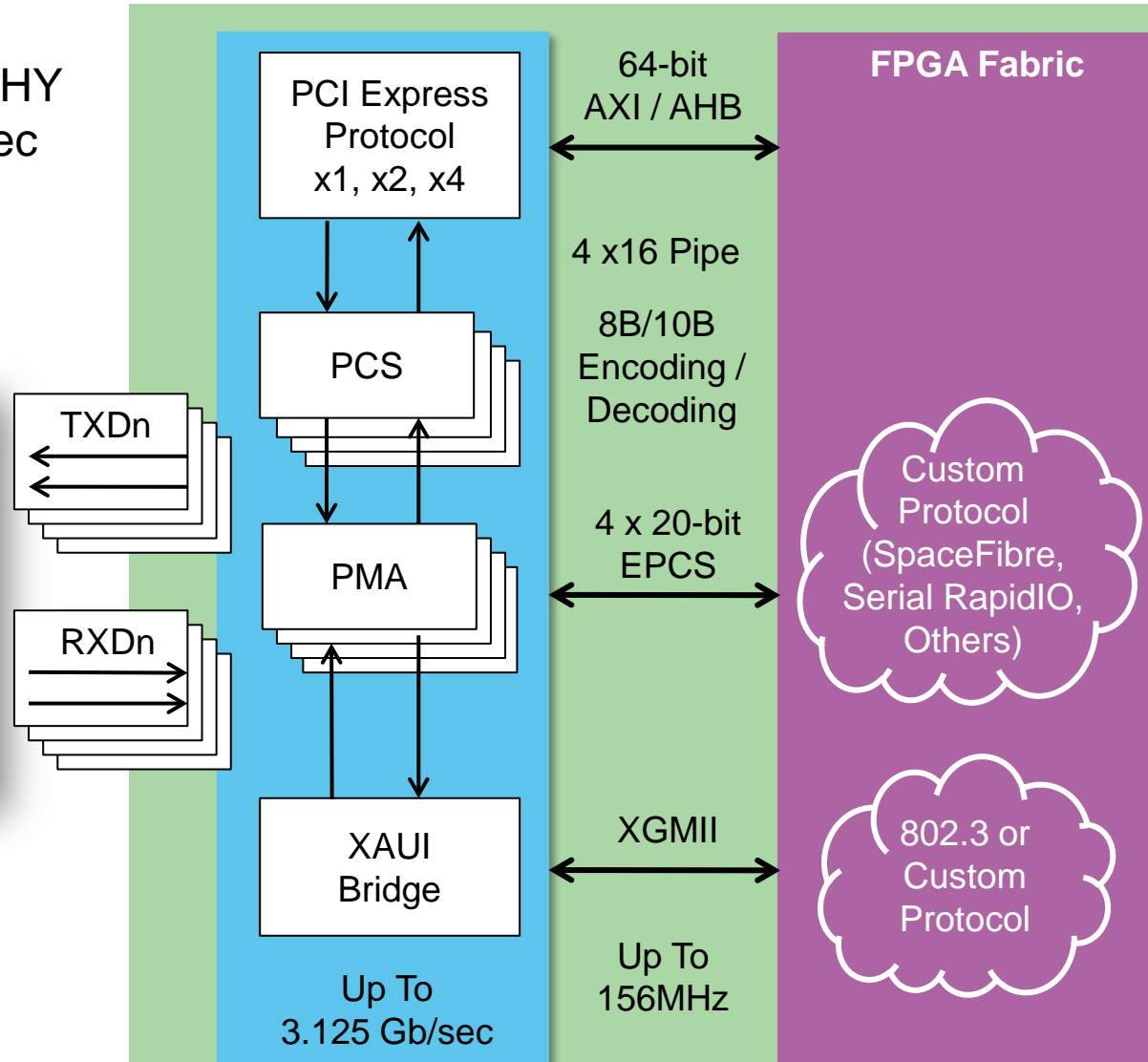
***Unique Microsemi RTG4 Feature  
See STAR Dundee SpaceWire Demo***

# 3.125 Gb/sec SERDES

PMA Based on PCIe Gen 1 PHY  
Performance 1 to 3.125 Gb/sec  
Up to 6 blocks with 4 lanes

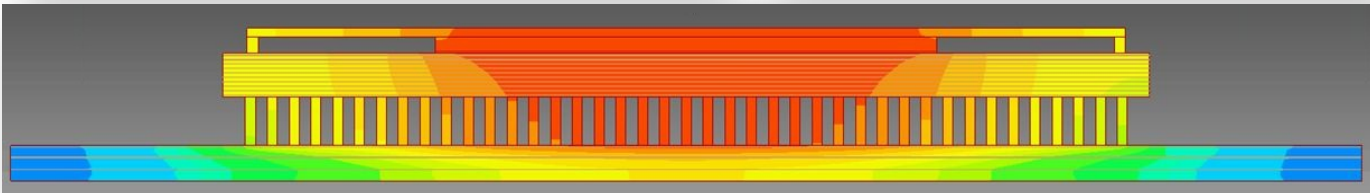
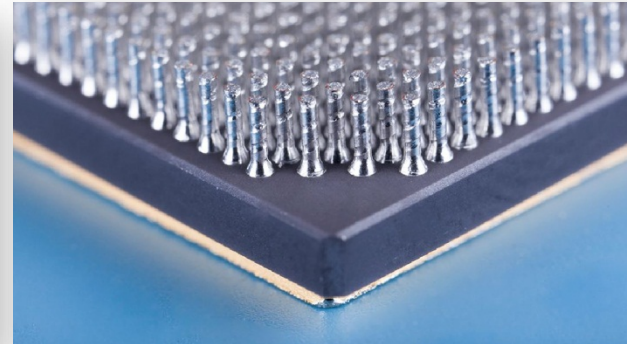
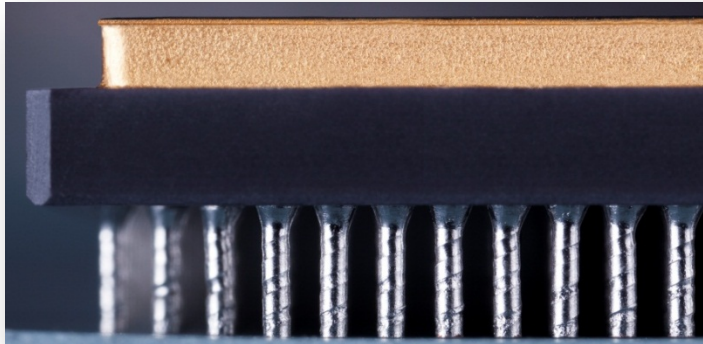
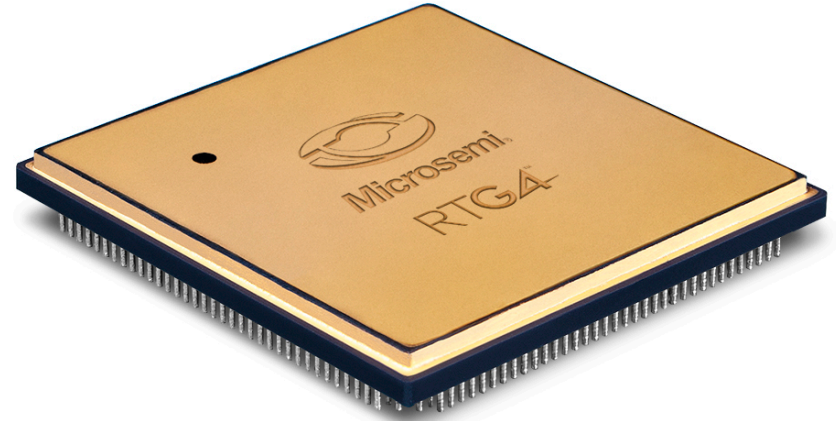


**See STAR Dundee  
SpaceFibre Demo**



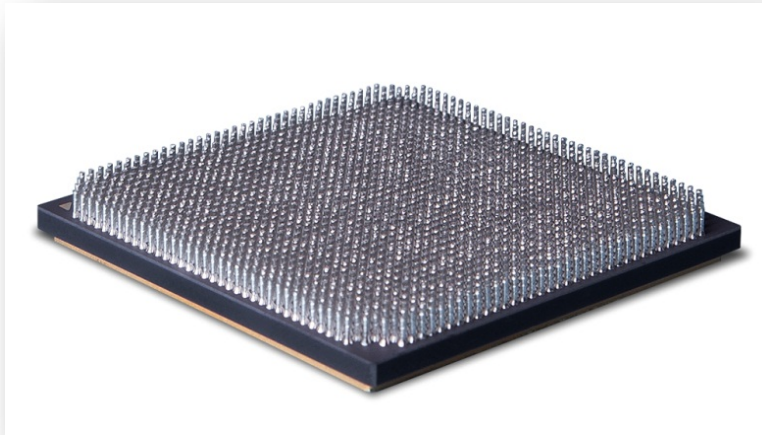
# RTG4 Packaging Update

- Hermetically sealed, ceramic packages
  - Embedded decoupling capacitors
    - Flight models will have PME (Precious Metal Electrode) capacitors (Presidio 0508)
  - Column Grid Array, Ball Grid Array, Land Grid Array, Ceramic Quad Flat Pack

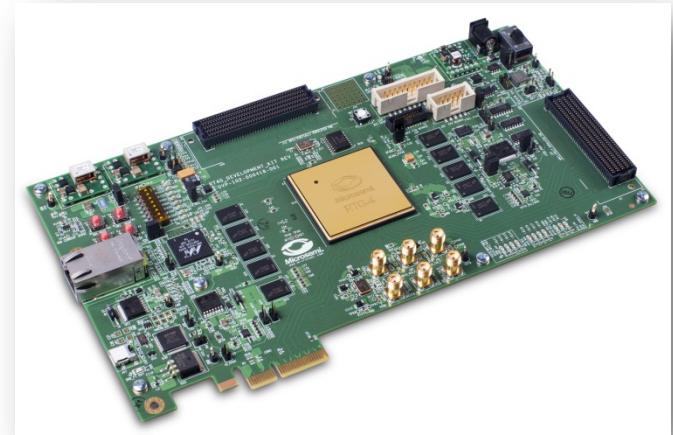


# RTG4 Availability, Qualification Schedule

- RTG4 devices for space flight applications
  - Engineering Silicon RT4G150 FPGAs: **NOW**
  - Libero SoC Design Software: **NOW**
  - RT4G150 development kit: **NOW**
  - Daisy chain packages: **NOW**
  - MIL-STD-883 class B flight units: September 2016
  - QML class Q qualification: Mid 2017
  - QML class V qualification: Early 2018



Ceramic Column Grid Array Package



RT4G150 Development Kit



# RTG4 Qualification Update

- **MIL-STD-883 Class B Qualification**
  - Completes in September 2016
  - Qualification will use RT4G150 in CG/LG1657 package
    - 3 wafer lots, 3 assembly lots
    - 1000 hours HTOL
  - Preliminary results:
    - HTOL: 6 RevA units and 6 RevC units passed 1000 hrs at Tj 146C and 151C
    - ESD: 3/3 units passed 2kV HBM per JEDEC JS-001
    - Latch-up: 3/3 units passed level 1 per JEDEC (JESD78) LU
    - NVM:
      - Non Volatile Cycling Endurance (NVCE; JESD22-A117) : 8/8 passed 400 cycles
      - High Temperature Retention (HTR, JESD22-A117) : 5/5 passed 536 hrs @ Tj=250C
- **QML Class Q Qualification**
  - SMD first draft in progress
- **QML Class V Qualification**
  - It is our intention to achieve QML-V

# RTG4 IP Cores

- SpaceWire – StarDundee
  - Demonstrated in RTG4 Rev A silicon at 200Mb/sec
  - To be validated in Rev C silicon
- SpaceFibre – StarDundee
  - Demonstrated in RTG4 Rev A silicon at 2.5Gb/sec
  - To be validated in Rev C silicon
- Leon3FT – Cobham Gaisler
  - Performance benchmark in Libero 11.7 software in progress
- Cortex M1 – ARM
  - Licensing agreement with ARM in final phase
  - To be validated in Rev C silicon. Target completion by June
- SRIO – IP vendor evaluation in progress



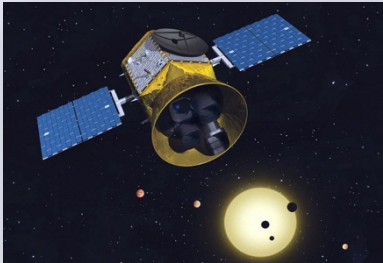
# RTG4 Software Update

- Libero SoC v11.6 SP1 – Released on 12/24/2015
  - Updated clock power contribution in SmartPower
- Libero SoC v11.7 – Released on 2/11/2016
  - Enable Rev C programming for RT4G150 device
  - Support up to 206 asynchronous resets
    - RT4G150 designs from previous Libero releases will be invalidated
    - RT4G150\_ES designs from previous Libero releases will be given option to update to latest cores
  - Fabric-generated clocks can be routed to nearest CCC to use CCC's SET filter
  - SynplifyPro
    - Infer non-pipelined ECC for LSRAM and uSRAM using directive “syn\_ramstyle=ecc”
    - Infer sequential-shift construct and map to uSRAM through a directive
  - Tie-off unused FDDR, SERDES, CCC, uPROM to save power
  - SmartPower includes updated static power and adds uPROM power
  - Improved Repair Min-delay feature by increasing the number of violated paths analyzed
- Power Estimator v3j – Released in Feb 2016
  - Added maximum process
  - Updated static power for core, IO bank and VPP



# Programs Baselineing RTG4

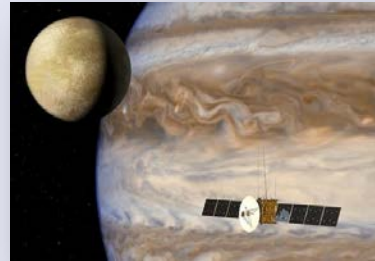
TESS  
(NASA)



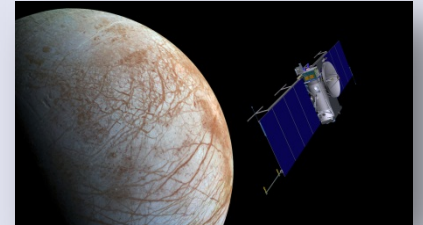
Orion  
(NASA)



JUICE  
(ESA)



Europa  
(JPL)



Digital Channelizer  
(Commercial)



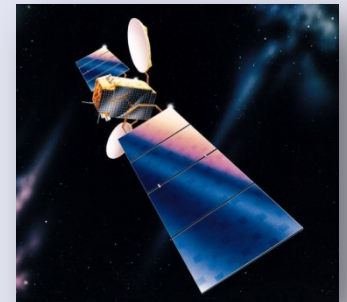
AIDA  
(ESA, DLR, NASA)



SLIM  
(JAXA)

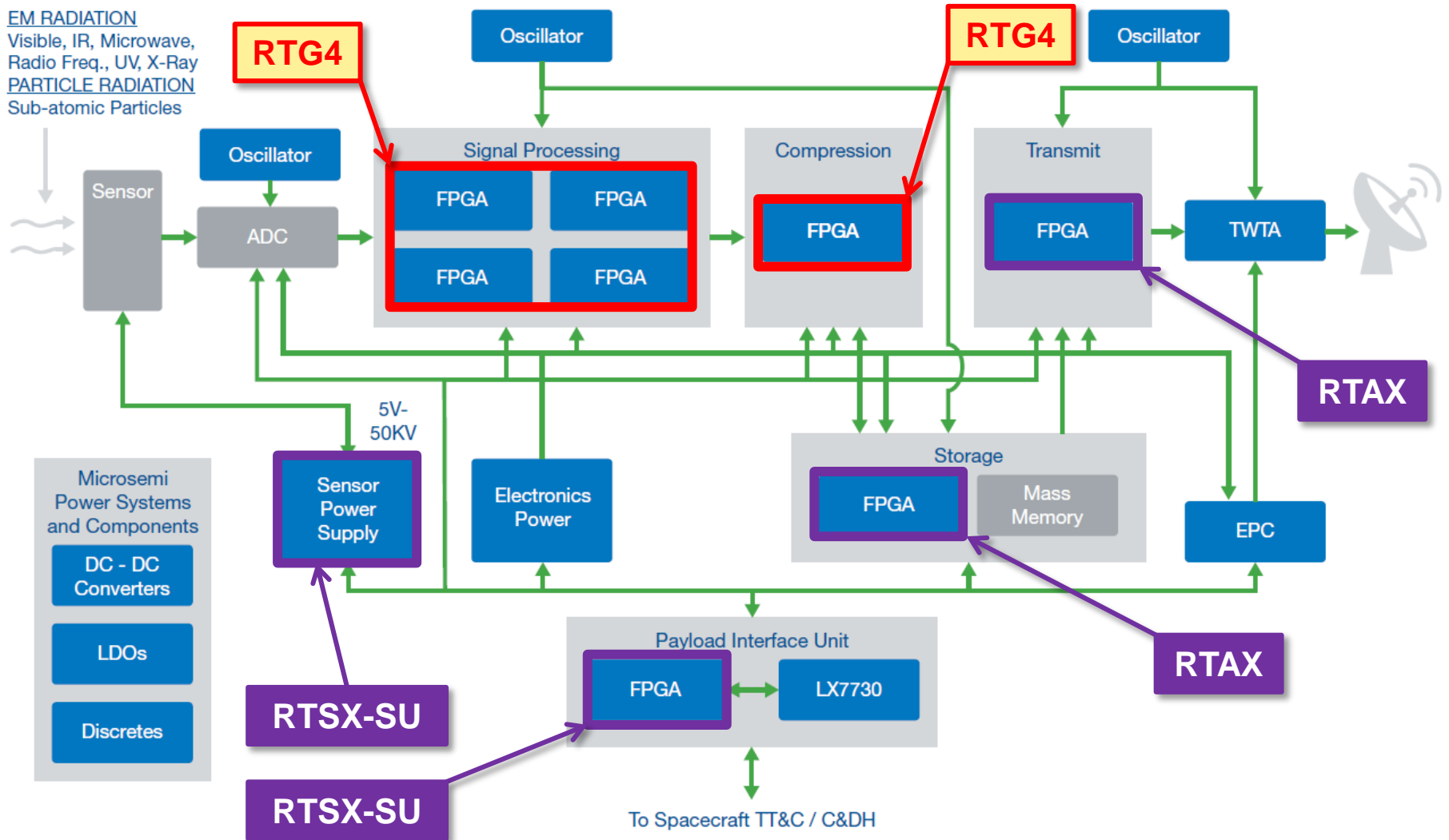


Commercial  
Program



# FPGAs in Remote Sensing Payload

EM RADIATION  
Visible, IR, Microwave,  
Radio Freq., UV, X-Ray  
PARTICLE RADIATION  
Sub-atomic Particles



**RTG4 complements existing Microsemi Radiation Tolerant FPGAs**

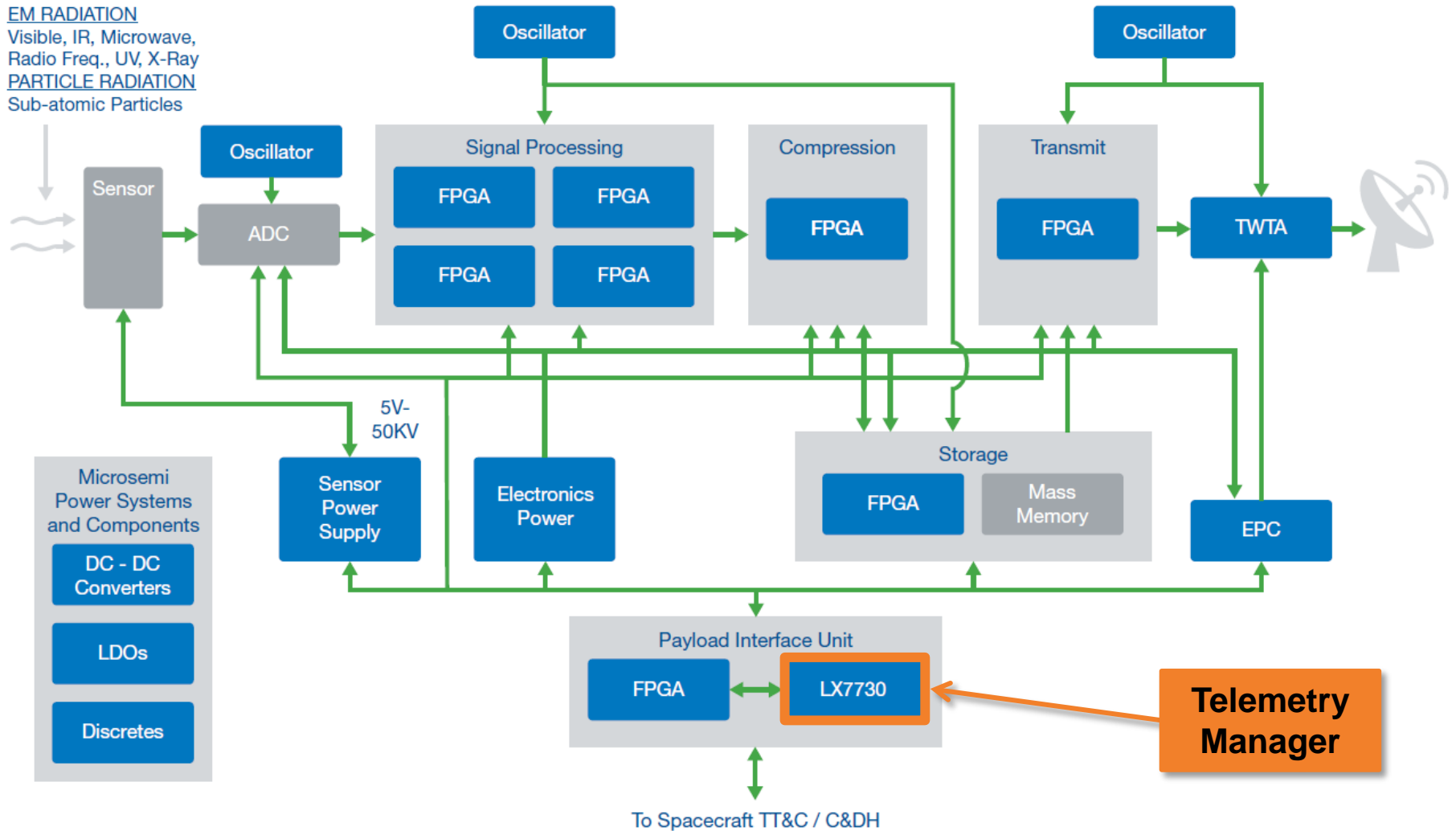
# Space System Managers in Remote Sensing Payload

## EM RADIATION

Visible, IR, Microwave,  
Radio Freq., UV, X-Ray

## PARTICLE RADIATION

Sub-atomic Particles



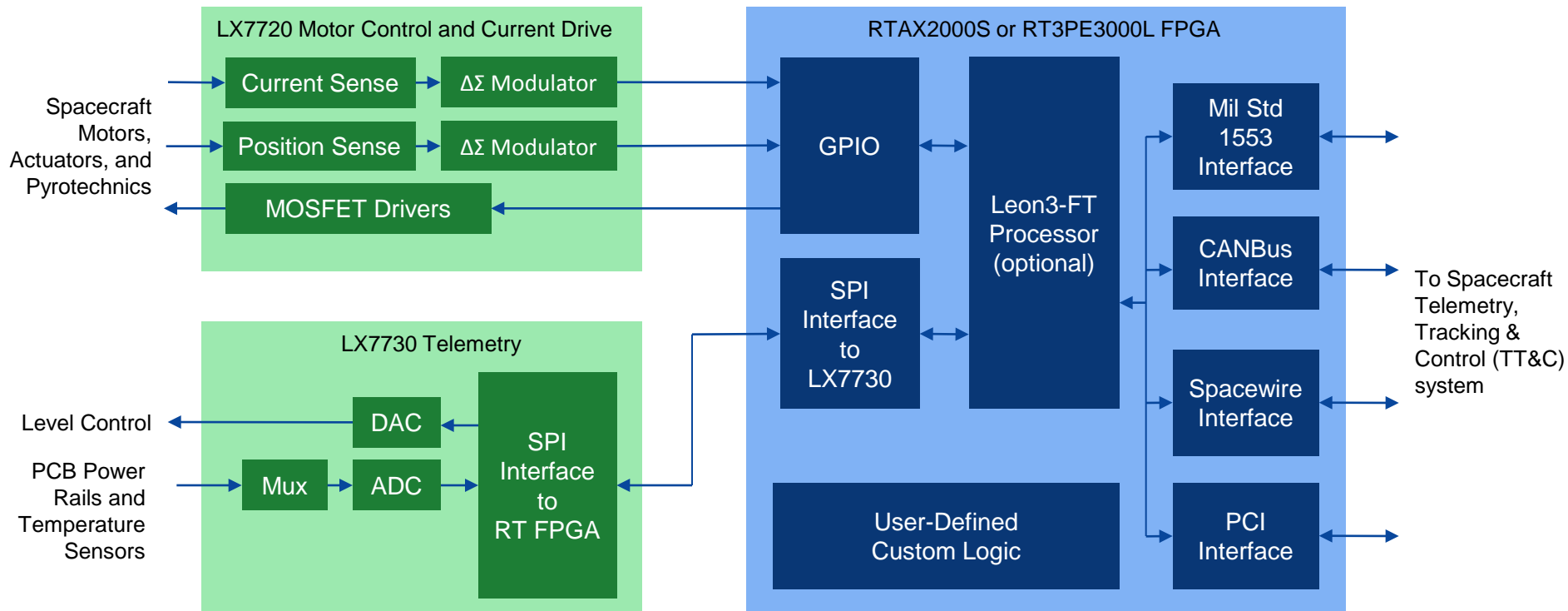
*RTG4 complements other Microsemi space products*

# Space System Managers

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# Space System Managers

- Standard off-the-shelf solutions for telemetry and power driver in space
- Microsemi mixed signal standard ASICs
  - LX7720 current sense, rotary position sense and MOSFET drivers
  - LX7730 voltage, current and temperature telemetry
- Microsemi RT FPGAs implement digital interface with satellite control bus





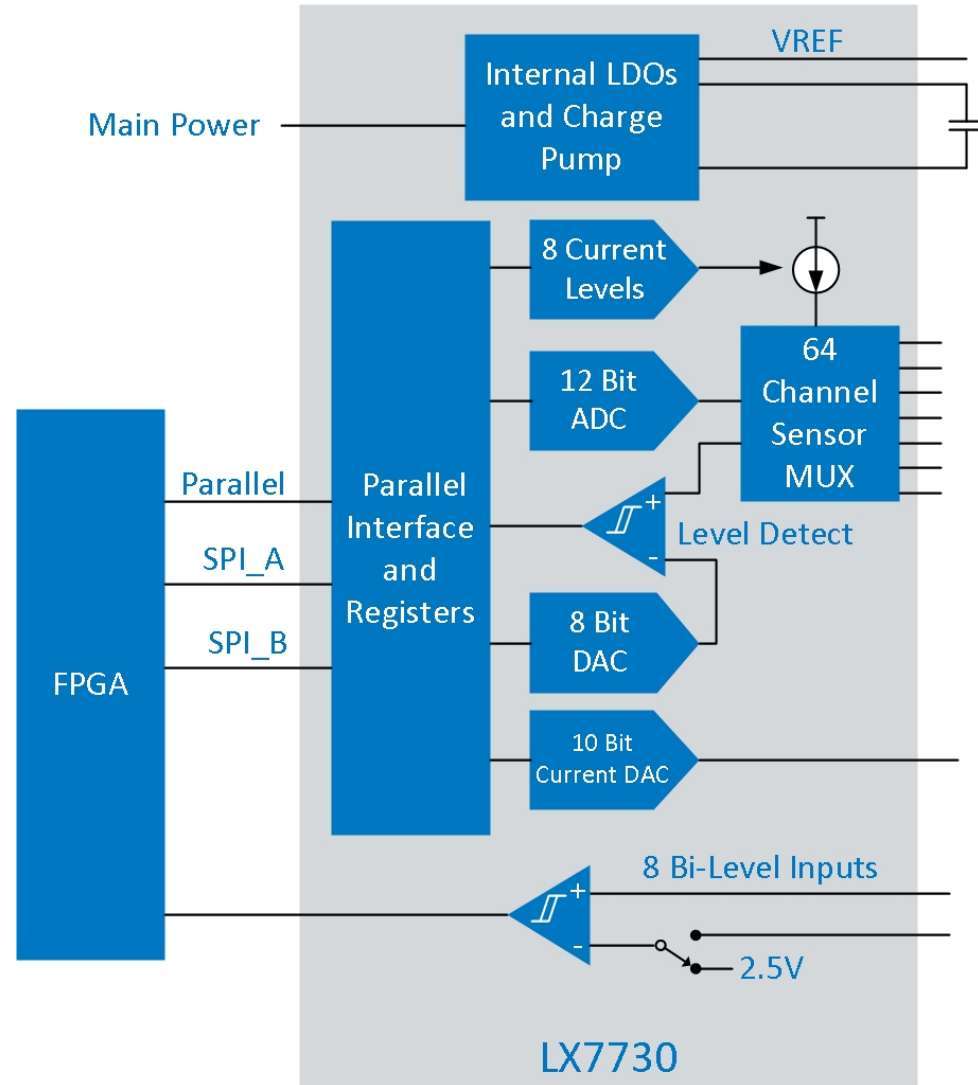
# LX7730 Telemetry Controller

## Features

- 64 channel MUX
- 25kSPS 12 bit ADC
- 2% Precision Adjustable Current Source
- 1% Precision 5.00V Source
- Threshold Monitoring
- 8 x Bi-level Logic
- 10 bit DAC
- Parallel or Dual SPI Interface
- Radiation Tolerant: 100krad TID, 50krad ELDRS, SE immune

## Applications

- Spacecraft Environment Monitoring
- Attitude Control
- Payload Equipment



# LX7730 Performance Highlights

Parameter	Comment	Min	Typ	Max	Units
SE or Diff sensor input		0		5	V
Differential Sensor common mode		-5		5	V
ADC conversion rate			25		kHz
ADC acquisition time			20		us
Reference voltage	Internal VREF	4.95	5.00	5.05	V
ADC non-linearity (integral or diff)		-2	0	2	LSB
MUX settling time			1.5		us
MUX leakage current	Power on or off	-100		100	nA
Bi-level threshold range		0.5		4.6	V
Bi-level propagation delay			1		us
DAC compliance range		0		3.0	V
DAC full scale current	Sourcing	1.94	2.00	2.06	mA

# LX7730 Single Event Radiation Test Results

Test	Conditions	Results
SEL Testing	Test up to $1e8$ part/cm <sup>2</sup> and 87.85MeV/mg.cm <sup>2</sup>	SEL Immune
SET Testing	Test up to $2.46e5$ part/cm <sup>2</sup> and 83.13MeV/mg.cm <sup>2</sup>	SET Immune on all generated voltages
SEU Scan Chain Test (269 FF)	Test up to $1.01e5$ part/cm <sup>2</sup> and 83.13MeV/mg.cm <sup>2</sup>	SEU Immune on all internal FFs
SEE DC Telemetry Test	Test up to $1.21e5$ part/cm <sup>2</sup> and 43.64MeV/mg.cm <sup>2</sup>	SE Immune to radiation events up to LET of 43.64MeV/mg.cm <sup>2</sup>
SEE AC Telemetry Test	Test up to $7.0e6$ part/cm <sup>2</sup> and 83.13MeV/mg.cm <sup>2</sup>	SE Immune to radiation events up to LET of 83.13MeV/mg.cm <sup>2</sup>
SEE Current Source Test	Test up to $1.0e6$ part/cm <sup>2</sup> and 43.64MeV/mg.cm <sup>2</sup>	SE Immune to radiation events up to LET of 43.64MeV/mg.cm <sup>2</sup>
SEE Current DAC Test	Test up to $1.0e6$ part/cm <sup>2</sup> and 43.64MeV/mg.cm <sup>2</sup>	SE Immune to radiation events up to LET of 43.64MeV/mg.cm <sup>2</sup>
SEE Cold Spare Test	Test up to $1.0e6$ part/cm <sup>2</sup> and 43.64MeV/mg.cm <sup>2</sup>	SE Immune to radiation events up to LET of 83MeV/mg.cm <sup>2</sup>

# LX7730 Availability Update

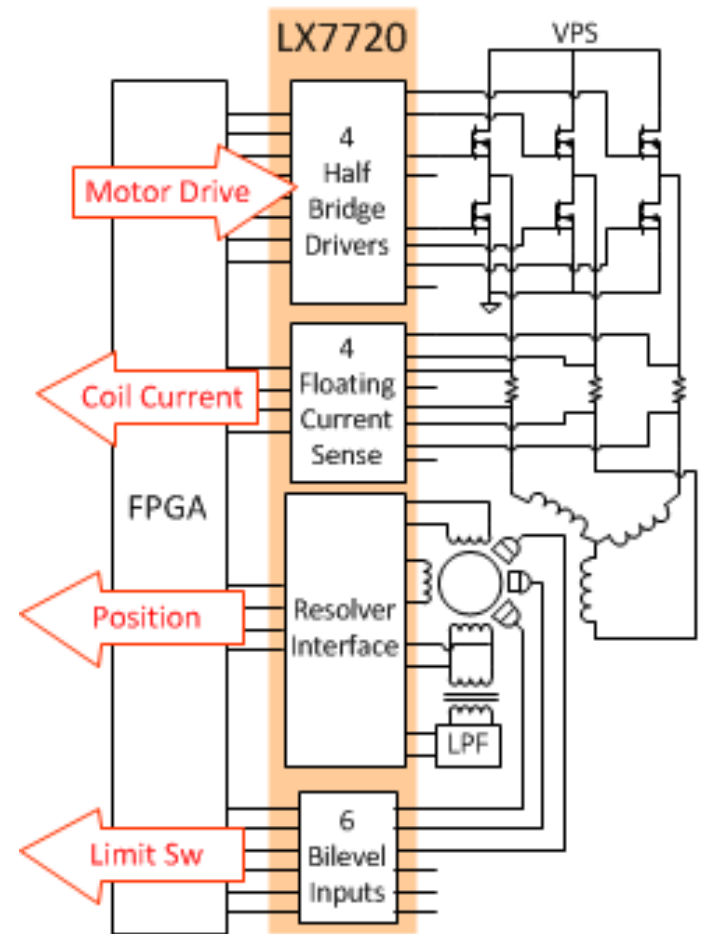
- Available now – LX7730 Engineering Silicon (ES) and LX7730 Evaluation Board (EVB)
- Product Availability

Part Number	Silicon	Availability
LX7730-ES & EVB	Production version	Now
LX7730MFQ-EQ samples	Pre-production Q flow samples	CQ2 2016
LX7730MFQ-EQ production	Production	CQ4 2016
LX7730MFQ-EV samples	Pre-production V flow samples	CQ2 2016
LX7730MFQ-EV production	Production	CQ4 2016

- We are seeking QML-Q and QML-V qualification

# LX7720 Power Driver

- Provides MOSFET motor drivers
  - 3 phase motors
  - Unipolar or bipolar steppers
- 4 high and low side relay drivers
- Up to 4 current sensors
  - Phase currents or RTN currents
  - Average current control loops
- Sensing for resolver or LVDT
- Detecting pulse sensors and limit switches
- Combination of LX7720 and FPGA provides a closed loop system



# LX7720 Performance Highlights

Parameter	Comment	Min	Typ	Max	Units
Motor Power Supply	De-rated by 20%	20	48	150	V
MOSFET driver impedance	Source or sink			1	$\Omega$
PWM frequency		DC		200	kHz
Current sense differential range		-250		250	mV
Current sense accuracy			7		bits
Current sense latency			1.5		$\mu$ S
Resolver carrier frequency		0.36		20	kHz
Resolver accuracy			16		bits
Bi-level threshold range		0.5		4.6	V
Bi-level propagation delay			1		$\mu$ s

# LX7720 Availability Update

- Launch and customer sampling in summer 2016
- Product Availability

Part Number	Silicon	Availability
LX7720-ES & EVB	Preliminary version	CQ3 2016
LX7720MFQ-EQ samples	Pre-production Q flow samples	CQ2 2017
LX7720MFQ-EQ production	Production	CQ3 2017
LX7720MFQ-EV samples	Pre-production V flow samples	CQ2 2017
LX7720MFQ-EV production	Production	CQ4 2017

- We are seeking QML-Q and QML-V qualification

# Conclusion

## ■ RTG4 High-Speed RT FPGAs

- High-bandwidth signal and data processing in radiation applications
- Radiation hardening by design
  - TID immune to > 125 kRAD
  - SEL and configuration upset immune to 103 MeV-cm<sup>2</sup>/mg
- MIL-STD-883 Class B qualification to be completed in Sept 2016
- Contact:  
[Minh.U.Nguyen@microsemi.com](mailto:Minh.U.Nguyen@microsemi.com), [Ken.O'Neill@microsemi.com](mailto:Ken.O'Neill@microsemi.com)

## ■ Space System Managers

- Standard mixed signal IC for space applications
- Radiation hardening by design
  - TID immune to 100 kRAD
  - SEL immune to 87 MeV-cm<sup>2</sup>/mg
- Contact:  
[Dorian.Johnson@microsemi.com](mailto:Dorian.Johnson@microsemi.com), [Ken.O'Neill@microsemi.com](mailto:Ken.O'Neill@microsemi.com)





# Summary

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- Microsemi is dedicated, focused, and investing in space products and capabilities
- Microsemi has been in the space business as a partner with our customers for more than 55 years
- Microsemi has the system, circuit, and production experience in space to be a long term supplier of state-of-the-art products for long life cycles
- Microsemi uses a system view of applications, and a broad range of technology and design experience to build the best-in-class products for space

# Microsemi Space Forum

- Presentations available at <http://www.microsemi.com/spaceforum>



Microsemi  
SPACE FORUM

East Coast	West Coast	Europe	India	India
<b>June 2nd 2015</b> Westfield's Marriott Washington Dulles Chantilly, VA	<b>June 4th 2015</b> Los Angeles Airport Marriott Los Angeles, CA	<b>June 18th 2015</b> The Palace Hotel Noordwijk, Netherlands	<b>August 11th 2015</b> Courtyard Marriott Ahmedabad, India	<b>August 13th 2015</b> The Leela Palace Bangalore, India