SEFUW: SpacE FPGA Users Workshop, 3rd Edition

Tuesday 15 March 2016

Design Experiences - Newton 1 and 2 (10:50 - 12:35)

-Conveners: David Merodio Codinachs

time	[id] title	presenter
10:50	[35] Implementation of Space-Industry IP : A Comparison of Space-Grade FPGAs	Dr BEDI, Rajan
11:20	[57] FPGA development flow for future large space FPGA	Mr MANNI, Florent
11:45	[41] Prototyping a SOC on RTAX4000D for Solar Orbiter's Low Frequency Receiver.	Mr JEANDET, Alexis
12:10	[74] LEON3/GRLIB for Space-Grade Programmable Devices Update and Roadmap	Mr ANDERSSON, Jan

Wednesday 16 March 2016

Design Experiences - Newton 1 and 2 (12:35 - 13:00)

-Conveners: Agustin Fernandez-Leon

time	[id] title	presenter
12:35	[44] Resource-Efficient Debugging Core to Evaluate FPGA Designs in On-Board Processors	Mr RITTNER, Florian