AURUM
Final Presentation

ESTEC, 2016

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THALES ALENIA SPACE INTERNAL

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AURUM RECONFIGURATION MODULE – Final Presentation

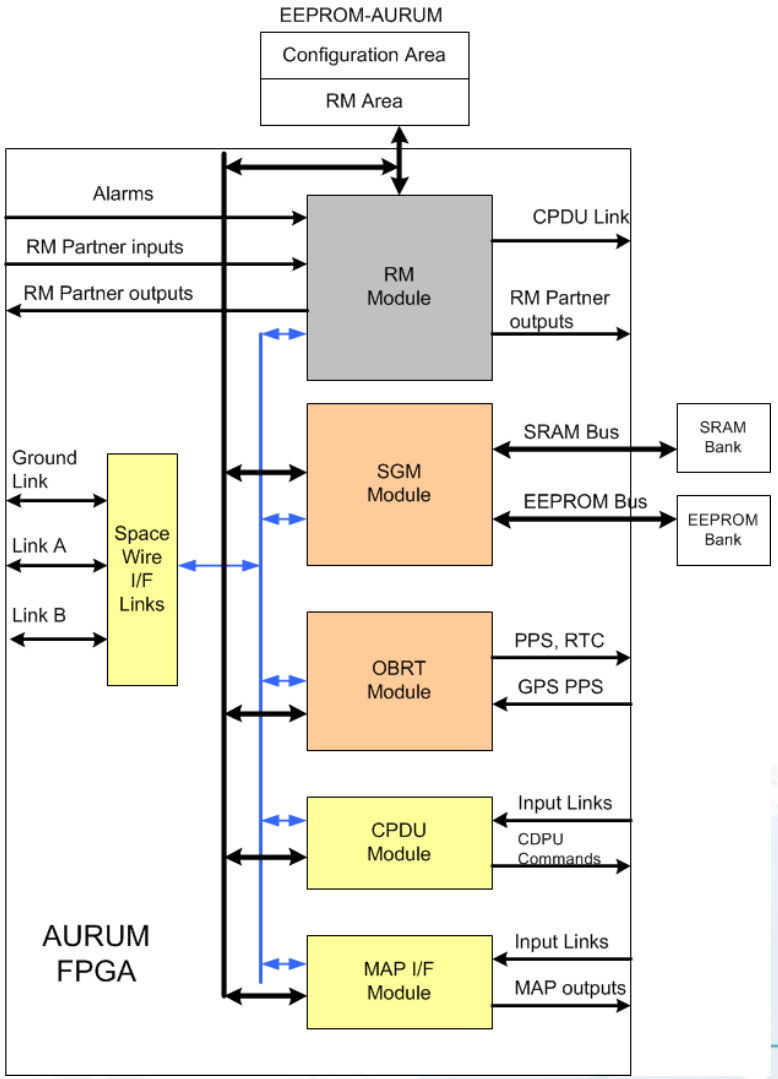
Project Context & schedule

- AURUM FPGA : RM development in the frame of a GSTP5 contract
- Based on the reutilization of the AURUM-I FPGA with modifications to comply with the DOS-F needs (ASRA and SMU equipment specification)
- SRR Held on March 2014
- Activities stopped from June up to end of 2014
- End of RM VHDL design : February 2015
- Global AURUM-F integration : May 2015
- PDR Review : June – July 2015
- CDR & AR Review : December 2015
- Final Presentation Review : June 2016 ← Here we are

AURUM Definition

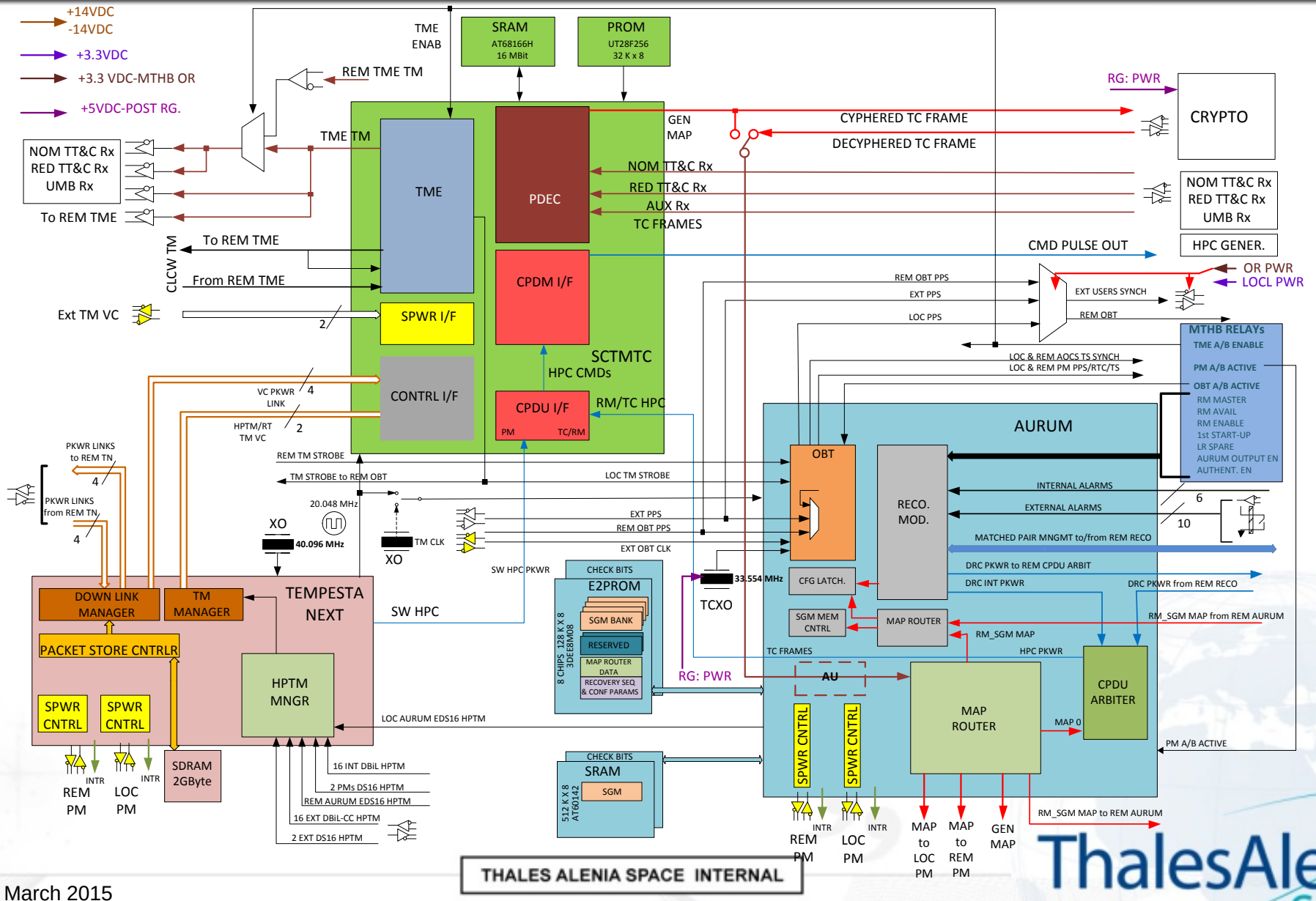
The AURUM FPGA implements:

- MAP Router to decode and forward the incoming TC segments from an external TC Decoder
- Input MAP I/Fs in order to receive and process “Low Level Commands” and SGM “Memory Load” commands from Ground
- CPDU Arbiter to manage Reconfiguration Commands coming from Local and Partner AURUM as well as HPC from Ground
- Reconfiguration Module for Matched Pair Management, Surveillance and Recovery Functions
- On Board Time Module for timing and synchronization functions
- Safe Guard Memory Module
- Management of Configuration Parameters
- SpaceWire I/F to communicate with Nominal and Redundant Processor Modules



AURUM – RM Presentation

AURUM Environment



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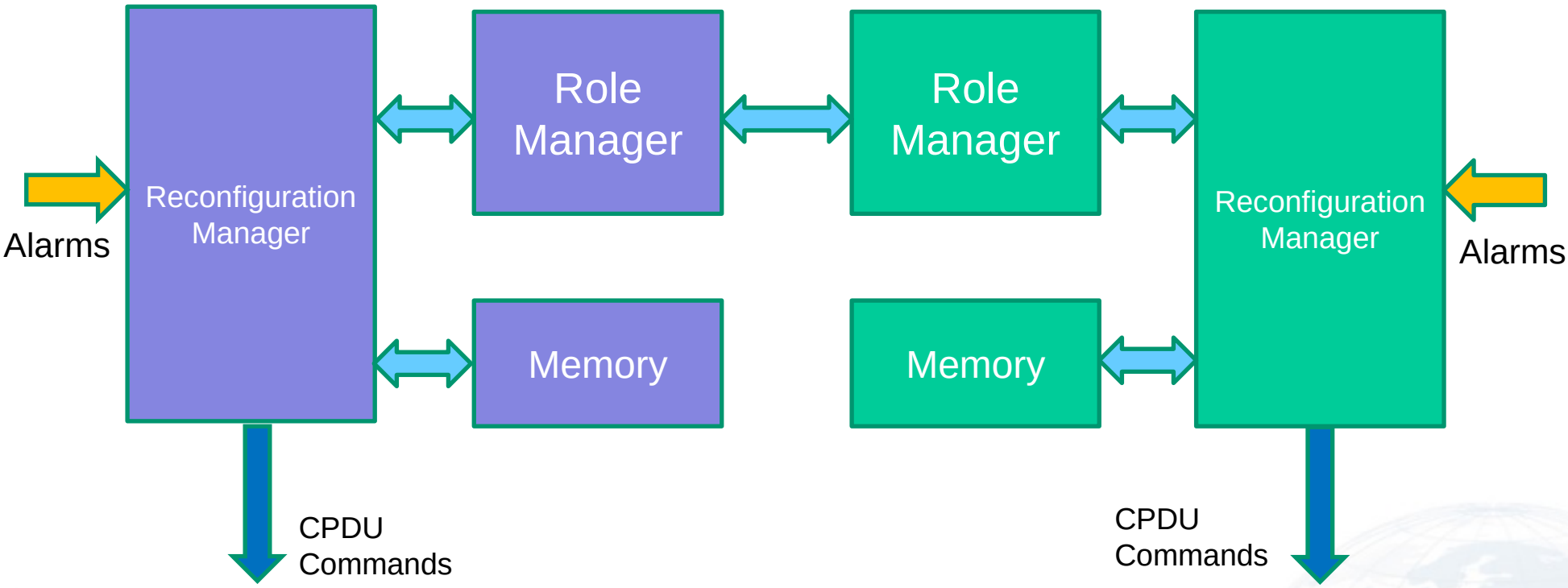
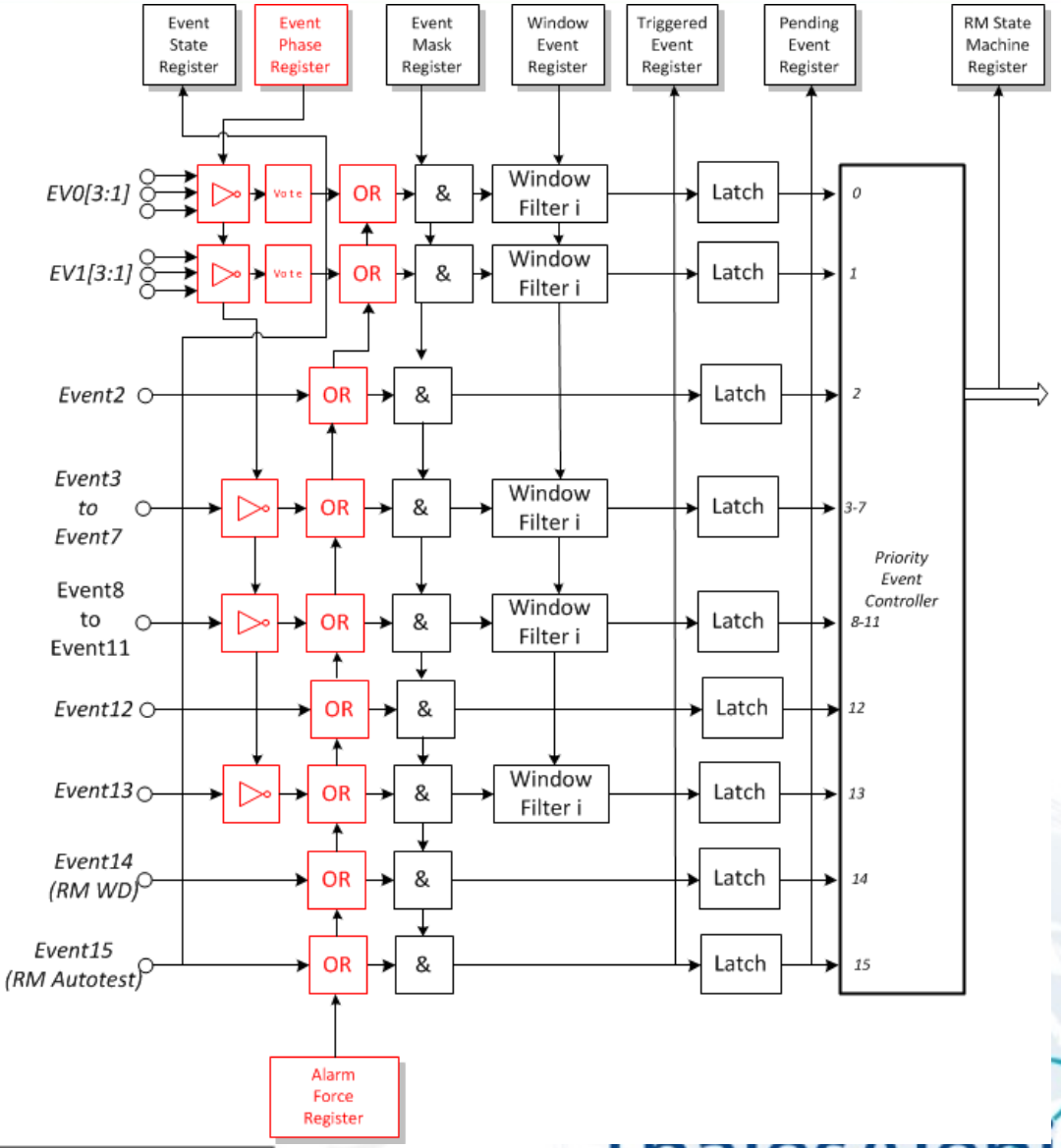
RM Redundancy concept



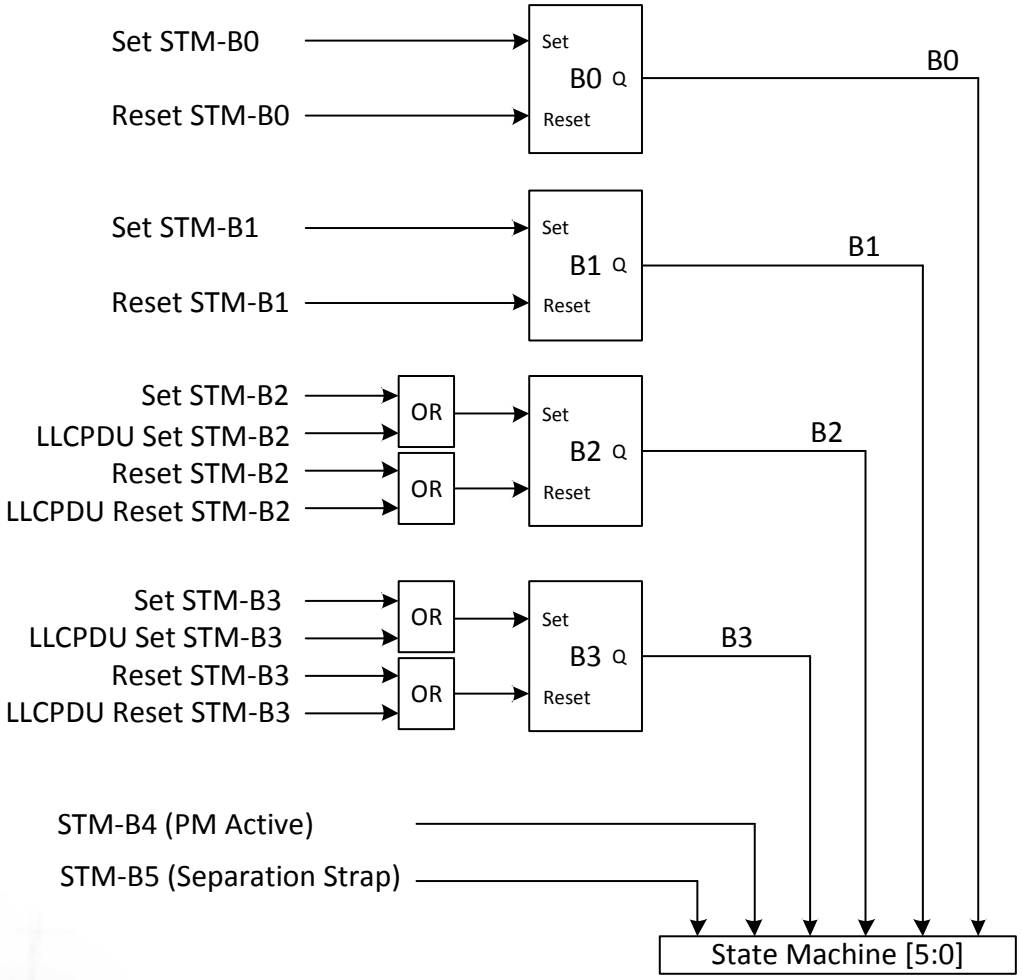
- Hot Redundancy:
  - One RM is master, authorized to generate CPDU commands
  - The other RM is Slave, surveying the Master and not authorized to send CPDU Cmds

RM Alarms Management

- 16 Events Management
  - 12 External, two with majority vote capability
  - 2 Software Events
  - 1 Watch Dog (for PM)
  - 1 RM Autotest (event 15)
- Events priority management
  - Event 0 has highest priority
  - Pending events management
- Alarm force register for AIT purposes



RM State Machine



- Capability to associate up to 16 different sequences to each event pending on the active PM and to the Satellite Separation Status
- RM State can be changed during a reconfiguration sequence
- RM State sub-set can be modified by ground TC

RM Sequence Generation upon event

- The Event number + the State Machine value define the Seq_Number[9:0] pointer giving the address on the Sequence Pointer Table of the Sequence to be executed
- Up to 63 different Reconfiguration Sequences can be defined
- Dummy sequences must be defined for not used ones.
- The length of each Reconfiguration Sequence is fixed.

RM Reconfiguration Sequence Format

- The Header field is used to check failures on data bus
- First DLC list is used to mask events, Reset WD, stop Autotest and send interrupts to PM
- Last DLC list is used to enable WD, reset pending interrupts and unmask events
- CRC Result field is used to check the sequence integrity

Mode	Field	Length	Contents	Comments
M/S	Header	1	Start ID	Fixed to 0x55
M/S	Header	1	Inverted Start ID	Fixed to 0xAA
M/S	Header	1	Reserved	Fixed to 0x00
M/S	Header	1	Reserved	Fixed to 0x00
M/S	Internal DLC List1	32	List of up to 32 DLCs	
M	CPDU L1	10	Single CDPU Command	
M/S	Delay L1	1	Delay of 5ms to N*100ms	from 5ms up to 25,5 s
M	CPDU P1	10	Single CDPU Command	
M/S	Delay P1	1	Delay of 5ms to N*100ms	from 5ms up to 25,5 s
M	CPDU L2	10	Single CDPU Command	
M/S	Delay L2	1	Delay of 5ms to N*100ms	from 5ms up to 25,5 s
M	CPDU P2	10	Single CDPU Command	
M/S	Delay P2	1	Delay of 5ms to N*100ms	from 5ms up to 25,5 s
	……			
M	CPDU L31	10	Single CDPU Command	
M/S	Delay L31	1	Delay of 5ms to N*100ms	from 5ms up to 25,5 s
M	CPDU P31	10	Single CDPU Command	
M/S	Delay P331	1	Delay of 5ms to N*100ms	from 5ms up to 25,5 s
M	CPDU L32	10	Single CDPU Command	
M/S	Delay L32	1	Delay of 5ms to N*100ms	from 5ms up to 25,5 s
M	CPDU P32	10	Single CDPU Command	
M/S	Delay P32	1	Delay of 5ms to N*100ms	from 5ms up to 25,5 s
M/S	Internal DLC List2	32	List of up to 32 DLCs	
M/S	Seq. Error Control	1	CRC Result - 8 MSB	
M/S		1	CRC Result - 8 LSB	

RM Implemented Digital Level Commands Detail (1/2)

- State Machine – Set/Reset B0-B3
  - Used to change the value of the State Machine bits during a Reconfiguration
  - Allows to manage up to 16 different States/Reconfigurations for the same Event
- MaskAllEv / UnMaskAllEv / UnMaskEv I / MaskEv i
  - Usually Events shalll be masked at the beginning to avoid additional alarms triggering then unmasked at the end of the reconfiguration
- RstAllPend
  - To be done at the end of the Reconfiguration to guarantee no other Reconfigurations execution due to the same Alarm effect
- WD_Arming_int
  - To rearm the WatchDog before ending the reconfiguration and restart the PM in a correct condition.
  - Usually to be done just before unmasking the WD Alarm

RM Implemented Digital Level Commands Detail (2/2)

- AutoStop / RMWD_Set /RMWD_Reset (RM Autotest Management)
  - AutoStop shall be used to stop ongoing Autotest inside the specific RM Test reconfiguration Sequence
  - RMWD_Reset shall be used at the beginning of a System Reconfiguration to avoid a Mastership Release due to the RM Autotest WD
  - RMWD_Set shall be sent at the end of the System Reconfiguration to authorize again the RM Autotest
- Reset_PM_Local /Reset_PM_Partner
  - To Reset Local and or Partner PM inside a Reconfiguration Sequence
- PM_Int
  - To send an interrupt to both PM to notify them than a reconfiguration is in progress The flag RF_RSO (“Recovery Function Recovery Sequence Ongoing”) of the Interrupt Register is set.
- Hot_IT_PM_Local / Hot_IT_PM_Partner
  - To send separate and direct interrupts to each PM to notify them than a reconfiguration is in progress.

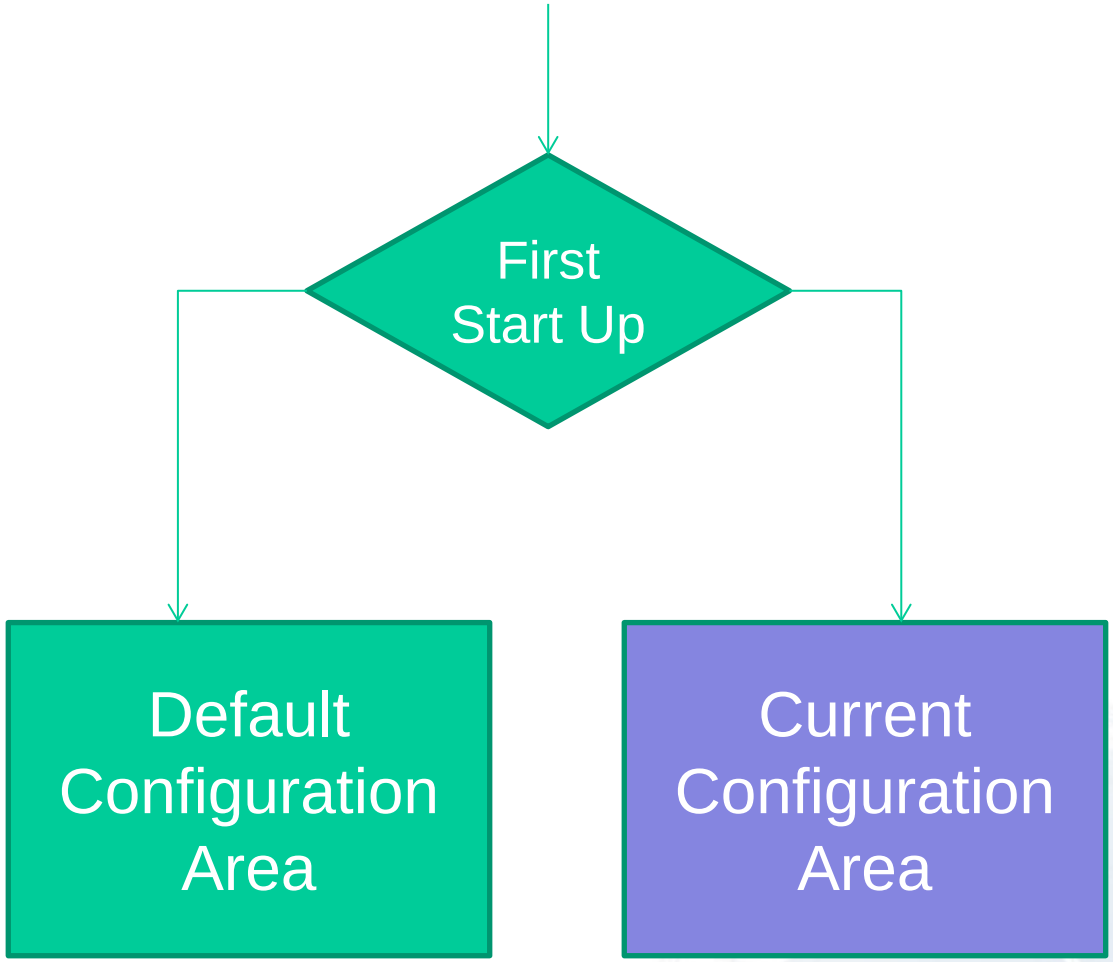
RM Sequence execution

- The good completion of a Reconfiguration Sequence is guaranteed by the checks performed before the execution :
  - Check of the sequence number, Header Field and CRC value
- And during the execution :
  - During the “Delay Li/Pi” delay the Slave checks if there is a Master/slave change and if done, he comes back to the previous CPDU command and continues the execution of the sequence as Master
- To guaranteed the good synchronisms between both RM
  - The Slave RM waits the equivalent time needed by the Master to send CPDU commands (fixed value) before going on

The minimum Reconfiguration duration is 390 ms (no delays between CPDU commands)

RM initialization capability

- RM can be initialized with data coming from two different area
- The choice of the area is defined by the “First Star-up” input signal
- Default area can only be written in ground
- Current area can be modified in flight if RM in Configuration mode



RM Failure Modes Analysis

- Failure on main clock or secondary power supply :
  - ✓ Detected by MPM Role management
- Failure on EEPROM data bus (bit stuck to 0 or 1) :
  - ✓ Detected by Header check of a sequence
- Failure on EEPROM data (bit cell stuck) :
  - ✓ Detected by CRC check
- Failure on RM Event Encoder on Sequence Generator blocs :
  - ✓ Detected by RM Autotest mechanism
- Specific failure on MPM interface leading to have 2 RM in master mode :
  - ✓ Compatible with the Sequence generation implementation. Each RM will send the first CDPU packet to the local Command Generator then the other to the partner CG.

Current Status & Next Steps

- Current Status :
  - ✓ AURUM reprogrammable FPGA used on 3 SMU FUMOs (L3G)
  - ✓ L3G EQM under manufacturing (AURUM FPGA will be burnt this month)

- Next Steps
  - ✓ RM Modelisation (tool for platform user)
  - ✓ L3G EQM (embedding AURUM) Qualification campaign T3 2016
  - ✓ AURUTC Authentication by Sofware (GSTP Extension)

End of presentation

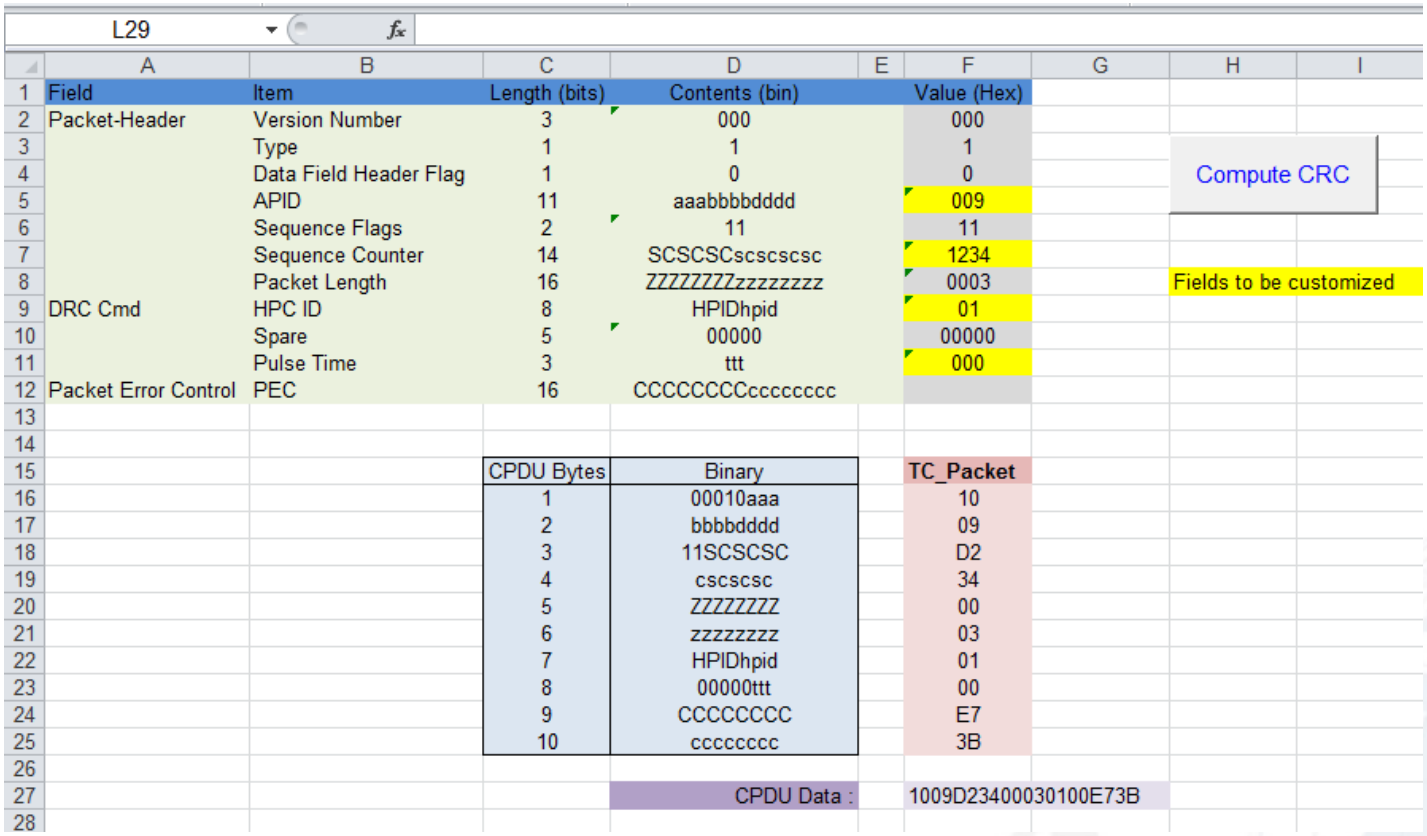
That's all

Thanks for your attention

Annexes

RM Sequences Definition Tools

- The Tool is based in an Excel File simplifying the elaboration of the RM Data
- The CDPU Format sheet allows to build CDPU commands and compute CRC field to be added in the CDPU Commands List



L29

	A	B	C	D	E	F	G	H	I
1	Field	Item	Length (bits)	Contents (bin)		Value (Hex)			
2	Packet-Header	Version Number	3	000		000			
3		Type	1	1		1		Compute CRC	
4		Data Field Header Flag	1	0		0			
5		APID	11	aaabbbbdddd		009			
6		Sequence Flags	2	11		11			
7		Sequence Counter	14	SCSCSCscscscsc		1234			
8		Packet Length	16	ZZZZZZZZzzzzzzzz		0003		Fields to be customized	
9	DRC Cmd	HPC ID	8	HPIDhpid		01			
10		Spare	5	00000		00000			
11		Pulse Time	3	ttt		000			
12	Packet Error Control	PEC	16	CCCCCCCCcccccccc					
13									
14									
15			CPDU Bytes	Binary		TC_Packet			
16			1	00010aaa		10			
17			2	bbbbdddd		09			
18			3	11SCSCSC		D2			
19			4	cscscsc		34			
20			5	ZZZZZZZZ		00			
21			6	zzzzzzzz		03			
22			7	HPIDhpid		01			
23			8	00000ttt		00			
24			9	CCCCCCCC		E7			
25			10	cccccccc		3B			
26									
27				CPDU Data :		1009D23400030100E73B			
28									

RM Sequence Definition Tools

- The CPDU Commands List can be customized according to the Mission needs
- CPDU commands are automatically inserted from CPDU Format Sheet by the user

	A	B	C	D	E	F	G	H
1	CPDU Commands							
2	**Cmd N°**	**@ Hexa**	**CPDU_List**	**Action**	**Data (10 bytes)**			
3	0	00	Empty CPDU	No action	1009D23400030000D40A			
4	1	01	CPDU#1	HLC#1	1009D23400030100E73B		Add CDPU	
5	2	02	CPDU#2	HLC#2	1009D23400030100E73B			
6	3	03	CPDU#3	HLC#3	1009D23400030100E73B			
7	4	04	CPDU#4	HLC#4	00000000000000000000			
8	5	05	CPDU#5	HLC#5	00000000000000000000		Adds the CPDU data computed c	
9	6	06	CPDU#6	HLC#6	00000000000000000000		To add a CPDU Data, the cell wh	
10	7	07	CPDU#7	HLC#7	00000000000000000000			
11	8	08	CPDU#8	HLC#8	00000000000000000000			
12	9	09	CPDU#9	HLC#9	00000000000000000000			
13	10	0A	CPDU#10	HLC#10	00000000000000000000			
14	11	0B	CPDU#11	HLC#11	00000000000000000000			
15	12	0C	CPDU#12	HLC#12	00000000000000000000			
16	13	0D	CPDU#13	HLC#13	00000000000000000000			
17	14	0E	CPDU#14	HLC#14	00000000000000000000			
18	15	0F	CPDU#15	HLC#15	00000000000000000000			
19	16	10	CPDU#16	HLC#16	00000000000000000000			
20	17	11	CPDU#17	HLC#17	00000000000000000000			
21	18	12	CPDU#18	HLC#18	00000000000000000000			
22	19	13	CPDU#19	HLC#19	00000000000000000000			

RM Sequence Definition Tools

- The DLC Commands Sheet gives all the DLC used by RM

	A	B	C	D	E	F
1	Cmd N° (Dec)	DLC	DLC_List	Cmd (Bin)	Cmd (Hexa)	Action
2	0	DLC0	No action	00000000	00	No action
3	16	DLC16	STM - Reset B0	00010000	10	
4	17	DLC17	STM - Reset B1	00010001	11	
5	18	DLC18	STM - Reset B2	00010010	12	
6	19	DLC19	STM - Reset B3	00010011	13	
7	32	DLC32	STM - Set B0	00100000	20	
8	33	DLC33	STM - Set B1	00100001	21	
9	34	DLC34	STM - Set B2	00100010	22	
10	35	DLC35	STM - Set B3	00100011	23	
11	46	DLC46	Unmask All Events	00101110	2E	
12	47	DLC47	Mask All Events	00101111	2F	
13	64	DLC64	Mask Event0	01000000	40	
14	65	DLC65	Mask Event1	01000001	41	
15	66	DLC66	Mask Event2	01000010	42	
16	67	DLC67	Mask Event3	01000011	43	
17	68	DLC68	Mask Event4	01000100	44	
18	69	DLC69	Mask Event5	01000101	45	
19	70	DLC70	Mask Event6	01000110	46	
20	71	DLC71	Mask Event7	01000111	47	
21	72	DLC72	Mask Event8	01001000	48	
22	73	DLC73	Mask Event9	01001001	49	
23	74	DLC74	Mask Event10	01001010	4A	
24	75	DLC75	Mask Event11	01001011	4B	
25	76	DLC76	Mask Event12	01001100	4C	
26	77	DLC77	Mask Event13	01001101	4D	
27	78	DLC78	Mask Event14	01001110	4E	
28	79	DLC79	Mask Event15	01001111	4F	
29	80	DLC80	Rearm Internal WD	01010000	50	
30	85	DLC85	Stop RM Autotest	01010101	55	
31	90	DLC90	Set TMWD Validation	01011010	5A	
32	91	DLC91	Reset TMWD Validation	01011011	5B	
33	96	DLC96	Reset All Pending Events	01100000	60	
34	112	DLC112	PM Interrupt	01110000	70	
35	113	DLC113	Reset Local PM pulse	01110001	71	
36	114	DLC114	Reset Partner PM pulse	01110010	72	

RM Sequence Definition Tools

- The Sequence Format sheet allows to build a complete Reconfiguration Sequence using the DLC and CPDU commands already build in the previous sheets

	A	B	C	D	E	F	G	H
1	**Sub-Address**	**Dec**	**Field**	**Length**	**Contents**	**Comments**	**Value**	**Compute CRC**
2	Hexa		Header					
3	000	0		1	Start ID	0x55 - fixed	55	
4	001	1		1	Inverted Start ID	0xAA - fixed	AA	
5	002	2		1	Reserved	0x00 - fixed	00	
6	003	3		1	Reserved	0x00 - fixed	00	
7	004	4	Internal DLC List1	1	No action	List of up to 32 DLCs	00	
8	005	5	Internal DLC List2	1	STM - Reset B0		10	
9	006	6	Internal DLC List3	1	STM - Set B0		20	
10	007	7	Internal DLC List4	1			00	
11	008	8	Internal DLC List5	1			00	
12	009	9	Internal DLC List6	1			00	
13	00A	10	Internal DLC List7	1			00	
14	00B	11	Internal DLC List8	1			00	
15	00C	12	Internal DLC List9	1			00	
16	00D	13	Internal DLC List1(	1			00	
17	00E	14	Internal DLC List11	1			00	
18	00F	15	Internal DLC List12	1			00	
19	010	16	Internal DLC List13	1			00	
20	011	17	Internal DLC List14	1			00	
21	012	18	Internal DLC List15	1			00	
22	013	19	Internal DLC List16	1			00	
23	014	20	Internal DLC List17	1			00	
24	015	21	Internal DLC List18	1			00	

No action
STM - Reset B0
STM - Reset B1
STM - Reset B2
STM - Reset B3
STM - Set B0
STM - Set B1
STM - Set B2

RM Sequence Definition Tools

- The Sequence Format sheet allows to build a complete Reconfiguration Sequence using the DLC and CPDU commands already build in the previous sheets

	A	B	C	D	E	F	G	H
1	**Sub-Address**	**Dec**	**Field**	**Length**	**Contents**	**Comments**	**Value**	**Compute CRC**
2	Hexa		Header					
39	024	36	CPDU L1	1	CPDU#3	Single Command	10	
49	02E	46	Delay L1	1	300 ms	Delay of N*100ms : 0 to 25,5 s	03	
50	02F	47	CPDU P1	1		Single Command	00	
60	039	57	Delay P1	1	400 ms	Delay of N*100ms : 0 to 25,5 s	04	
61	03A	58	CPDU L2	1	Empty CPDU	ngle Command	10	
71	044	68	Delay L2	1		lay of N*100ms : 0 to 25,5 s	00	
72	045	69	CPDU P2	1		ngle Command	10	
82	04F	79	Delay P2	1		lay of N*100ms : 0 to 25,5 s	00	
83	050	80	CPDU L3	1		ngle Command	10	
93	05A	90	Delay L3	1		lay of N*100ms : 0 to 25,5 s	00	
94	05B	91	CPDU P3	1		ngle Command	10	
104	065	101	Delay P3	1	0 ms	Delay of N*100ms : 0 to 25,5 s	00	
105	066	102	CPDU L4	1	Empty CPDU	Single Command	10	
115	070	112	Delay L4	1	0 ms	Delay of N*100ms : 0 to 25,5 s	00	
116	071	113	CPDU P4	1	Empty CPDU	Single Command	10	
126	07B	123	Delay P4	1	0 ms	Delay of N*100ms : 0 to 25,5 s	00	
127	07C	124	CPDU L5	1	Empty CPDU	Single Command	10	
137	086	134	Delay L5	1	0 ms	Delay of N*100ms : 0 to 25,5 s	00	
138	087	135	CPDU P5	1	Empty CPDU	Single Command	10	
148	091	145	Delay P5	1	0 ms	Delay of N*100ms : 0 to 25,5 s	00	
149	092	146	CPDU L6	1	Empty CPDU	Single Command	10	
159	09C	156	Delay L6	1	0 ms	Delay of N*100ms : 0 to 25,5 s	00	
160	09D	157	CPDU P6	1	Empty CPDU	Single Command	10	
170	0A7	167	Delay P6	1	0 ms	Delay of N*100ms : 0 to 25,5 s	00	
171	0A8	168	CPDU L7	1	Empty CPDU	Single Command	10	
181	0B2	178	Delay L7	1	0 ms	Delay of N*100ms : 0 to 25,5 s	00	

Empty CPDU
CPDU#1
CPDU#2
CPDU#3
CPDU#4
CPDU#5
CPDU#6
CPDU#7

RM Sequence Definition Tools

- The Sequence Format sheet allows to build a complete Reconfiguration Sequence using the DLC and CPDU commands already build in the previous sheets

	A	B	C	D	E	F	G	H
1	**Sub-Address**	**Dec**	**Field**	**Length**	**Contents**	**Comments**	**Value**	**Compute CRC**
2	Hexa		Header					
760	2F5	757	Internal DLC List18	1			00	
761	2F6	758	Internal DLC List19	1			00	
762	2F7	759	Internal DLC List20	1			00	
763	2F8	760	Internal DLC List21	1			00	
764	2F9	761	Internal DLC List22	1			00	
765	2FA	762	Internal DLC List23	1			00	
766	2FB	763	Internal DLC List24	1			00	
767	2FC	764	Internal DLC List25	1			00	
768	2FD	765	Internal DLC List26	1			00	
769	2FE	766	Internal DLC List27	1			00	
770	2FF	767	Internal DLC List28	1			00	
771	300	768	Internal DLC List29	1			00	
772	301	769	Internal DLC List30	1			00	
773	302	770	Internal DLC List31	1			00	
774	303	771	Internal DLC List32	1			00	
775	304	772	Seq. Error Control	1	CRC Result - 8 MSB	CRC s@=000h	EC	
776	305	773		1	CRC Result - 8 LSB	up to s@303h	0A	
777	306	774		249	Free			
778	3FF	1023						
779								
780								
781								

RM Sequence Definition Tools

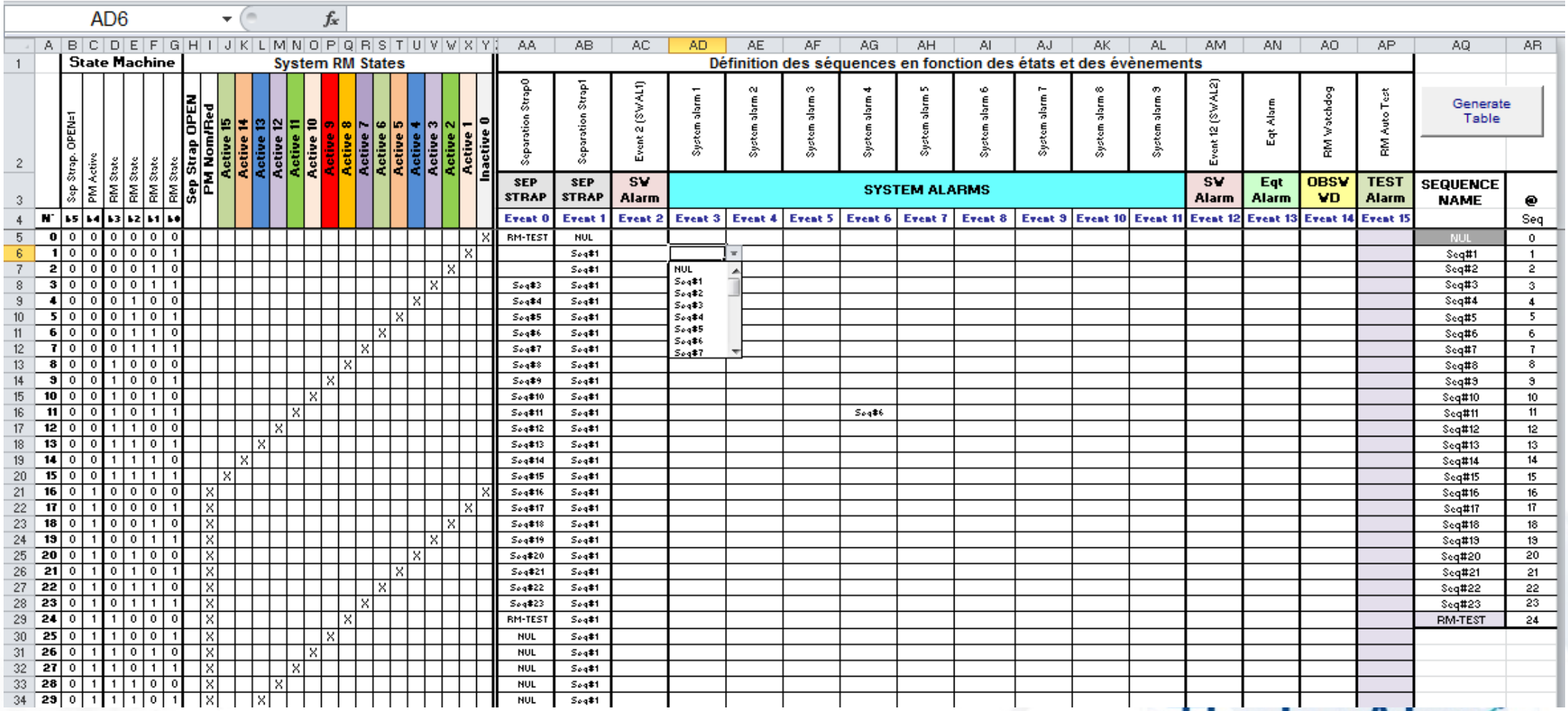
- The RM Sequences sheet includes all the defined sequences. They can be automatically added from the Sequence Format Sheet

	A	B	C	D	E	F	G	H	I	J
1		Add Sequence								
2	Field	Seq#1	Delay (ms)	Seq#2	Delay (ms)	Seq#3	Delay (ms)	Seq#4	Delay (ms)	Seq#5
3	Start ID	0x55		0x55		0x55		0x55		0x55
4	Inv. Start ID	0xAA		0xAA		0xAA		0xAA		0xAA
5	Reserved	0x00		0x00		0x00		0x00		0x00
6	Reserved	0x00		0x00		0x00		0x00		0x00
7	DLC-L1-1	00		No action						
8	DLC-L1-2	10		STM - Reset B0						
9	DLC-L1-3	20		STM - Set B0						
10	DLC-L1-4	00								
11	DLC-L1-5	00								
12	DLC-L1-6	00								
13	DLC-L1-7	00								
14	DLC-L1-8	00								
15	DLC-L1-9	00								
16	DLC-L1-10	00								
17	DLC-L1-11	00								
18	DLC-L1-12	00								
19	DLC-L1-13	00								
20	DLC-L1-14	00								
21	DLC-L1-15	00								
22	DLC-L1-16	00								
23	DLC-L1-17	00								
24	DLC-L1-18	00								
25	DLC-L1-19	00								
26	DLC-L1-20	00								
27	DLC-L1-21	00								
28	DLC-L1-22	00								
29	DLC-L1-23	00								
30	DLC-L1-24	00								
31	DLC-L1-25	00								
32	DLC-L1-26	00								
33	DLC-L1-27	00								
34	DLC-L1-28	00								
35	DLC-L1-29	00								

AURUM – RM Final Presentation

RM Sequence Definition Tools

- The Reconfiguration Table sheet allows to define the Reconfiguration Strategy
  - The List of Sequence on the Right side and be added by List choice



RM Role Manager Definition

- Possible RM combinations

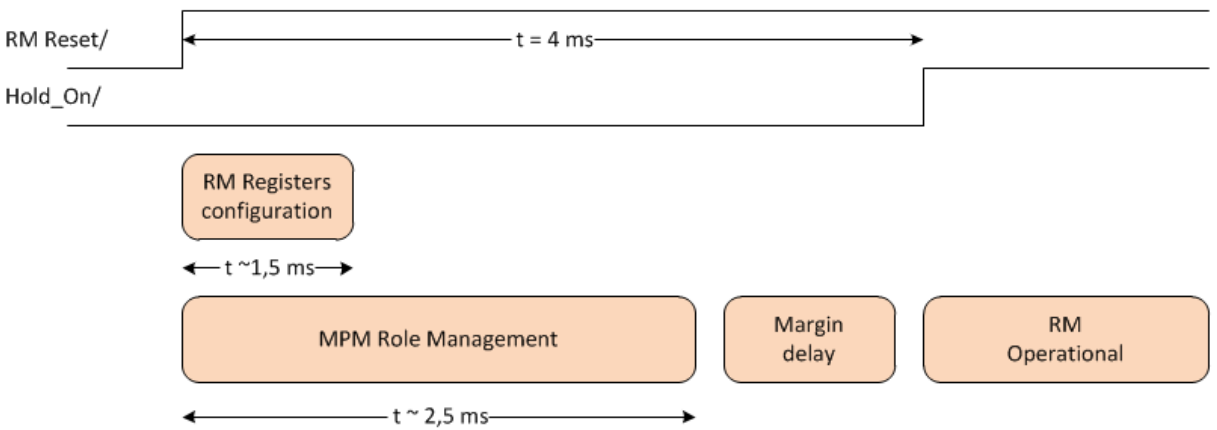
		RM-1			
		Master	Stand-by	Configuration	Off (Vcc loss)
RM-2	Master	**YES (1)**	YES	YES	**YES**
	Stand-by	YES	NO	NO	**NO**
	Configuration	YES	NO	NO	**NO**
	Off (Vcc loss)	YES	NO	NO	NO

(1) This combination may occur only in case of failure. This ambiguity must be resolved at ASW level or Ground level.

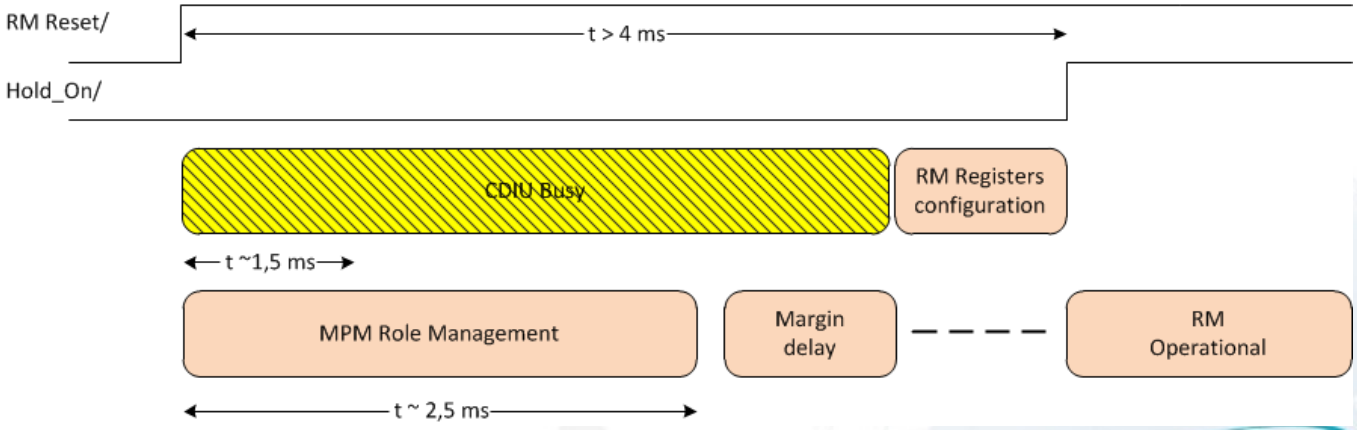
RM Initialization Phase

- The RM Configuration parameters are loaded in the internal Registers
- The MPM starts the Role contention to define the Master and Slave
- After 4 ms the RM is ready to process Alarms
- The RM WD and RM Autotest start when RM is Operational

CASE1 – CPUI I/F ready

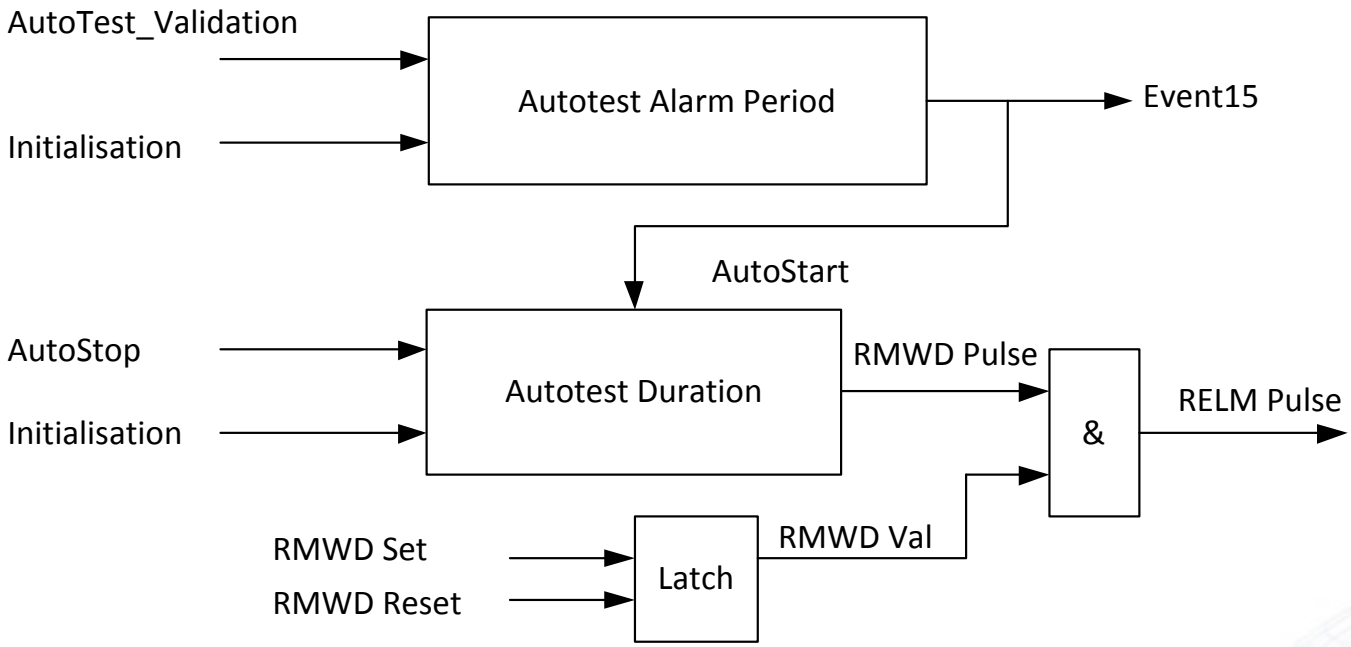


CASE2 – CPUI I/F busy



RM Autotest

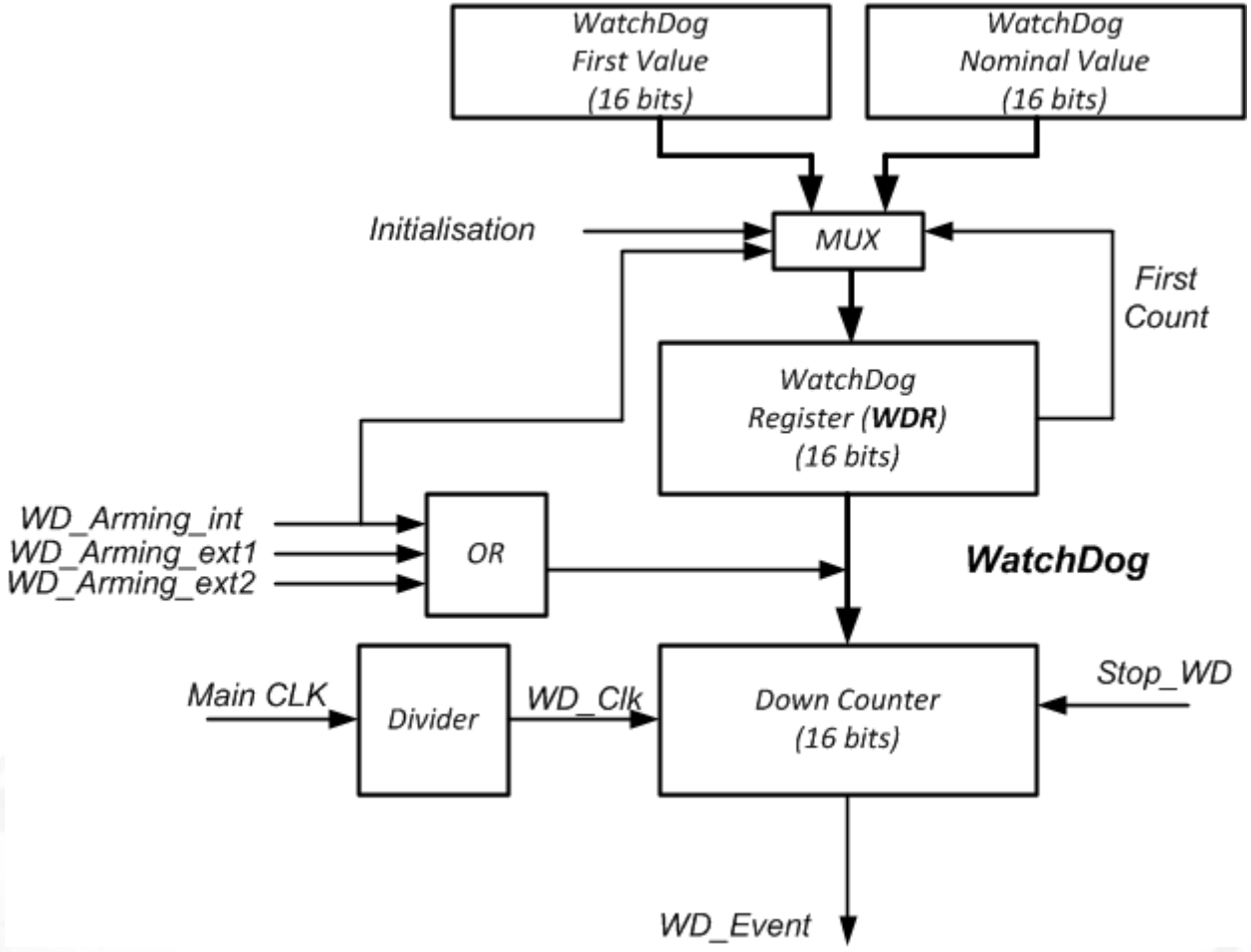
- Allows to detect failures on the event processor or memory management of the RM before an operational sequence execution



- The Autotest Alarm Period will be configurable between 16 seconds and 256 seconds
- The Autotest watch dog duration will be configurable between 4 seconds and 64 seconds
- Can be inhibit and re started during a nominal reconfiguration sequence

RM Watch Dog Event

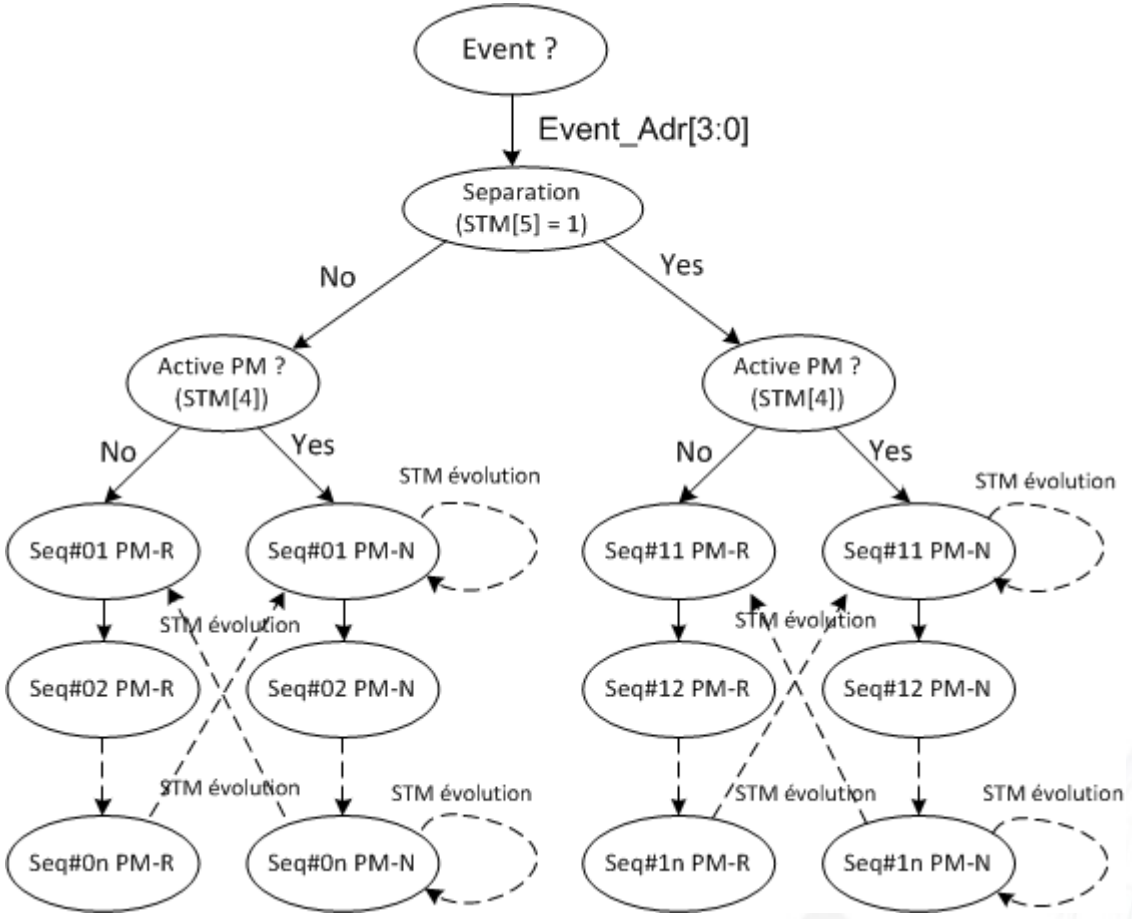
- Allows to detect any failure on PM or in the internal communication link (SpW)



- Implements a first power on delay and nominal watch dog period
- Can be rearmed by a command inside a reconfiguration sequence or by each PM
- Can be Stopped during AIT (stop WD input pin)
- WD delay and period can be programmed from 1 ms up to 65.5 seconds

RM States Capability

- Thanks to the use of “Satellite Separation” information, “Active PM” and internal events States, it is possible to define a powerful FDIR strategy



RM CPDU commands management

- The “CPDU Li/Pi” fields are complete CDPU Packets (length fixed to 10 bytes) to be sent to the External CDPU I/F module only if the RM is in Master_Mode
- The coherence and definition of the CPDU packet shall be guaranteed at equipment level
- The fields “Delay Li/Pi” correspond to the delay to be waited before continuing the reconfiguration sequence. The contents of each field is the number of steps of 100 ms to be waited from 0x00 (5 ms of fixed delay) up to 0xFF (25,5 seconds).

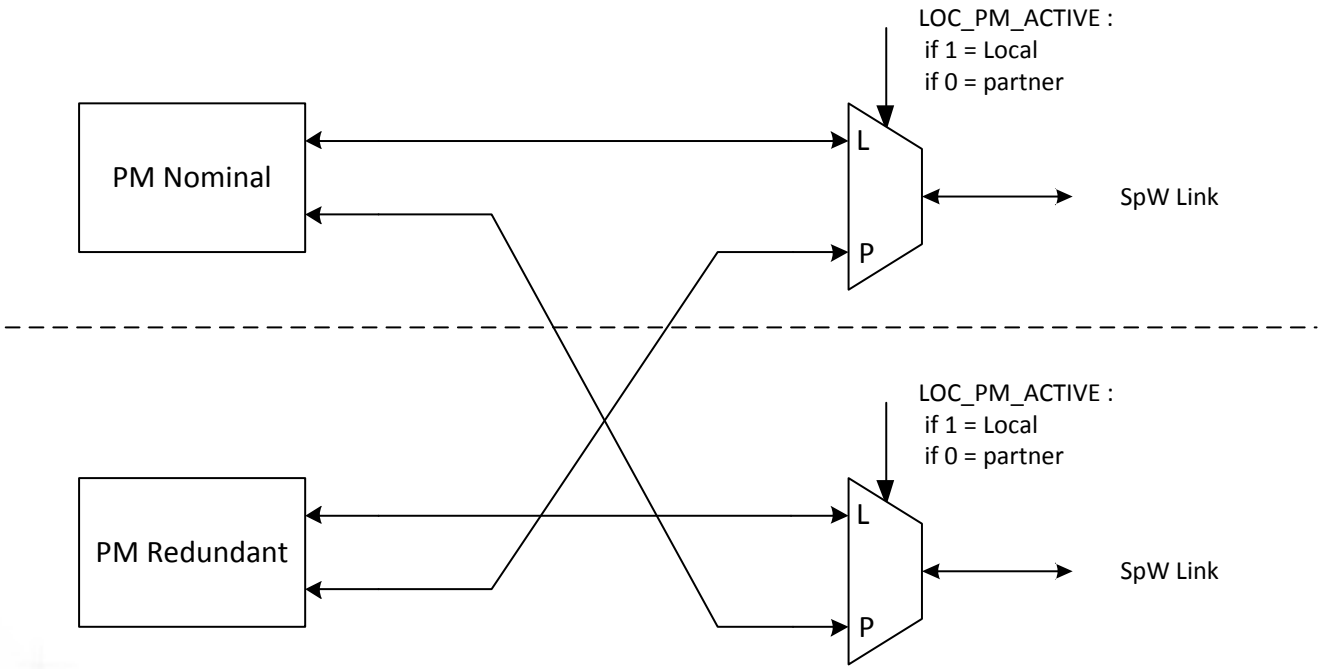
CPDU packets	Physical output	Remarks
CPDU Li packets	Routed to the local CPDU arbiter block	internal FPGA routing Sending time is ~ 1ms
CPDU Pi packets	Routed to the Partner AURUM - CPDU arbiter block	Sending time is ~ 1ms

RM Configuration Latches

- The RM configuration latches value can be changed by ground CPDU commands :
  - RM Auto Test configuration
  - PM Write Enable to RM Registers
- The RM State Machine bits B2 & B3 can be changed by ground CPDU command in addition of DLC commands

RM-PM Space Wire Cross-Strap

- AURUM-F manages 2 SpaceWire links, but only one is selected at a time.
- The selection is done using the LOC_PM_ACTIVE input pin Status.



LOC_PM_ACTIVE pin value is always inverted between nominal en redundant paths and managed at equipment level

RM Registers

- RM Status Registers :
  - State Machine, Last Triggered Event, Last Sequence Executed
  - Configuration Latches values; Check Errors raised
  - History from last 16 Reconfigurations
  - Real Time Events Status
  - Pending Event Registers
  - Triggered Events
  - Role Manager Status

GSTP Work Packages

- WP 1100 - AURUM Requirements Definition & Analysis
- WP 1200 - Feasibility Study
- WP 2100 - Architectural and Detailed Design of the AURUM FPGA
- WP 2200 - Detailed Design and layout generation and verification
- WP 3100 - Validation/Testing of the AURUM FPGA
- WP 3200 - Preparation for Final Review
- WP 4100 - Project Management
- WP 4200 - Test & System Support

AURUM – CDR/AR - ANNEXES

GSTP Deliverables

	GSTP Deliverable	Included in doc ##	Chapter ##
TN1	AURUM FPGA Requirement Specification	Aurum Requirement Specification : 0005-0004705919 issue 4	All
TN2	AURUM FPGA Requirements Trade off and Analysis	Aurum Requirements analysis : 0005-0004806175 issue 1	All
TN3	AURUM FPGA Development Plan	Aurum FPGA Development Plan : 0005-0004704758 issue 4	All
TN4	AURUM FPGA Control Plan	Aurum FPGA Control Plan : 0005-0004704736 issue 1,1	All
TN5	AURUM FPGA Feasability and Risk Analysis	TN5a - Aurum Feasability Study : 0005-0006565645 issue 3 TN5b - Aurum Risk Analysis : 0005-0006565684 issue 3	All All
TN6	AURUM FPGA Architecture definition report	AURUM_F Design Description : 0005-0006567536 issue 2	Chapt 5
TN7	AURUM FPGA verification plan	AURUM_F Design Description : 0005-0006567536 issue 2	Chapt 7
TN8	AURUM FPGA verification and optimization report	AURUM_F Design Description : 0005-0006567536 issue 2	Chapt 8
TN9	AURUM FPGA verification plan (updated)	AURUM_F Design Description : 0005-0006567536 issue 2	Chapt 7
TN10	AURUM FPGA verification and optimization report (updated)	AURUM_F Design Description : 0005-0006567536 issue 2	Chapt 8
TN11	AURUM FPGA Design entry report	AURUM_F Design Description : 0005-0006567536 issue 2	Chapt 9
TN12	AURUM FPGA Netlist generation report	AURUM_F Design Description : 0005-0006567536 issue 2	Chapt 9
TN13	AURUM FPGA Netlist verification report	AURUM_F Design Description : 0005-0006567536 issue 2	Chapt 9
TN14	AURUM FPGA Design validation plan	AURUM_F Test Plan : 0005-0006574178 issue 1	All
TN15	AURUM FPGA data sheet	Aurum_F DataSheet : 0005-0006552976 issue 2	All
TN16	AURUM FPGA Validation Report	Test Report : TLW-DOC-01396_v1_Test Report	All
TN17	Reconfiguration Module for the Multi-mission Core Computer Final Report (Executive summary included)	TBW *(Final Presentation)*	
TN18	Reconfiguration Module for the Multi-mission Core Computer Final Presentation	TBW *(Final Presentation)*	
TN19	Reconfiguration Module for the Multi-mission Core Computer Project webpage	TBW *(Final Presentation)*	
TN20	AURUM FPGA detailed specification	Aurum Requirement Specification : 0005-0004705919 issue 4	All