Reconfiguration Module for Multimission Core Computer

The objectives of these GSTP activity were :

- To design the AURUM FPGA functions, compliant Thales Alenia Space needs for Observation & Science.
- To procure a Bread Board of the TMTCMMRM board on with the AURUM FPGA is embedded,
- To verify the newly developed RM functions on the TMTCMMRM Bread Board.

The RM functions as defined on this GSTP allow its re-usability for future CNES & ESA missions to extend its potential applications to Observation & Science applications, for a wide variety of orbits.

The testing was performed by a mixed TAS-F Toulouse and TAS-I Gorgonzola team, using TAS-I Milan test facilities already procured and developed in the frame of the Italian TMTCMMRM board design.

The AURUM FPGA, implements the following functions:

- MAP Router to decode and forward the incoming TC segments from an external TC Decoder
- Input MAP I/Fs in order to receive and process “Low Level Commands” and SGM “Memory Load” commands from Ground
- CPDU Arbiter to manage Reconfiguration Commands coming from Local and Partner AURUM as well as HPC from Ground
- Reconfiguration Module for Matched Pair Management, Surveillance and Recovery Functions
- On Board Time Module for timing and synchronization functions
- Safe Guard Memory Module
- Management of Configuration Parameters
- SpaceWire I/F to communicate with Nominal and Redundant Processor Modules