TEC-SW Final Presentation Days 2016

LeonSVF Multicore Prototype for Leon3

Activity: Lab Investment
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Agenda

- **First Part : leonSVF Overall Presentation**
  - Context
  - LEB Features
  - Principle of Operation
- ***Second part (Telespazio-Vega GmbH):***
  - Independent Characterization
- **Third Part : MultiCore Prototype**
  - Multicore Design Overview
  - New features
  - Qualification & Performance
  - Main Lesson learned
  - Conclusion

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Part 1
leonSVF Overall Presentation

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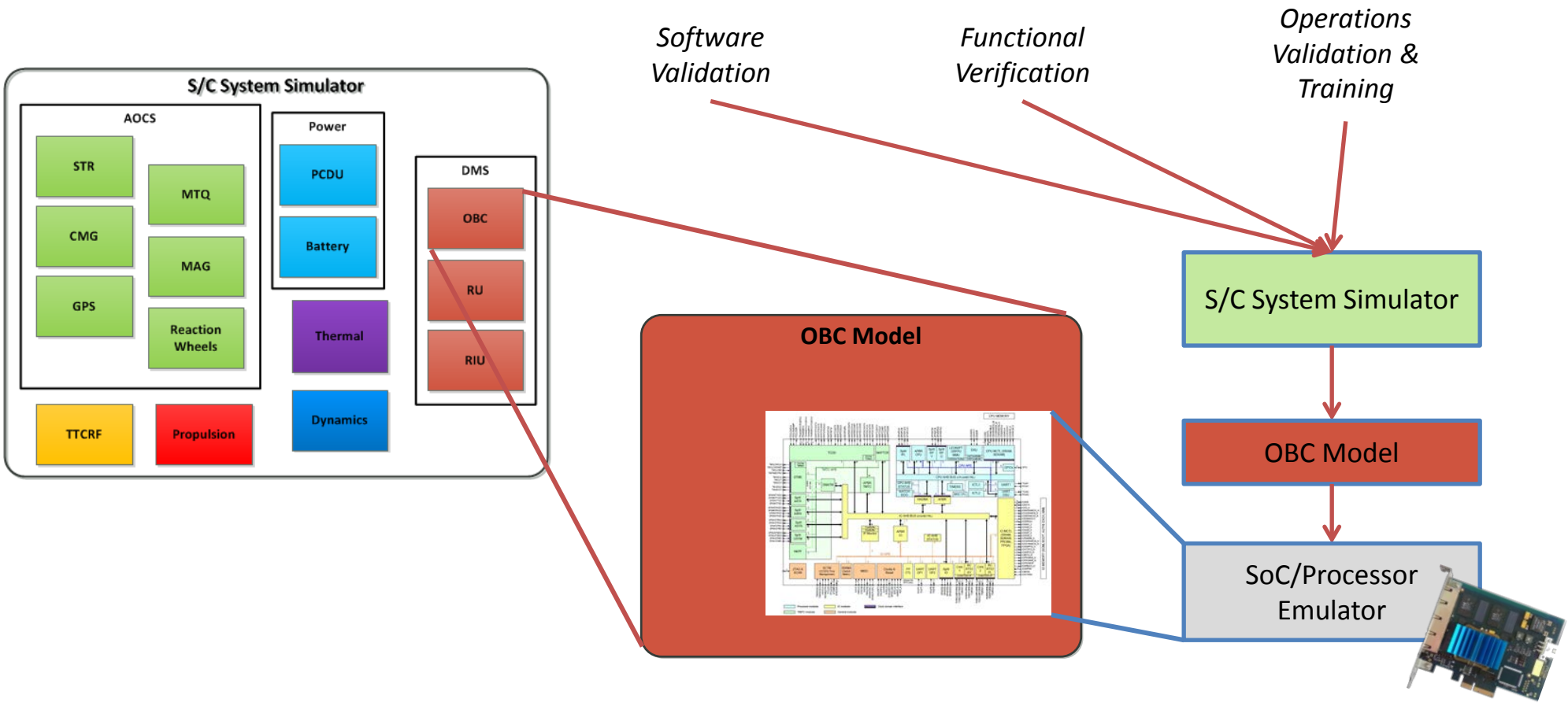
Context (1/4)

SoC/Processor emulation into Satellite simulation



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Context (2/4)

Leon Emulation Board (LEB)

- Satellite simulation in SW:
  - S/C Dynamics
  - Units
  - OBC
  - Leon peripherals

- Leon emulation in FPGA
  - Leon IP Core VHDL

    MCTL, UART, GPIO, IT,…
  - GR FPU VHDL

  → Hardware in the loop (HIL)

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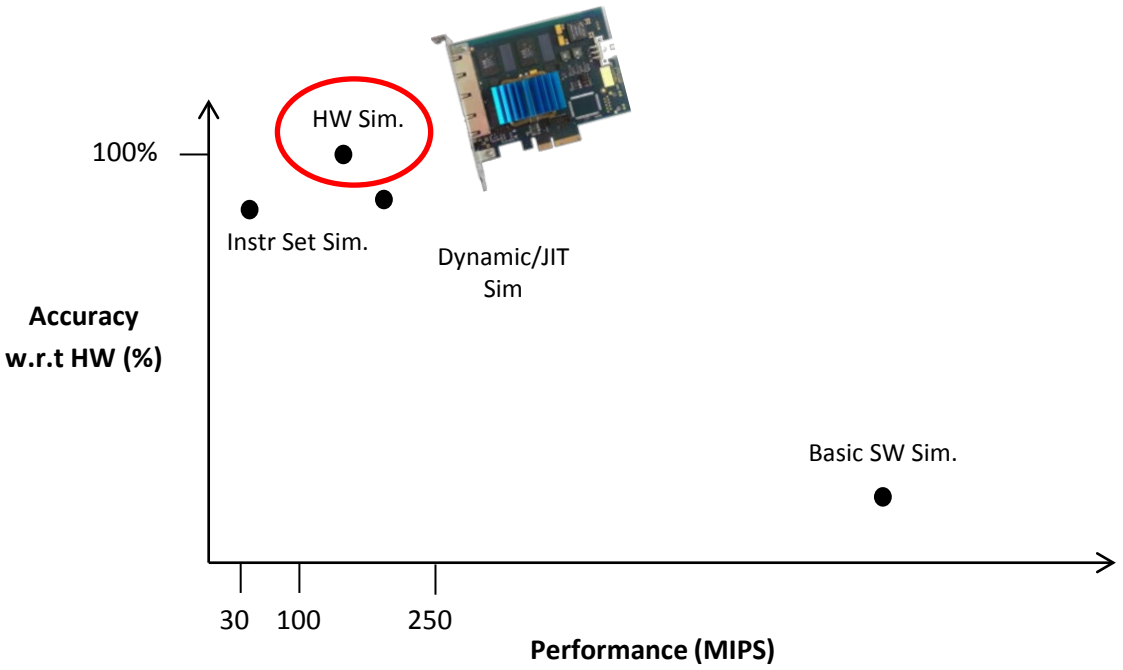
Context (3/4)

Processor/SoC emulator State of the Art

- **Facilities based on full Numerical Simulation** :
  - Instructions Set Simulator (Aeroflex-Gaisler TSIM, Airbus DS Simleon, …)
  - Dynamic Translator/ Just-in-time (SciSys QERx, Airbus DS Simleon, …)
- **Hybrid simulation with High emulation accuracy**



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Context (4/4)

Comparison between H/W and S/W emulators

Items	SW	HW	Reason
Representativity	-	+	If HW is dedicated to a target SoC or looks like it -> perfect; otherwise HW deviates from flight OBC or HW needs tailoring. SW Simulation has a limited representativity, for example : FPU, Functional blocks, Cache, Pipelines , …
Memory map	+	-	Overall memory map is frozen in HW versus flexible in SW Simulation. If real IP Core embedded in HW, its HW/SW ICD is fixed. If HW is dedicated to or looks like a target SoC -> perfect; otherwise OBSW & simulations need remapping or HW needs tailoring
Speed of FPU/Cache/MC Sync simulation	-	+	SW Sim uses FPU of host (inaccurate) or a SW library (slow). Synch IU <--> FPU fuzzy. HW 100% accurate Cache model representativity and multi core synchronization impacts performance and accuracy
Speed of LEON instructions simulation	+	+	HW faster at high CPU loading, SW faster at low CPU loading because SW Sim can skip time (e.g. wait states or power down)
Speed of Functional blocks simulation	+	-	Communication with simulated blocks : LEB : PCIe bus overhead (slow) SW Sim : internal function calls (fast)
Cost	Similar		
Leon CPU speed	+	+	Speed of SW Sim / HW emulators increases with new workstations and new FPGAs

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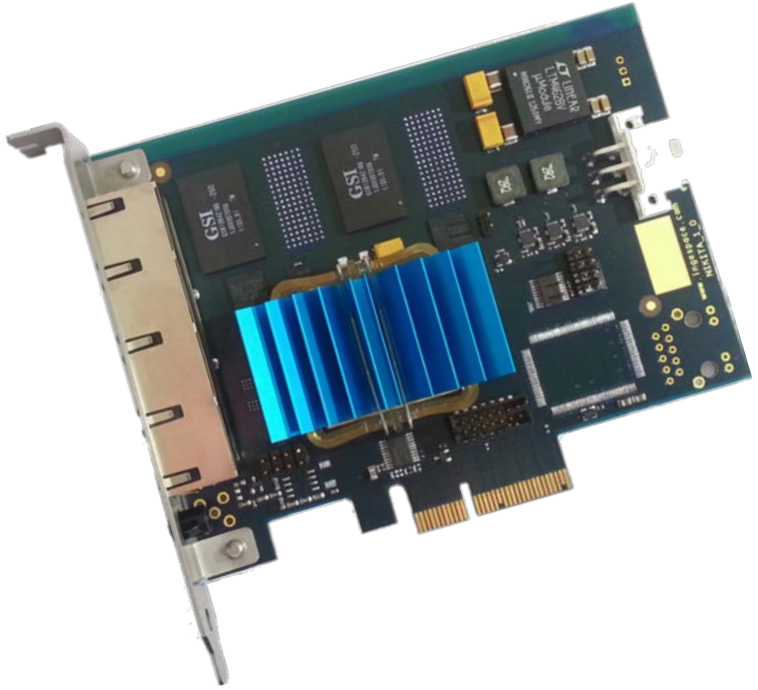
LEB Features (1/2)

- Support both LEON2 & LEON3 @ Real time OBC Simulation at 100Mhz
- 100% representative
- SoC oriented
- Simulate IP Cores on AMBA bus APB/AHB
- Based on Ingespace NIKITA Board with
  - Virtex 6 FPGA & PCI Express x4 Gen1
  - 32 Mbytes of SRAM with 0 wait states
  - 64 Mbytes SDRAM



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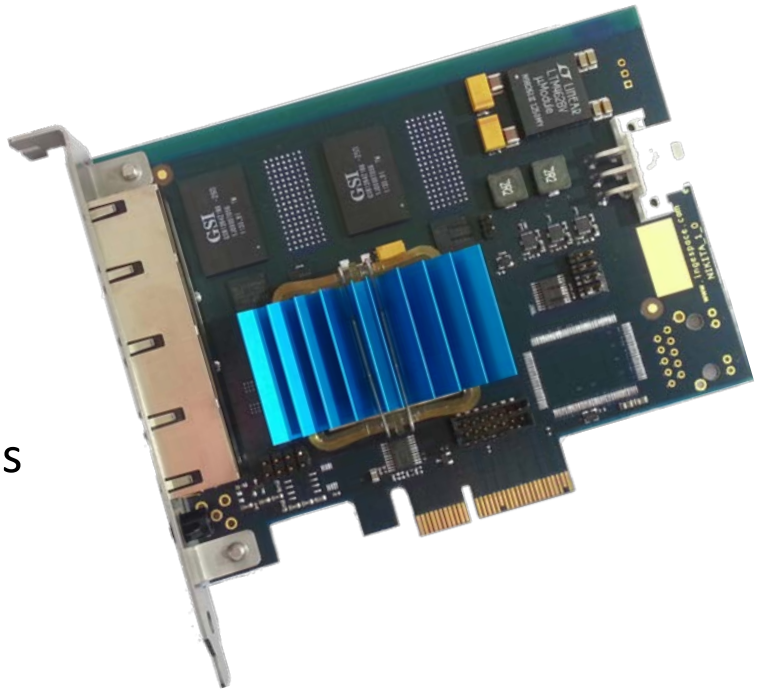
LEB Features (2/2)

Available Leon Emulation Board (LEB) Configurations

- LEB for ATMEL AT697
- LEB for Generic LEON3
- **LEB for LEON3**

  (used by Telespazio Vega characterisation activity)
  - Inspired from SCOC3 SoC by Airbus DS
  - Embedded Spacewire IP Cores & 2 Amba buses



- **New Configuration : LEB for Dual Core LEON3 SoC**
  - 2x LEON3 @ 100 Mhz
  - 2x GR FPU
  - 2x SpW IP Cores

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Principle of Operation

- Simulated Real Time counter (SRT) ←→ Leon clock
- Leon clock & SRT are suspended/frozen when:
  - OBSW accesses I/O
  - OBSW accesses AMBA where no IP Core is present in FPGA
  - SoC Tx/Rx a SpW packet / UART character / toggles PIO pin
  - Simulation Time Events expires
- LEB calls back simulation SW via the PCI express bus (comm overhead)
- Simulation SW do their work:
  - provides data to / retrieves data from SoC (I/O, AMBA, RAM...)
  - Raise interrupts…
- Leon clock & SRT are resumed and so on…

Part 2
Characterisation by Telespazio-Vega

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Part 3
Multicore Prototype

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Multicore Design Overview (1/4)

New Multicore Configurations

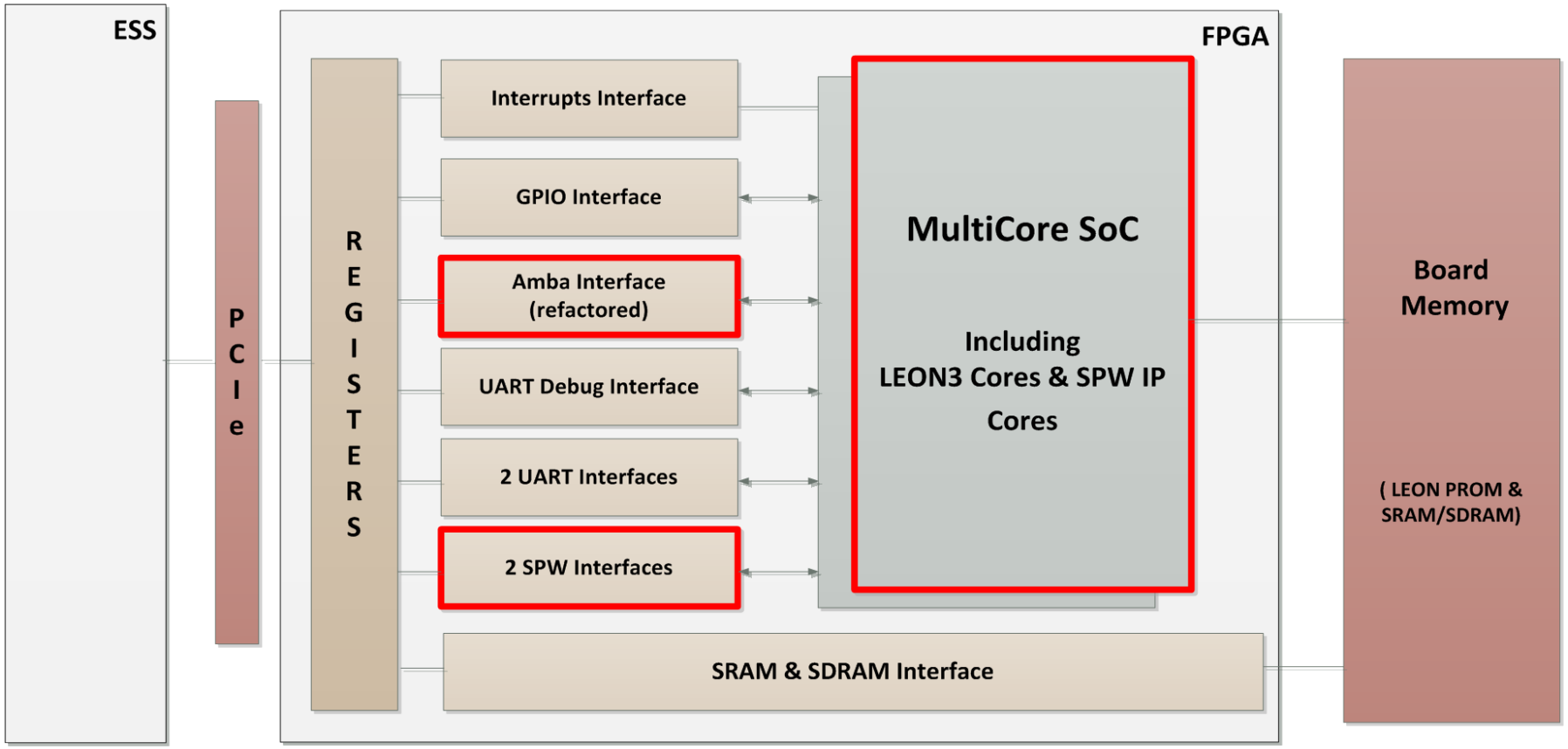
LEON2 Product Line Configuration	LEON3 Airbus DS SCOC3-inspired configuration	LEON3 Product Line Configuration
- Leon2FT@100Mhz - GRFPU	- Leon3@100Mhz - GRFPU - SpW Links - 2 Amba buses	- Leon3@100Mhz - GRFPU

- SRAM & SDRAM Support
- Fast simulation of I/O mapped memories
- SW Simulation on I/O and AMBA bus (APB and AHB)
- LEON UART characters ←→ Simulation SW
- LEON pins ←→ Simulation SW

- Scheduler and Timed Events
- GDB Server
- Save and Restore of simulation contexts
- API TSIM compliant
- Runs in Eurosim, SimTG on 32-bit RedHat and SIMSAT on 64-bit SUSE

Multicore Design Overview (2/4)

Design Configuration Overview



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Multicore Design Overview (3/4)

Focus on Multicore System On Chip Configuration

- **2 LEON3 IP cores** with dedicated MMU configured to fit GR712 LEON3 cores configuration
- **2 GRFPUs**, one per core

- Shared IPs :
  - 1 shared DSU IP Core to manage both core with DSU UART
  - 1 shared IRQMP configured to manage the 2 Cores IT and wake up function
  - All other LEON3 product line IP Cores (MCTL, GPTIMER, GPIO)

- Embedded Links :
  - 2 SPW IP Cores linked to 2 SPW cradle bridges
  - 2 APB UART IP Cores linked to 2 UART cradle bridges

- All LEON3 product line cradle modules including **new Amba master module** and **updated SPW module**

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Multicore Design Overview (4/4)

Focus on Memory Mapping Configuration

- **Based on GR712RC SoC Memory Mapping**
- **All IP are shared by both Cores**

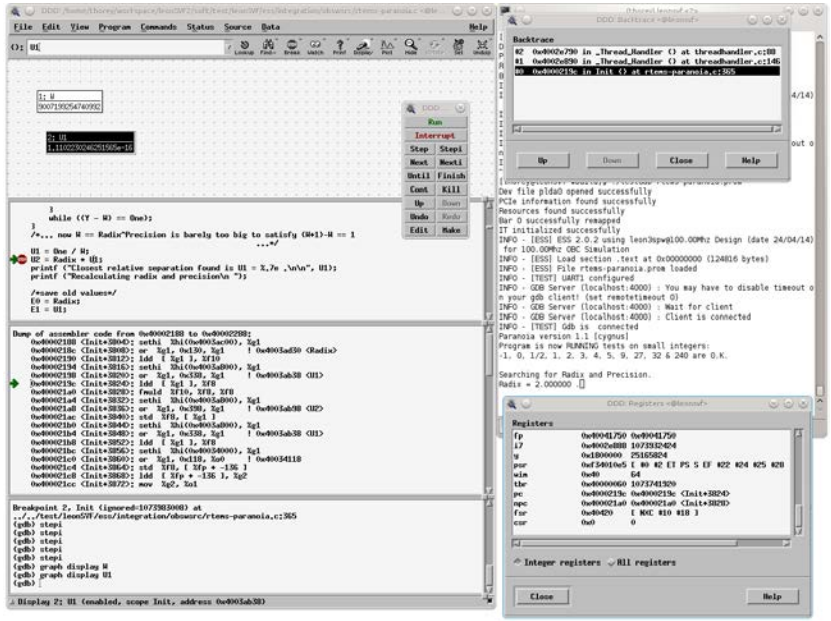
Embedded IP Cores (DSU, IRQMP, SPW,…)

Connection of Simulated APB IP Cores

Connection of Simulated AHB IP Cores using new Amba Master Module

Start Address	Denomination	Suspend on OBSW read/write access	Same as GR712RC
0x00000000	PROM CS0 (4MB)	No	Partially
0x10000000	PROM CS1 (4MB)	No	Partially
0x20000000	IO (2*4MB for 2 exclusion areas)	Yes	Partially
0x40000000	RAM (16MB) & SDRAM(64MB)	No	Partially
0x80000000	MCTRL	No	Yes
0x80000100	APBUART 1	No	Yes
0x80000200	IRQMP	No	Yes
0x80000300	GPTIMER	No	Yes
0x80000400	APBUART 2	No	No
0x80000500	APB SLAVES	Yes	No
0x80000700	AHB UART (Debug)	No	Yes
0x80000800	APB SLAVE	Yes	No
0x80000900	GRGPIO	No	Yes
0x80000A00	SPW IP CORE 1 APB	No	No
0x80000B00	SPW IP CORE2 APB	No	No
0x80000C00	APB SLAVES	Yes	No
0x80000F00	AHB Status	No	Yes
0x80001000	Not mapped	No	Yes
0x800FF000	APB PnP AREA	No	Yes
0x80100000	Not mapped	No	No
0x90000000	DSU	No	Yes
0xA0000000	SPW IP CORE 1AHB	No	N/A
0xB0000000	SPW IP CORE 2AHB	Yes	N/A
0xC0000000	AHB SLAVES	Yes	No
0xFF000000	AHB PnP AREA	No	Yes

Multicore New Features (1/2)



- **Reused and adapted Features to Multicore :**
  - **GDB Server** allows to debug the OBSW Breakpoint, patch & dump memory, Ctrl-C management (limited to 1 core management)
  - **Spacewire** Packet transfers
  - **Embedded Scheduler**
  - **I/O & Amba Simulations** interfaces
  - **Save and Restore** adapted to manage both cores

New Features support :

- **New Amba Master** to enhance Amba transfer representativity and efficiency
- **Additional Spacewire** Suspends to support unlimited packet size

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Multicore New Features (2/2)

Focus on the new Amba Master module

- **More representative access + efficiency on AHB Amba bus by Simulated IP Cores**

Example : A SPW Simulated IP Core want to write 1 packet of 45 words into LEON3 SRAM

- **Solution 1 on old Implementation :**

Step 1 : steal 1 cycle on Amba Bus
Step 2: Store data into SRAM via ESS patch
Step 3: time event of 20 AMBA cycles until next transfer
Goto step 1 for 45 times

Problems: slow simulation and Leon cache not updated

- **Solution 2 on old Implementation :**

Step 1 : steal 45 Amba Bus cycles
Step 2: Store data into SRAM via ESS patch

Problems: not representative, Leon cache not updated

- **Using new Implementation :**

The AMBA Master Simulation Block (VHDL) manages all 45 words of a data block via AMBA to the memory and the gaps between them. This requires only 1 interaction between ESS and FPGA over the PCI bus.

Advantages:
- Representativity, speed, cache updated

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Qualification & Performance (1/3)

Qualification : Functional check

- **Multicore Test using Picture Processing multicore OBSW – CPU load intensive, uses FPU**
  - Output : 2 matrix with processing results
  - Results have been compared to matlab reference (green cells means equals to matlab results)

	leonSVF results X :											
	0	1	2	3	4	5	6	7	8	9	10	11
0	0	0	0	0	-0,0272425	-0,02383679	-0,05996602	0,01450059	0	0	0	0
1	0	0	-0,03796626	-0,08027391	-0,14500986	-0,05829088	-0,00698274	-0,08474018	-0,12258804	0,02331212	0	0
2	0	-0,00556938	-0,04224532	-0,14677045	-0,06824593	-0,09725637	-0,05554496	-0,07421988	-0,04691166	-0,00525214	0,03122422	0
3	0	0,03929284	-0,14258643	-0,11586312	-0,08742855	-0,15113171	-0,08091272	-0,04469322	-0,03932942	0,01961895	-0,052892	0
4	-0,05876434	-0,02114767	-0,1277496	-0,02240873	-0,1024	0	0	-0,01383479	-0,08567739	-0,11215178	0,0070408	-0,01837351
5	-0,02920584	-0,10785595	-0,12440335	0,02572675	0,03792246	0	0	-0,09474247	0,05155893	-0,02174176	-0,05676809	-0,00531103
6	0,00774245	0,05411035	-0,00613514	0,01362586	0	0	0	0	-0,0111724	0,01531424	-0,01580577	-0,03488355
7	-0,01579601	-0,00433848	-0,02616506	0,03302502	0,06654145	-0,12589774	0,0088163	0,04528931	0,01827775	-0,07175049	0,04717768	-0,057357
8	0	-0,04131199	-0,052969	-0,05423346	-0,01286214	-0,11710246	-0,07781	-0,04005313	-0,14603582	-0,04382784	-0,1125848	0
9	0	-0,08256921	0,01684842	-0,0003744	-0,03994603	-0,08760989	-0,09755418	-0,120765	-0,18261248	-0,07322775	-0,03283646	0
10	0	0	-0,097423	-0,06416837	-0,01359759	-0,11452549	-0,13430024	-0,07918	-0,14560232	-0,16304451	0	0
11	0	0	0	0	-0,0818721	0,00532785	0,02210423	0,05977169	0	0	0	0

	leonSVF Results Y :											
	0	1	2	3	4	5	6	7	8	9	10	11
0	0	0	0	0	-0,108583	-0,17416807	-0,12044843	-0,12787156	0	0	0	0
1	0	0	-0,11007495	-0,11568485	-0,07226207	-0,18394333	-0,18708636	-0,07927127	-0,15229483	-0,11134124	0	0
2	0	-0,11464847	-0,15384806	-0,20272148	-0,17251831	-0,15149958	-0,15449524	-0,15435054	-0,16258147	-0,12556169	-0,13481885	0
3	0	-0,08356385	-0,12215087	-0,23166267	-0,15860848	-0,16332288	-0,15198888	-0,15330923	-0,06244015	-0,11842387	-0,06612077	0
4	-0,05204692	-0,11707801	-0,1346038	-0,15443101	-0,1824543	0	0	-0,16621055	-0,15410979	-0,08076708	-0,09868997	-0,14387665
5	-0,19326762	-0,10202931	-0,14258695	-0,16598077	-0,17626868	0	0	-0,197654	-0,15512287	-0,12935411	-0,12901525	-0,20049166
6	-0,16486876	-0,20751598	-0,12314378	-0,12361083	0	0	0	0	-0,08643284	-0,08418692	-0,05130667	-0,15068841
7	-0,17114693	-0,16387874	-0,15952946	-0,19642709	-0,11596622	-0,11256862	-0,11732335	-0,18390609	-0,15663847	-0,09347397	-0,08493775	-0,14863227
8	0	-0,021853	-0,1559001	-0,11879797	-0,29651267	-0,16733608	-0,22702176	-0,19161416	-0,13359679	-0,18921407	-0,22769614	0
9	0	-0,08393033	-0,1090465	-0,20144373	-0,06733987	-0,16596282	-0,13144269	-0,17705703	-0,15826433	-0,12837961	-0,08664152	0
10	0	0	-0,10710601	-0,07549905	-0,1889309	-0,24242131	-0,20183501	-0,23175234	-0,18081079	-0,18822154	0	0
11	0	0	0	0	-0,20983324	-0,15660614	-0,0954474	-0,10019037	0	0	0	0

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Qualification & Performance (2/3)

Qualification : Processing duration (OBSW time)

- **Algorithm execution time comparison between 3 targets:**
  - LEB running at 100Mhz
  - AIRBUS DS Simleon Dynamic JIT multicore emulator configured at 100Mhz
  - ALTERA DE4 FPGA board with LEON3 PROXIMA Multicore design by Cobham running at 80Mhz (based on GR712RC). Durations below are scaled to 100Mhz to enable comparison.

	Duration (in us) on leonSVF board	Duration (in us) on Simleon	Duration (in us) on ALTERA board
Algo Part 1 (Coarse Offset)	300 248	268 390	356 382
(Algo Part2) Fine Offset	227 034	222 383	322 084
(Algo Part2) Building Reference	86 840	88 439	100 820
Total	**666 001**	**631 082 (-5%)**	**800 811 (+17%)**

ALTERA board and LeonSVF board have different types of SDRAM chips.
SimLeon has a generic timing of the memory which is not characterized against either HW boards.

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Qualification & Performance (3/3)

Performance

- **Algorithm execution duration comparison between 3 targets:**

	leonSVF Board	AIRBUS DS Simleon JIT	ALTERA board
Processing duration (OBSW point of view)	666 ms	631 ms	801 ms
Processing Real Time duration	675 ms	-	801 ms
Speed Factor	**0.98**	**< 1.0***	**1.0**

** Simleon timing measurements are not relevant for now. Concurrent memory accesses under optimization*
Performance is very dependent on emulator parametrization (e.g synchronization period, …)

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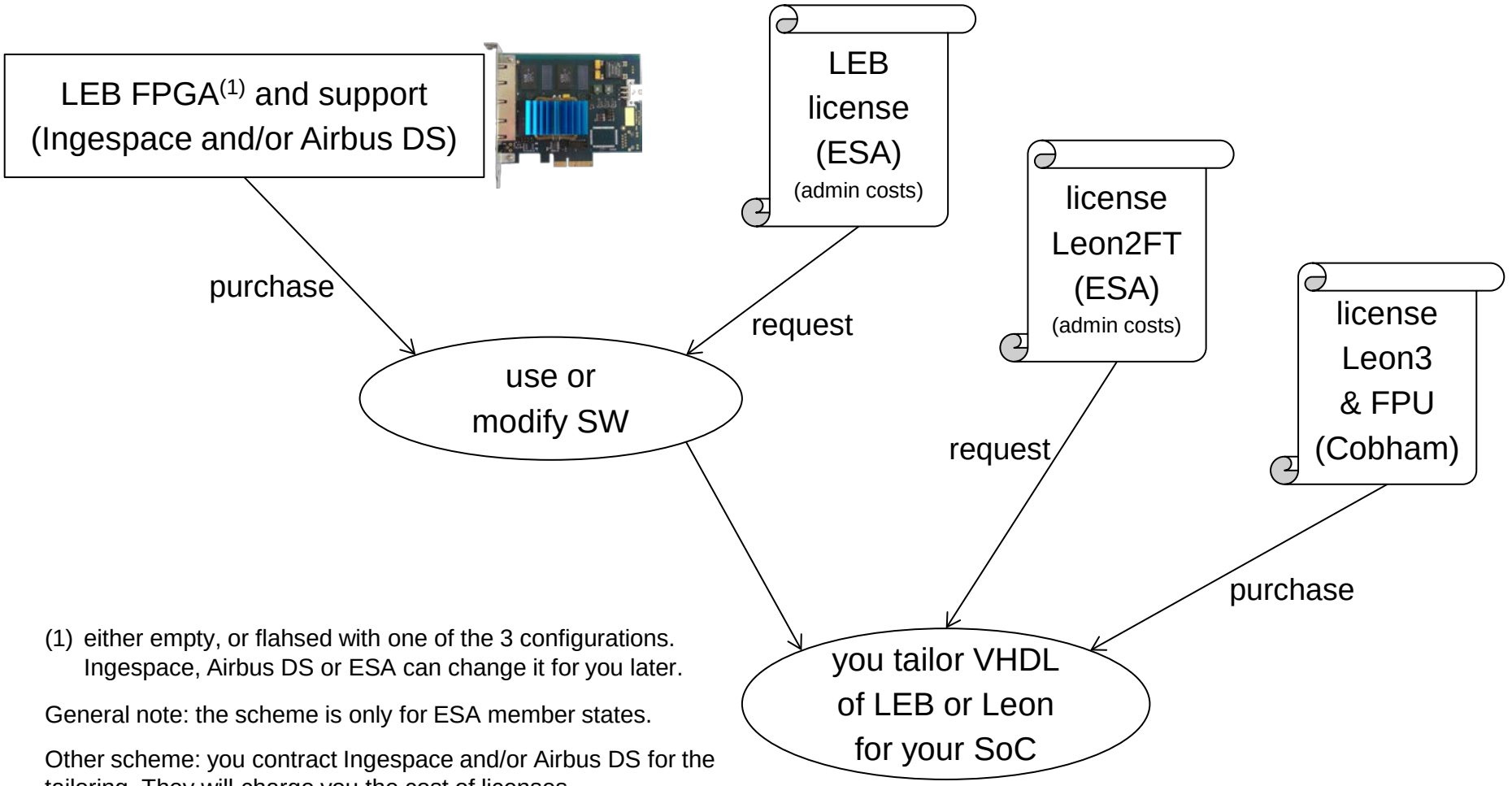
Lessons learned

- **Cores Initialization**
  - Bdinit function (used by Gaisler Mkprom) have been adapted
  - DSU and IRQMP additional initialization to do

- **RTEMS Multi core support**
  - Compilation process have been updated to support leon3smp BSP
  - No documentation on BSP during multicore initialization Issues debugging

- **Limited GDB debugging**
  - ESS GDB server don’t support multicore specific GDB commands
    - Future enhancement

How to get an LEB



(1) either empty, or flahsed with one of the 3 configurations. Ingespace, Airbus DS or ESA can change it for you later.

General note: the scheme is only for ESA member states.

Other scheme: you contract Ingespace and/or Airbus DS for the tailoring. They will charge you the cost of licenses.

Conclusion

LEB Product maturity has been demonstrated

- Implementation of new multicore configuration easy thanks to reusable blocks
- Multi-cores configuration running at 100 Mhz

Limitation

- Simulation representativy limited by the LEB hardware (memory chips, buses number)
- Tailoring leonSVF hardware (e.g memory chips) is harder than on SW emulator

Enhancement

- Add support for specific GDB command for multicores in the ESS
- New SoC Configuration…

Thank You for your Attention

Any Questions ?

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