LeonSVF Multicore prototype for Leon3

The key component of the LeonSVF is the Leon Emulation Board (LEB), a reusable building block for Software Validation Facilities and System Simulators of satellites based on Leon2 and Leon3 Systems on Chip (SoC). The current CCN#3 of the project “OBC Simulator Architectures and Interfaces to System Test Benches” has produced a multicore configuration of the LEB with 2xLeon3 + 2xGRFPU.

The multicore LEB provides a combined level of accuracy and performance that cannot be provided anymore by any kind of software simulations (instruction set or block-oriented simulators) thanks to the execution of the VHDL of the Leon IP Core and the other IP Cores of the target System on Chip.

The LEB is a PCIe board with an FPGA which executes the actual Leon VHDL code thus enabling cycle-accurate execution of the Leon3 dual core at 100MHz minus simulated I/O load overheads. The LEB is designed for Linux workstations and is controlled via an API compatible with TSIM by Cobham-Gaisler. The key mechanism of the LEB is that whenever simulation events trigger from any Leon IP core (I/O or AMBA access, timed events etc), the clock to the whole SoC is suspended to keep time representativity for the on-board software (OBSW) while the simulations execute. The synchronisation between the cores is implicit in the VHDL execution, whereas a software-based CPU emulation would either have a level of inaccuracy or a performance penalty, like also MMU, caches and FPU simulation.

At present 4 configurations of the LEB exist: 1) for the Atmel AT697; 2) for a generic Leon3; 3) for a Leon3 SoC inspired from the SCOC3 SoC by Airbus DS and which embeds the Spacewire IP Cores; 4) dual core SoC with 2xLeon3 + 2xGRFPU and 2 Spacewire IP Cores.