Schedulability Analysis Techniques and Tools for Cached and Multicore Processors

Modern real-time embedded systems combine complex functionality together with stringent timing requirements. In the space industry, the on-board software has to efficiently utilize the processor resources, while retaining certain predictability guarantees through the application of proper schedulabitily analysis. These challenges can be attained only within a coherent design flow that adopts the principles and the requirements of space software engineering standards such as ESA's ECSS-E-ST-40C. However, the emerged multi-core processor platforms utilize various performance enhancing features that are associated with new sources of unpredictable behaviour. New requirements for soft real-time constraints, mixed-criticality levels, time/space budget and WCET analysis have to be addressed. This raises the need of a rigorous design approach to ensure the expected predictability guarantees and the need to reconsider the existing industrial practice and standards, while using an industrial-strength tool-chain for model-based software development.

The MoSATT-CMP project introduces a rigorous model-based design flow grounded on a multi-core aware model of computation called Fixed Priority Process Networks. The MoSATT-CMP design flow was automated using ESA's TASTE tool-chain and model transformations to BIP (Behaviour, Interaction, Priority) a timing-aware formal concurrency modelling language that supports schedulability analysis and scheduling code generation. Parts of the design flow utilize an innovative measurement-based statistical WCET analysis and an automated instruction code evaluation of the performance of the possible task allocation and shared-cache configuration alternatives, to detect potential interference bottlenecks. We employ flexible scheduling policies that take into account task allocation and mixed-criticality considerations, with respect to the target platform's computational resources. Finally, we provide results that demonstrate the effectiveness of our approach through the design, implementation and execution of a Guidance, Navigation and Control application by Elecnor Deimos Space on the NGMP platform (that incorporates a processor containing four LEON4FT and two FPUs with a shared L2 cache). The demonstration was performed on the NMFP (N2X platform) which implements the ESA's next-generation multi-core platform architecture.