FINAL PRESENTATION DAYS 2016

Control Loop Processor -

Platform for hard real time space applications

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S.A.B.C.A.

AGENDA

- **PERIMETER**

- **ARCHITECTURE**

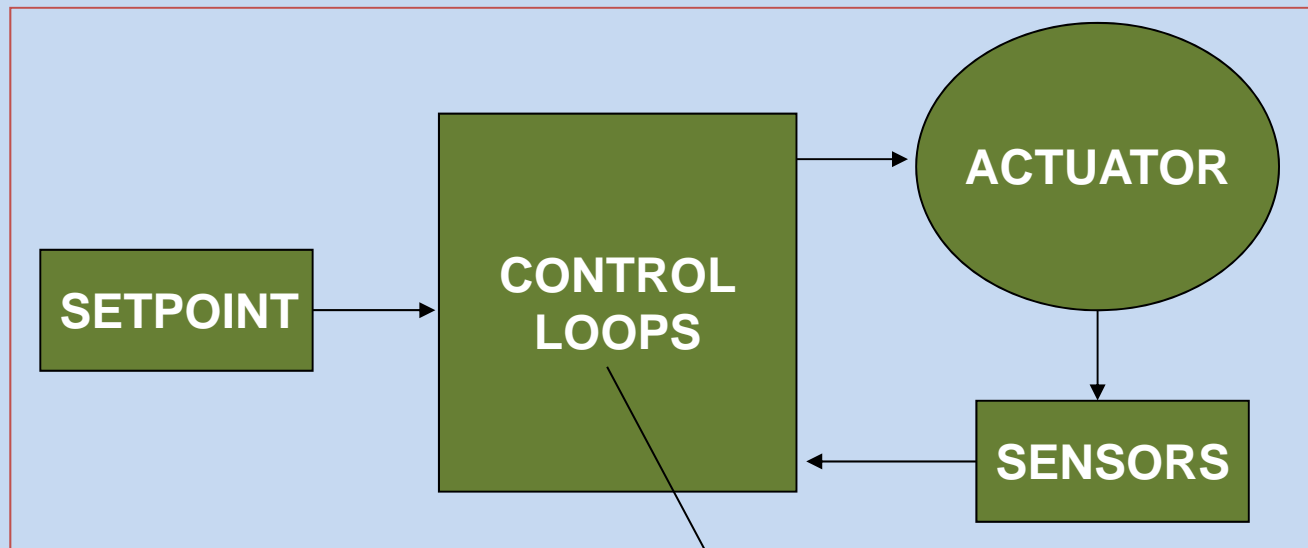- **SOFTWARE DEVELOPMENT ENVIRONMENT**

- **VALIDATION**

- **EXAMPLE OF APPLICATIONS**

- **SUMMARY**

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PERIMETER

- ## Introductive Example:

Example of VEGA TVC:

BW Loop #1 (outer loop) @ 10Hz

BW Loop #2 (middle loop) @ 100Hz

BW Loop #3 (inner loop) @ 1KHz
If sampling rate = 10xBW, execution @ 10 KHz

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PERIMETER

- **Targeted needs characteristics**

  - One to several nested control loops with tight processing constraints

  - Light to moderate interaction with equipment communication busses

  - Tight interaction with on-board interfaces (sensors, PWM…)

  - Most complex loop is often the inner one, e.g.

    +/- 1K to 10K arithmetic operations @1-10 kHz

PERIMETER

- **Limited implementation options are available for space**

  - Analog solution

    - not always feasible if loop is too complex

  - Hardwired digital logic on an ASIC/FPGA

    - Must be tailored/redesigned from mission to mission (high non-recurrent cost)
    - May be subject to ITAR

  - SW implementation on a general purpose microprocessor or DSP

    - May lead to real time issues or high cost solution

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PERIMETER

- **Towards Control Loop Processor**

  - Deterministic Behavior ASSP

  - Application programmable by SW (no OS) or intuitive interface

  - High data processing efficiency when needed

  - ITAR free solution (for ASSP at least)

  - Commercial product is targeted with Software Development Environment

  - Tolerant to radiation effects

  - Tailored CLP alternatives: tunable solutions at RTL level to fit application needs

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ARCHITECTURE

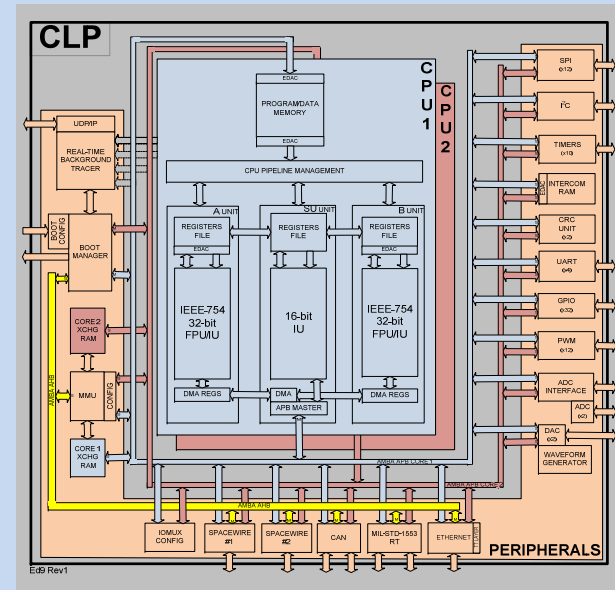# ARCHITECTURE

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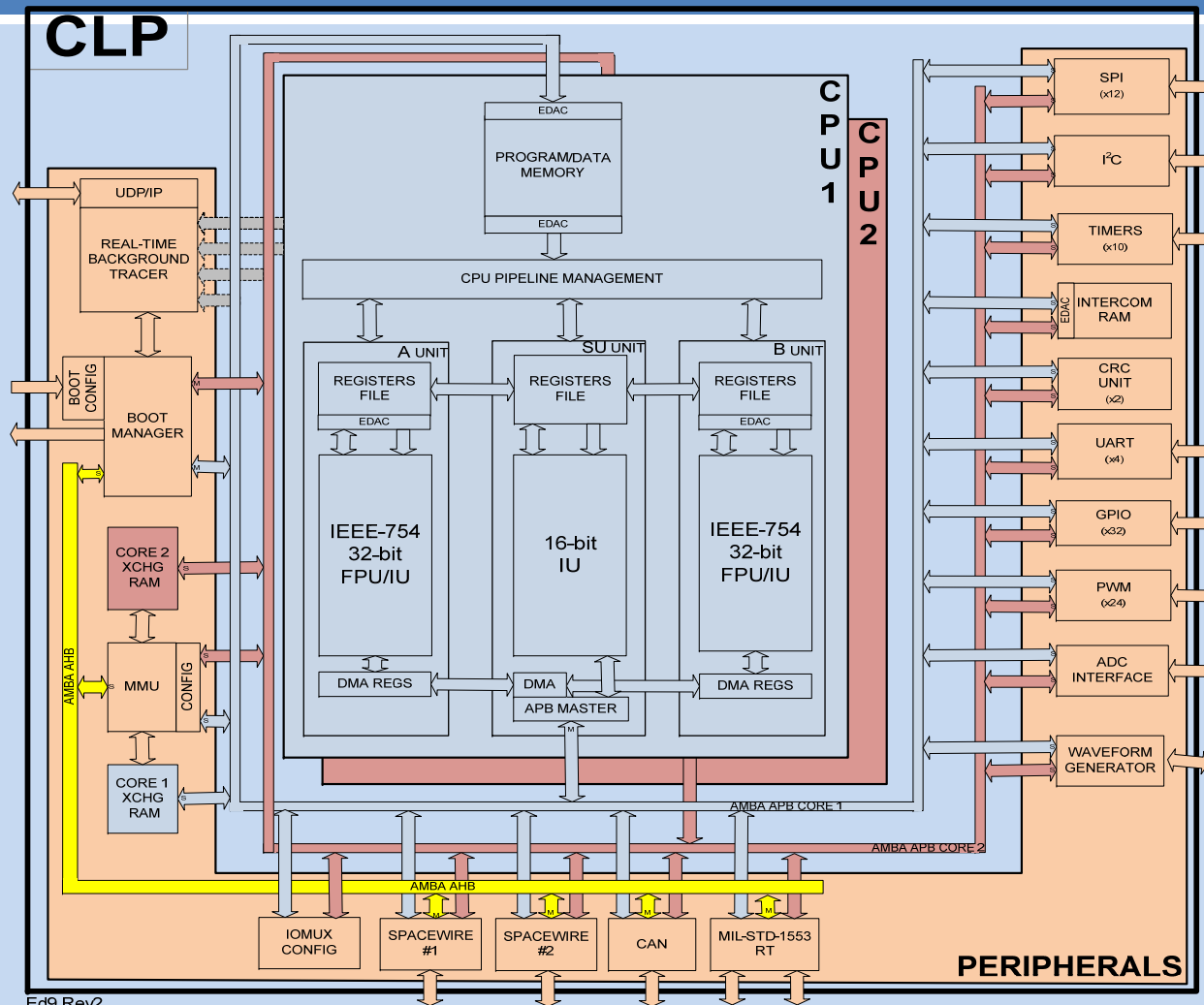
- **Dual-CPU**

  - Two-axis control or other partioning models
  - RISC architecture
  - SIMD approach
    - For complex arithmetics (vectorial control)

- **Deterministic Behaviour**

  - No caches
  - No interrupts
  - No operating system
  - I/O servicing by SW is performed by polling or DMA
    - Each I/F has dedicated or shared registers/memory with SW
    - Each I/F can work in a stand-alone fashion

- **Scheduling of SW tasks made with time slots controlled by timers**

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ARCHITECTURE

- **Two 32-bit IEEE-754 FPU per CPU**
  - Enable high dynamic data usage
  - Saturating arithmetic to avoid overflow
  - Two large register files (RGP0 to RGP511)
  - 16/32-bit integer operations are possible
- **One 16-bit IU per CPU**
  - One Register File
- **One 32768x39bits Program Memory per CPU**
  - Available for data storage if required
- **One on-chip APB peripheral bus per CPU**
  - Allocation of peripherals to CPUs is defined and fixed during boot
- **Exceptions management with counters**
 - Restart on errors can be programmed

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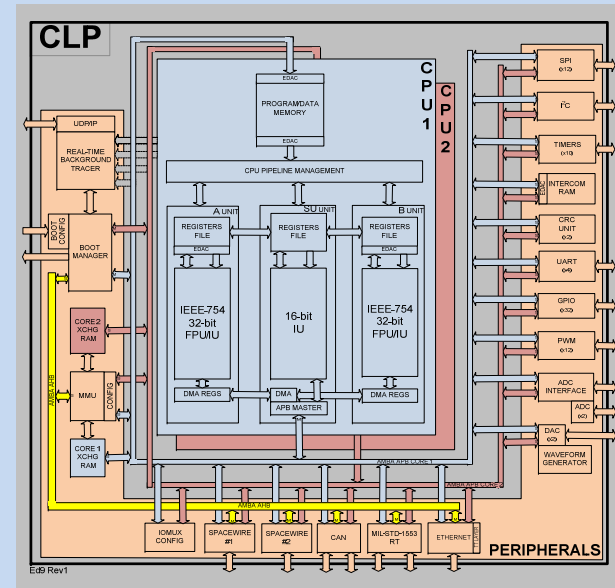
ARCHITECTURE

- **Wide range of interfaces**
  - ADC parallel interface to external ADCs
    - Configurable and autonomous
  - 2 AWG (Arbitrary Waveform Generator)
    - Useful for LDVT or resolvers excitation
  - 24 PWM
  - 2 SPI
    - master or slave
    - Up to 6 slaves per SPI
    - Autonomous behavior is also possible
  - I2C
    - Master or slave
  - 4 UART
  - 106 GPIO
    - Embeds 8-bit programmable I/F for EEPROM

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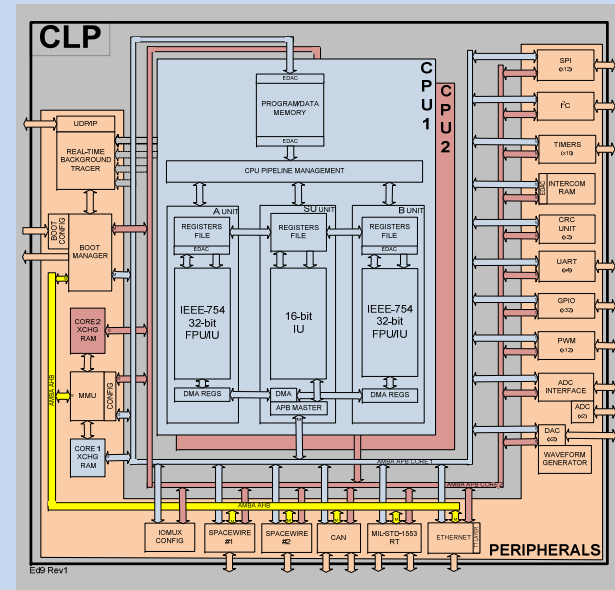
# ARCHITECTURE

- **Wide range of bus interfaces**
  - 2xSpaceWire
    - Support RMAP Protocol
  - CAN
    - Integrates redundancy management
  - MIL-STD-1553 RT
  - MMU dispatching AHB to XCHG_RAM

- **Real-Time Background Tracer (RTBT)**
  - Non-intrusive
  - real-time debugging is available

- **Booting via SpW, CAN, RTBT or 8-bit EEPROM (GPIO)**
  - 4 different boot tentatives can be programmed
  - Performs APB peripheral allocation to CPUs and peripheral initialization

- **EDAC and scrubbing management**
  - Programmable address ranges and frequency
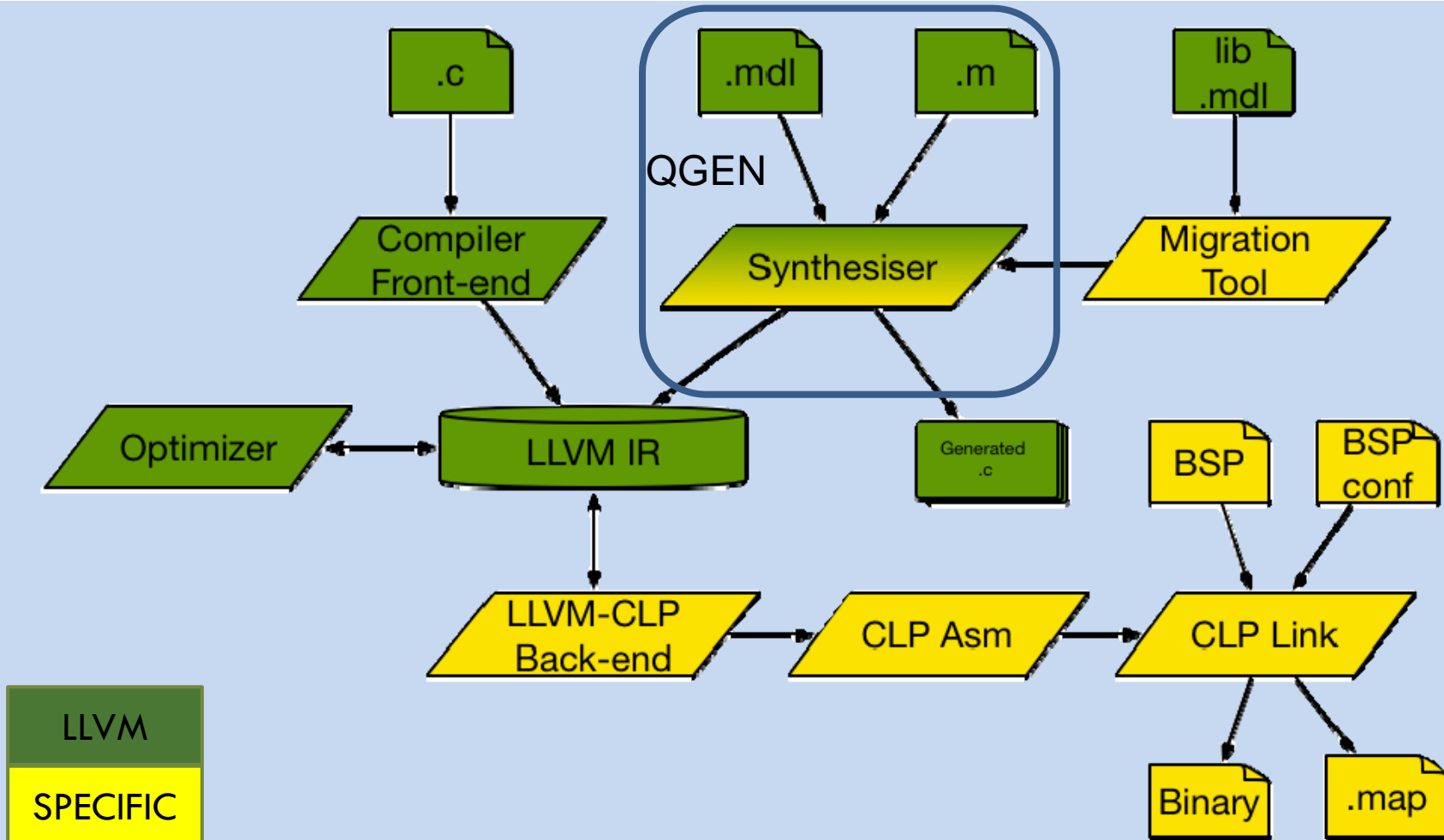
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SOFTWARE DEVELOPMENT ENVIRONEMENT

SDE
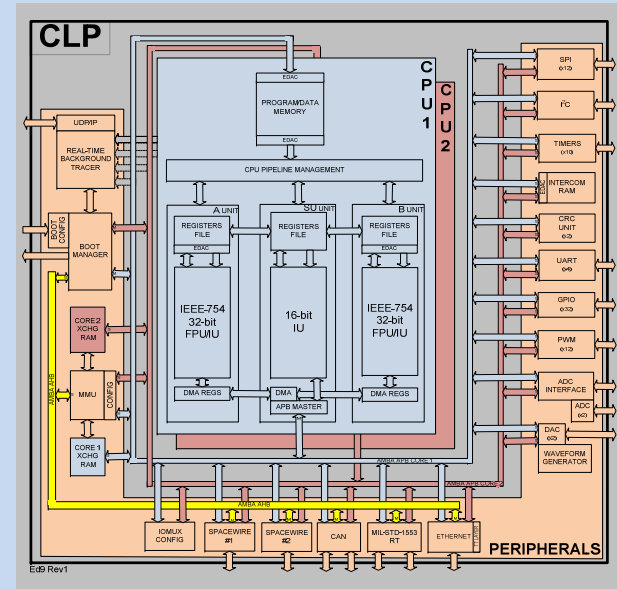
- **Assembler and Macro Library already available in preliminary version**
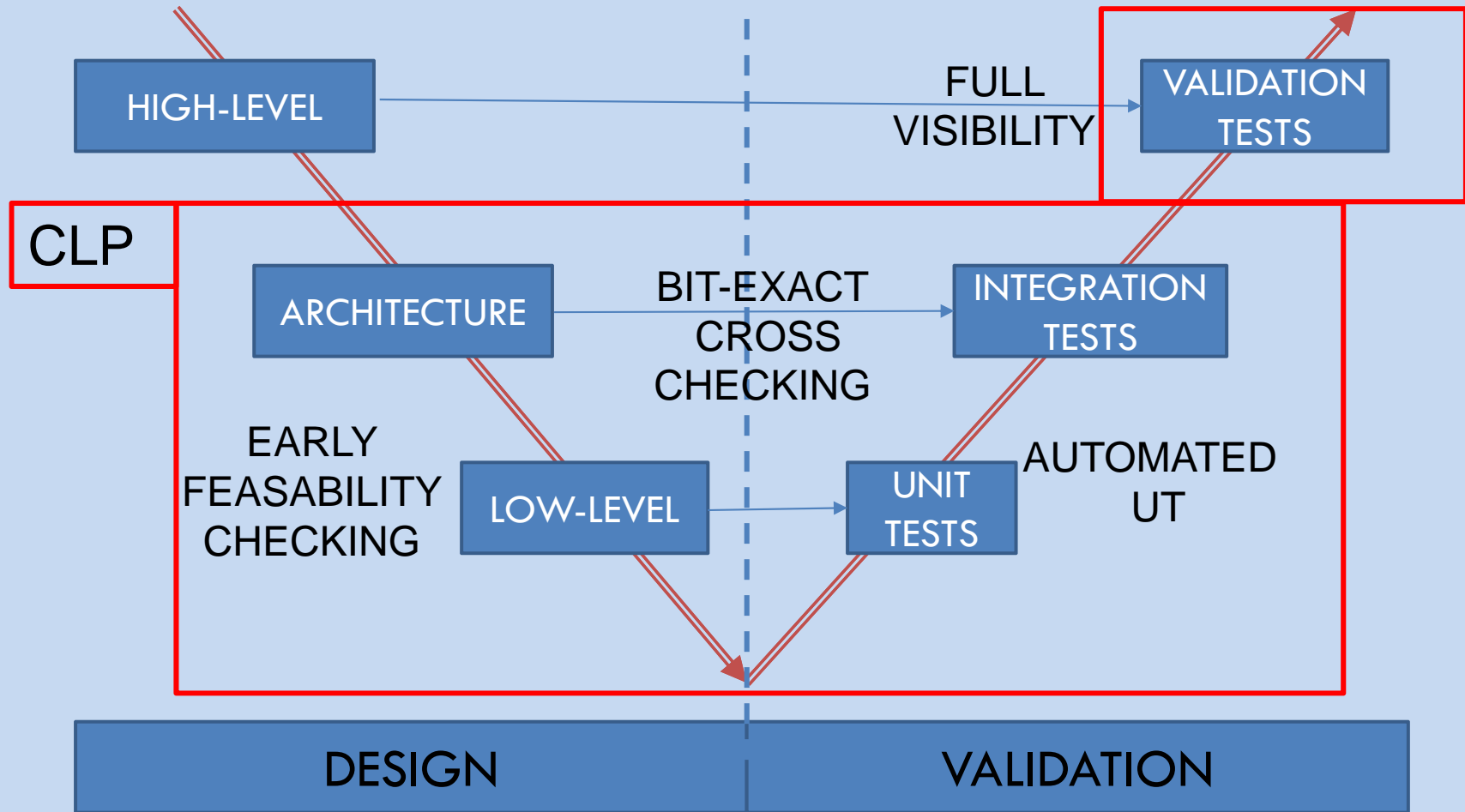
- **Spacebel (B) as main subcontractor**

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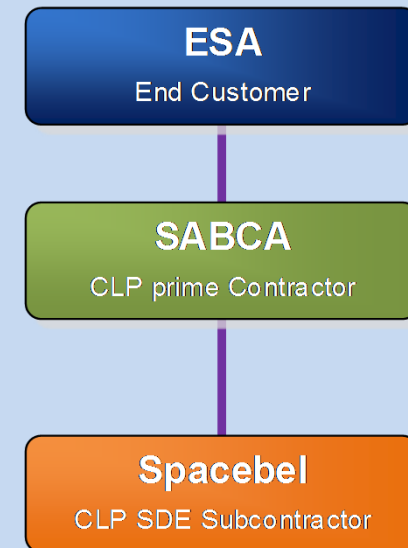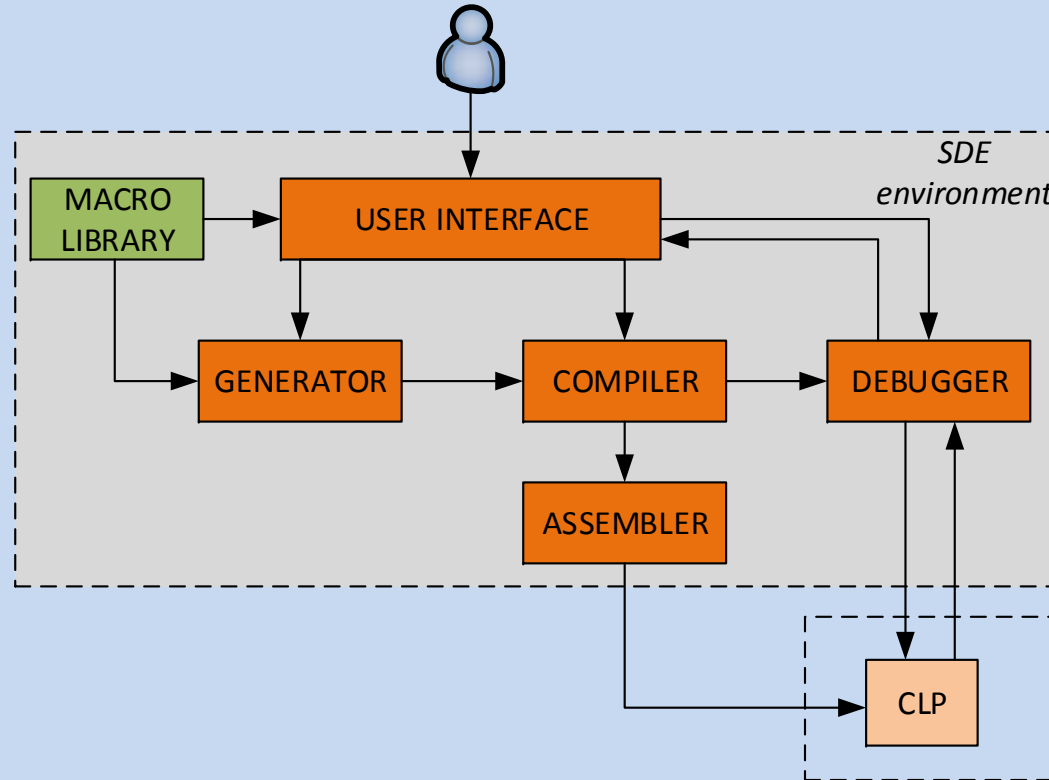
SOFTWARE DEVELOPMENT ENVIRONEMENT

- **Development Environment based on Eclipse**

- **Automatic code generation from Matlab/Simulink**
    - Based on QGEN tool (developed by ADACore)
    - Pre-defined Macro library provided for some optimized functions

- **C compiler based on LLVM**
    - LLVM supports SIMD and can extract vectorial behavior from linear code.

- **Instruction Set Simulator/Debugger**

- **Initialization Generator**

- **Real-time background tracer Manager**

- **Unit Test Manager**

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SOFTWARE DEVELOPMENT ENVIRONEMENT

CLP

HIGH-LEVEL

ARCHITECTURE

LOW-LEVEL

FULL VISIBILITY

VALIDATION TESTS

BIT-EXACT CROSS CHECKING

INTEGRATION TESTS

EARLY FEASABILITY CHECKING

UNIT TESTS

AUTOMATED UT

DESIGN

VALIDATION

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VALIDATION

VALIDATION STRATEGY

VALIDATION PLAN

Title: CLP Test Bench schematic.

Legend:
- C++
- VHDL
- TCL
- Shell Script
- Perl script
- Python script
- Text files
- Linux tool

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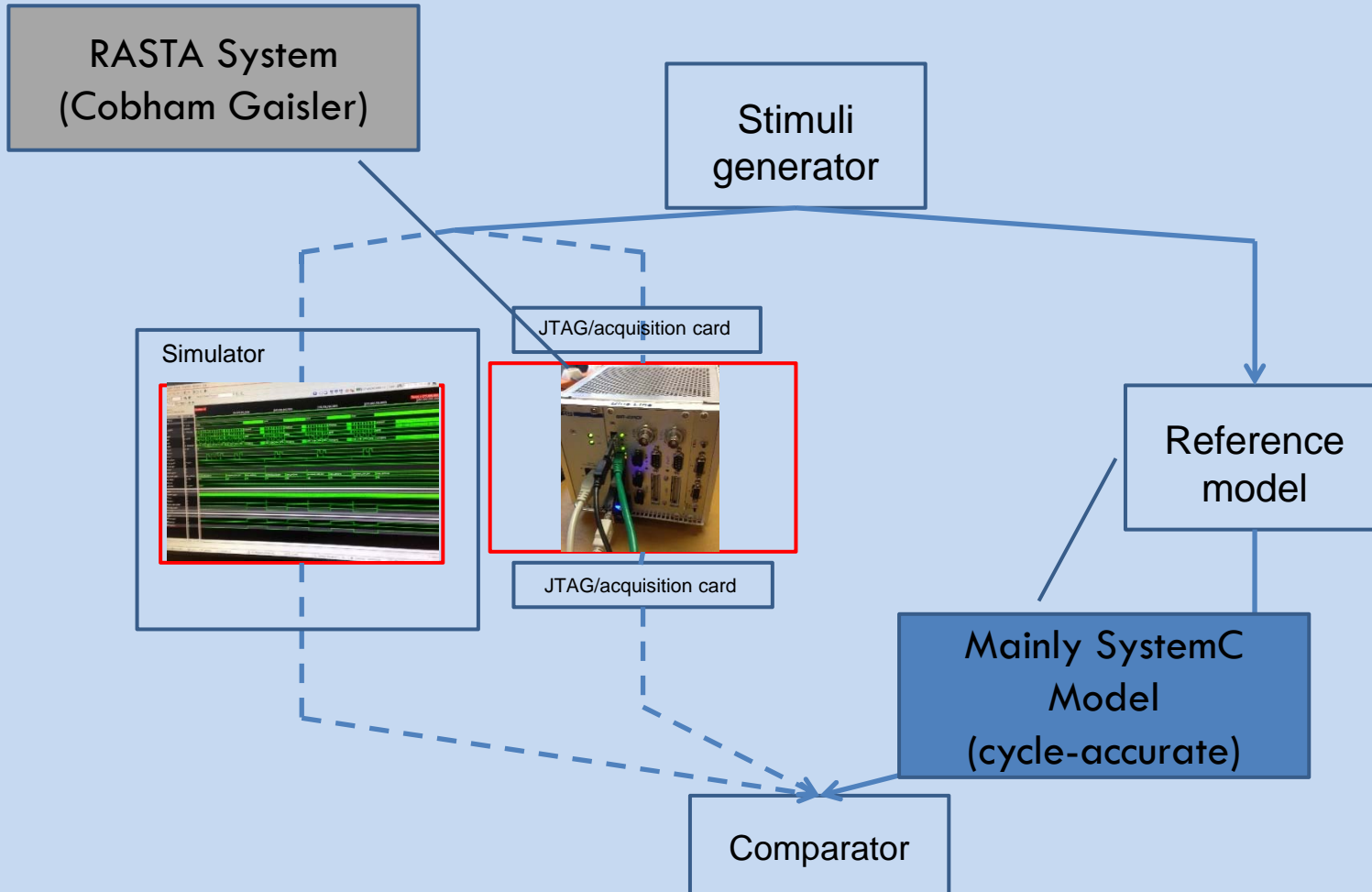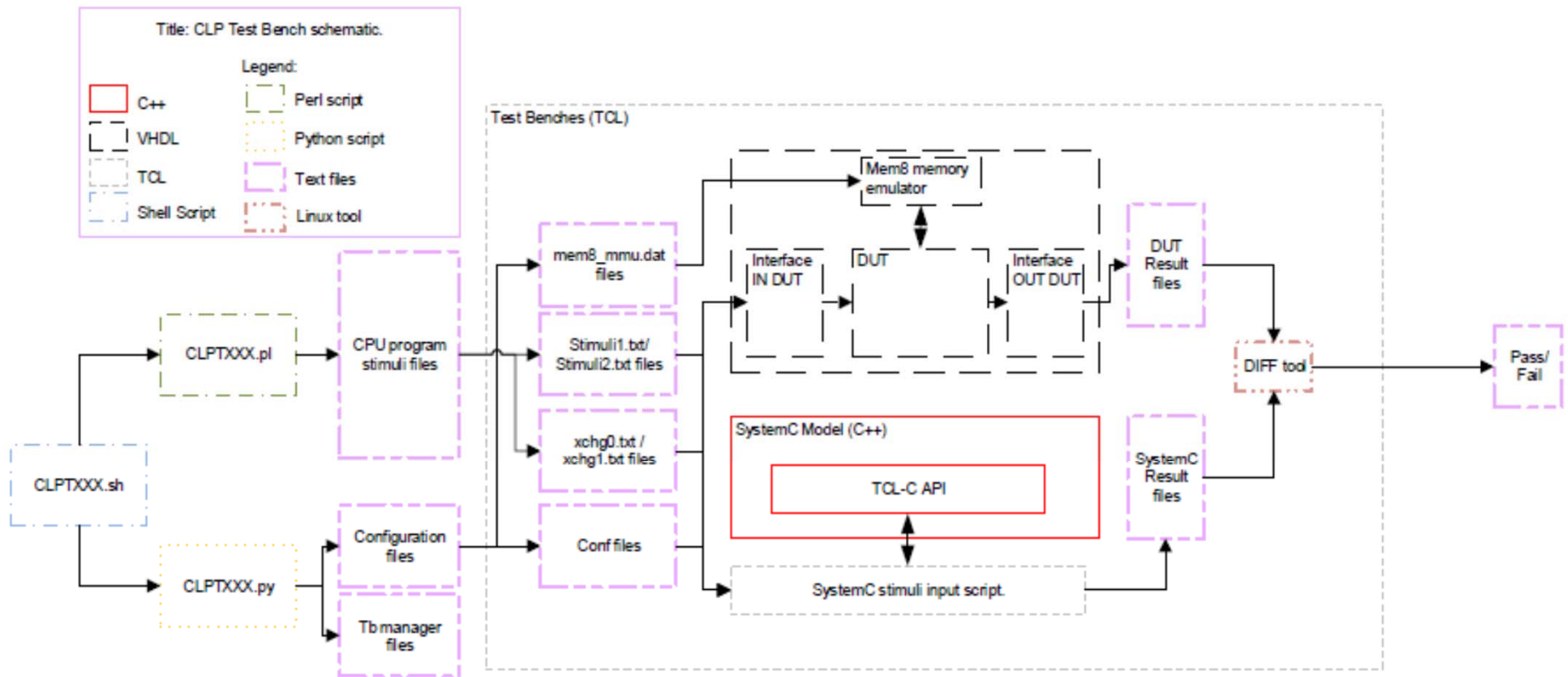
VALIDATION ACTIVITIES

- **Processor, models and testbenches complexity is high**

  - Full traceability between specification and validation plan

  - 650+ files, 140 000+ lines of code (w/ comments)

  - 700+ automated test campaigns executed around 5 testbenches

    - Pseudo-random and directed vectors

- **Unified architecture**

  - Test scenarios can be reused (with minimal effort) between simulation (RTL and post-layout) and board testing

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USE CASES

USE CASES

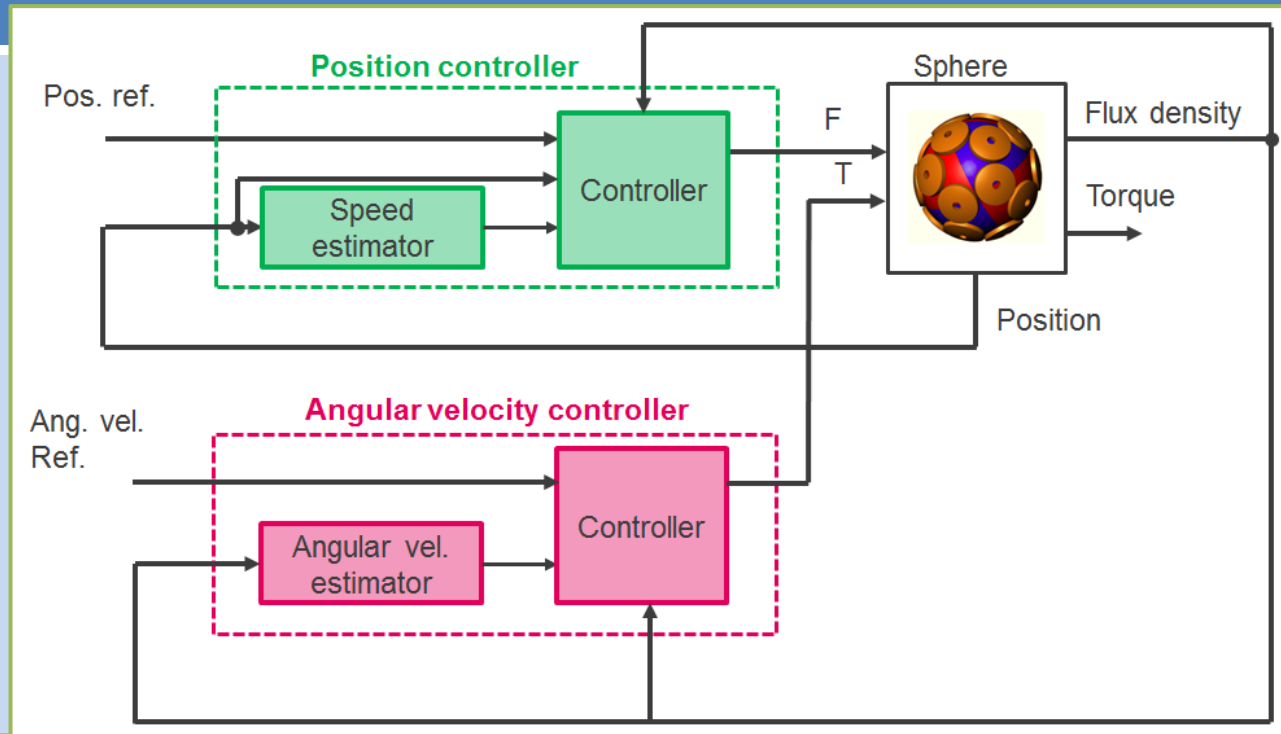- Launchers control of electromechanical actuators (VEGA-C and A6 TVC)

- Flap control systems (IXV, PRIDE)
  - IXV based on Vega Z23 upper stage

- Levitated Reaction sphere control (ELSA)
  - see next slide
  - http://elsa-project.eu/

- Rover distributed motor control

- Exo-skeleton and robotics applications in general

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EXAMPLE OF CLP APPLICATION

3 Control Loops (@ 10kHz)

- Position Loop to control levitation/centering of the rotor in the stator
- Angular velocity Loop
- Current loops (@ 100 kHz)

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EXAMPLE OF CLP APPLICATION

- **TASK#1**: **3 torque setpoints and bus management @ 10Hz**
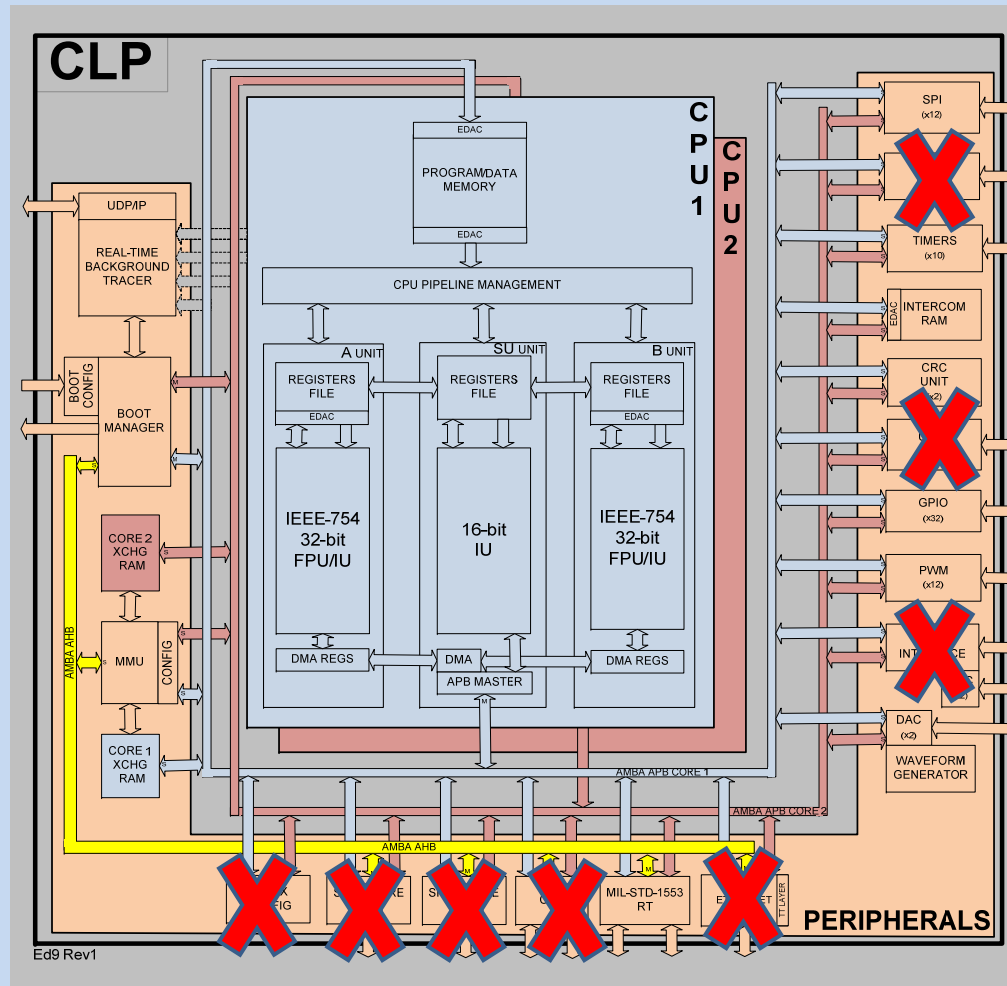   - acquisition from MIL-STD-1553

- **TASK#2**: **3 position and 7 flux sensors @ 10 kHz**
    - acquisition and post-processing

- ***TASK#3**: Main Control Loop @ 10 kHz*
    - *4000 to 5000 Floating-point operations required*
    - *Up to 50 MFLOPS are required*

- **TASK#4**: **20 Current Loops @ 100 kHz**
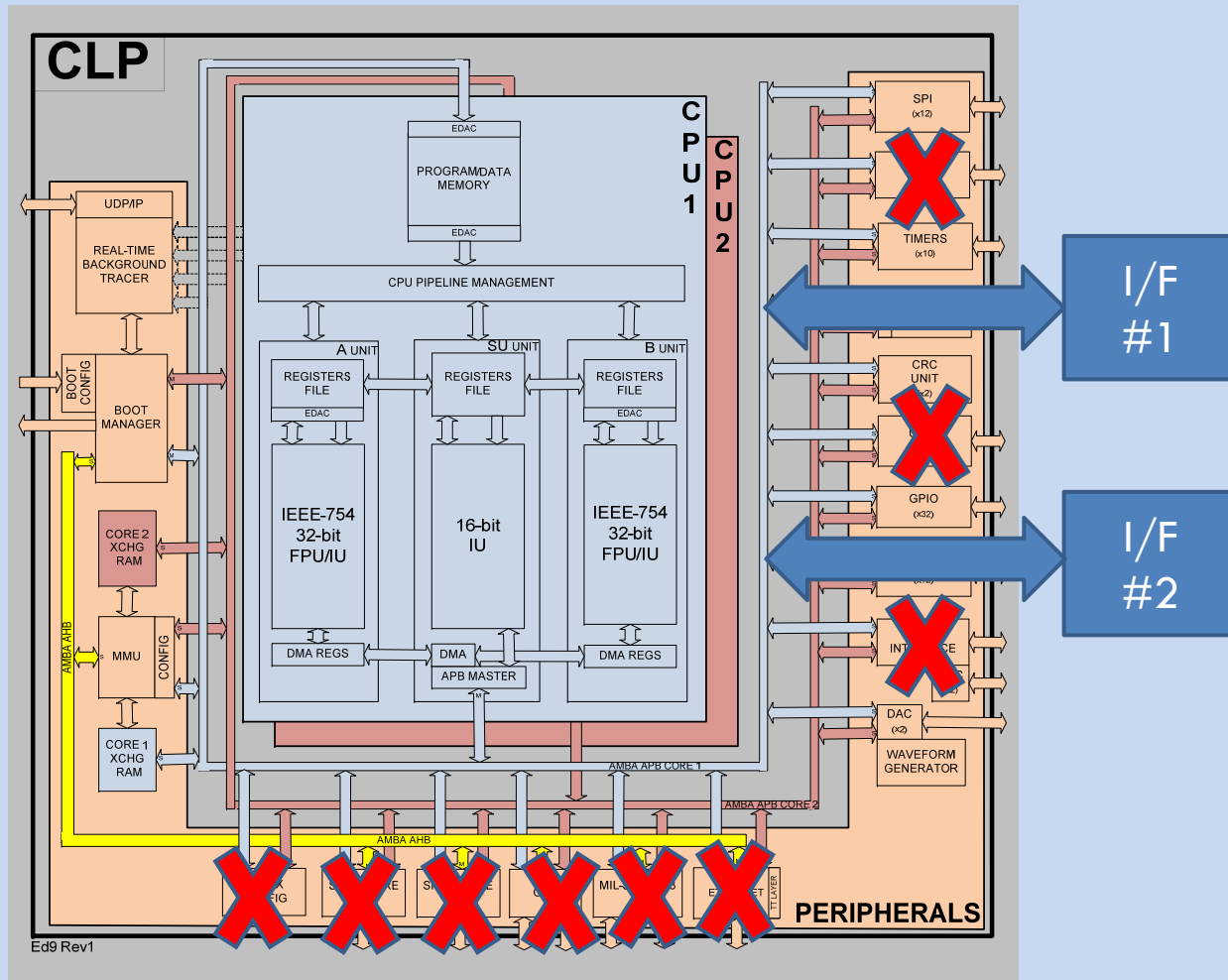   - 20 PID with PWM generation
    - 20 currents acquistion

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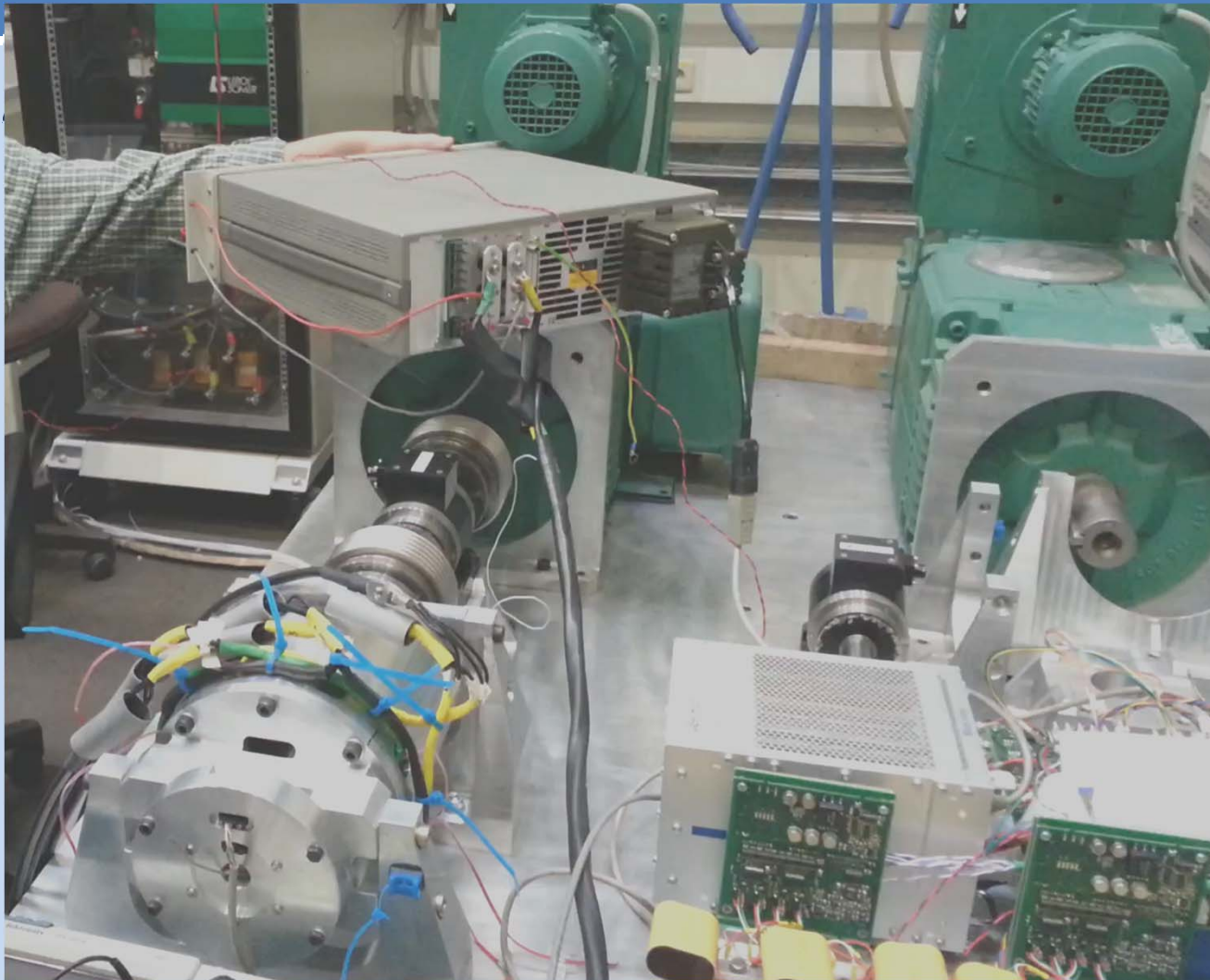# EXAMPLE OF TAILORED CLP APPLICATION

Integrated in an FPGA

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EXAMPLE OF TAILORED CLP APPLICATION

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SUMMARY

AVAILABLE ITEMS

- **IP VHDL code, extensively validated**
  - can be configured as an IP for tailored versions
  - Cobham Gaisler IPs have been used
  - Spacewire, CAN and I2C validation still need completion

- **SystemC model**
  - Cycle accurate with respect to VHDL code

- **Evaluation board based on RASTA system (Cobham-Gaisler)**
  - CLP Bit stream is available

- **Assembler, Tracer and unit test manager**

- **Automated and extensive testbench manager**

- **Preliminary CLP datasheet**

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COMING ITEMS

- **Q1 2017**
  - Waiting for DARE65 availability (DARE180 initially foreseen)
  - SDE v1.0 (C-compiler not included yet)
- **Q3 2017**
  - SDE v2.0 (full set of tools, confidence tests)
- **Q1 2018**
  - Start of ASIC design (TBC)
- **Q3 2019**
  - ASIC prototype tests and characteristation (TBC)
- **2020**
  - Flight Models according to ESCC-9000 (TBC)
  - SDE qualified (production release) (TBC)
- **For more information**
  - http://clp-space.com/

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