Control Loop Processor Phase 1

- GSTP, started 2013
  - SABCA, SpaceBel
  - IMEC, TU-Eindhoven
- Objective
  - Processor for control loops in mechatronics
  - Fully deterministic
    - no cache, no IRQ, only forward branch
  - 2x2 IEEE754 FPU's
    - 2 FPU per core (SIMD) → complex arithmetic
    - 2 independent cores → two axis control (e.g. TVC)
- Background
  - BRISC (biprocessor reduced-instruction-set computer, 1990)
  - HBRISC2: space version ~2002 in 0.35 um, flying on Vega
  - HBRISC3: study in the frame of Ariane-5-ME (2012)
- Achievements
  - SRR, PDR: SoC design in VHDL, extensively verified
  - Core of tool chain: Assembler...
- Follow-up phases
  - Phase 2A: full SDE tool chain Simulink QGEN, LLVM backend
  - ASIC implementation TBD