CLP: Control Loop Processor, Architectural Design, Verification and FPGA prototypes

CLP is a new microprocessor with focus on hard real-time control applications developed by SABCA. CLP is a System-On-Chip (SoC), with numerous peripherals and two CPU cores, each CPU having two IEEE754 Floating Point Units (FPU) in a Single Instruction Multiple Data (SIMD) configuration. This architecture [1] allows performing two-axis control loops with complex floating point arithmetics in one chip. The CLP has no interrupts, the two cores execute from private (non-shared) on-chip memory, and the allocation of the peripherals is frozen at boot time. With appropriate programming precautions, e.g. not using conditional backward branches, an upper boundary for the execution time (= worst case execution time, WCET) can be guaranteed.

The associated Software Development Environment (SDE) relies on Qgen [2] and the LLVM compiler [3], allowing control SW development starting from Simulink and/or from C-Code.

A key driver for CLP is the Thrust Vector Control (TVC) of launch vehicles, where X and Y orientation of the nozzles must be controlled. A predecessor chip of CLP, called HBRISC2 (single core only), is currently being used for the TVC of VEGA and for the flap control of IXV (Intermediate eXperimental Vehicle). Other mechatronic applications can be found for example in robotics or rovers, or with magnetically suspended reaction spheres such as the European Levitated Spherical Actuator [4] project.

The GSTP activity has arrived at the end of Phase 1, a complete and extensively verified VHDL model is available, along with the lower layers of the software tools (e.g. assembler). The CLP concept, implemented in low-cost commercial FPGA, has been adopted by Ariane-6 for the TVC of the lower stages. While the development of the full software environment (SDE) is currently in progress, the CLP design is now ready for further utilisation, either as an IP core for FPGA, or, if market demand and a suitable technology are identified, for implementation as an ASIC.

Besides the CLP itself and its SDE, the presentation will also focus on the comprehensive and highly scripted verification platform developed for CLP, involving RTL simulation and FPGA test against a cycle-exact SystemC reference model, using random stimuli generation, automatic result comparison and automatic nightly non-regression simulations.

Links:

[1] CLP Basic Features. http://clp-space.com/WordPress3/basic-features/
[2] AdaCore QGen. http://www.adacore.com/qgen
[3] The LLVM Project. http://llvm.org/
[4] The ELSA Project. http://elsa-project.eu/