OBC Mass Memory (Solid State mass Memory Board/Module Integrated in OBC)

The overall objective has been to integrate a multi-user complex file based mass memory into the On-Board Computer (OBC) to facilitate a cost effective solution with high performance utilising state-of-the-art solid state memory technologies while at the same time ensure the reliability and endurance required for a mission in the harsh space environment.

The detailed objectives for this study were the following:

- Define and assess a suitable up-screening and test method for flash memory devices taking into account the reliability and endurance concerns in the harsh space environment
- Define and design the OBC Mass Memory Module (OBC-MM) fulfilling the requirements stated in this technical proposal focusing on design for reliability techniques including innovative error correction coding and other error recovery techniques
- Define a suitable division between hardware and software considering necessary performance as well as modularity and flexibility with respect to file system implementations and memory technology and evolution
- Develop and manufacture a representable model of the OBC-MM with components and technologies that have flight equivalent solutions thus demonstrating the suitability of the OBC-MM for flight model realisation
- Develop OBC-MM Engineering Model demonstrator software including a file system, file access and management services available to on-board software (OBSW) nominally running on the OBC processing module as well as CFDP and direct storage of payload TM data to demonstrate the suitability of the OBC-MM architecture and design
- Prepare and execute a demonstrator test suite to verity the OBC-MM architecture and design including error injection to verify the suitability of the chosen error correction and recovery techniques

The OBC-MM architecture supports different OBC and MM configurations.

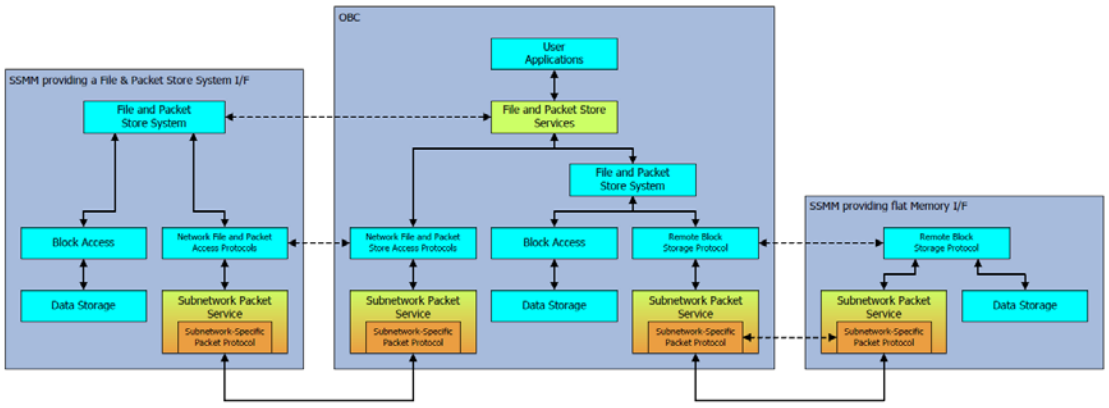

Figure 1: OBC-MM Relationship the OBC

The OBC-MM engineering model has been integrated together with the MFC hardware from the Single Board Computer Core study for the demonstrator ensuring that the developed mass memory module will work smoothly as an integrated mass memory in the On-Board Computer.