Extensions and Validation of Virtual Platform for complex System-on-Chip and IP Cores

This project involved several activities:

1. Evaluation and planning.

The previous project highlighted some issues and shortcomings of SoCRocket. Moreover, the public version of SoCRocekt has been developed and diverged from the one owned by ESA.

Therefore, the purpose of the first activity was to identify the future developments of SoCRocket and the required effort.

This involved performing an accurate analysis of the two code base in order to:

- Evaluate whether the two versions should be merged and the required effort;
- Propose next-to-implement features and calculate the required effort.

2. Enhancement.

This activity intended to extend SoCRocket with new models, which allowed the SoC simulation possibilities to increase.

Three new bus related models have been selected and consequently developed:

- SpaceWire router;
- GR1553b Milbus controller;
- GRCan Can controller.

3. Validation

The framework originally used co-simulation as a method of validating the device models. However, due to the lack of availability and high prices of the VHDL models, the latest models, developed in a previous project, could not be validated.

One of the aims of this project was therefore to provide another method of models/platform validation and apply it to the models that were not yet validated.

A method based on randomized testing has been implemented and used to validate core models such as the memory controller, the level 2 cache and the SpaceWire router.