

The most important thing we build is trust



SpaceFibre Port IP Core

TEC-ED & TEC-SW Final Presentation Days

6 – 7. December 2016

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Commercial in Confidence

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Cobham Gaisler AB



Official name since 10 December 2014

- Founded in 2001
- Located in Gothenburg, Sweden
- Fully owned subsidiary of Cobham plc
- Management team with 60 years combined experience in the space sector:
 - Sandi Habinc: General Manager
 - Per Danielsson: Senior Advisor
 - Jan Andersson: Director of Engineering
- 24 employees with expertise within microelectronics and software design
- Complete design facilities in-house for ASIC and FPGA development
- 63.8 MSEK or 8.8 M\$ turnover 2015





Programme of work



- The activity was planned as a 14 months activity with the following milestones:
 - Task 1: Preliminary SpaceFibre delivery (+2 months)
 - Task 2: Final SpaceFibre delivery (+12 months)
- Due to preliminary internal work, Cobham Gaisler was able to already provide a fully verified prototype implementation as a result of Task 1, which at that time was implemented according to draft version H1 of the specification.
- During Task 2, the implementation and verification environment was continuously updated to reflect the updates of the specification, with the final delivery being in sync with the latest draft version H7 v3.

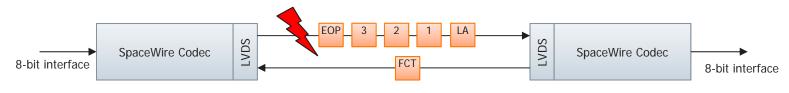
Deliverables



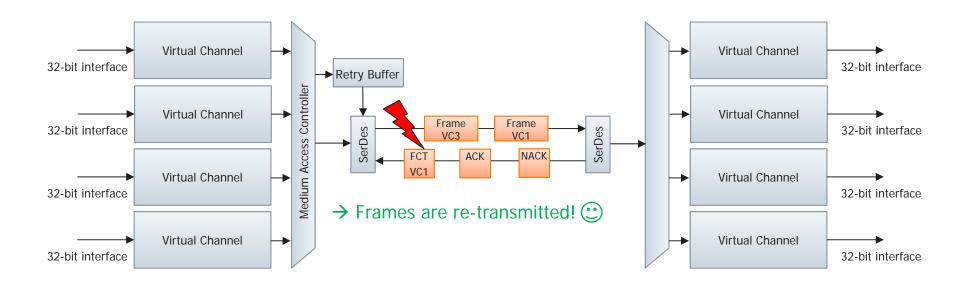
- Datasheet and User's Manual (D1 and D2)
- Verification and Validation Report (D3)
- Final Report (FR)
- VHDL Sources & Testbench (MOD1) including:
 - Source files
 - Testbench
 - Macro files for ModelSim/QuestaSim and Riviera-PRO
 - Simulation Log File
 - Code Coverage Reports
 - Synthesis and Place & Route Estimates



Introduction: SpaceFibre – A powerful enhancement of SpaceWire



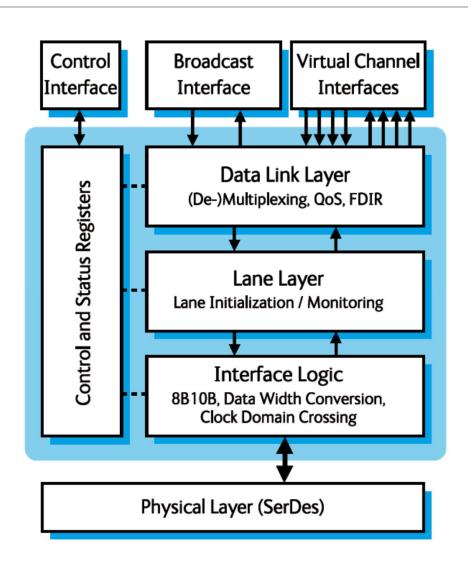
→ Data is interrupted (EEP added)



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Introduction

- Implemented, verified and validated according to latest specification H7 v3.
- Single-lane implementation optimized for speed.
- Highly configurable, yet easy to use IP core.
- Integration into existing SpaceWire designs, e.g. routing switches, is straight-forward.





Configurability

Virtual Channels

- The number of virtual channels
- The depth of the receive buffers.
- The depth of the transmit buffers.
- Width of the data bandwidth credit counter.
- Bandwidth idle time limit in clock cycles.

Broadcast Channel

- Width of the broadcast bandwidth credit counter.
- Minimum bandwidth credit threshold limit.

Error Recovery

- Depth of the data error recovery buffer.
- Depth of the FCT error recovery buffer.
- Depth of the broadcast error recovery buffer.

SerDes Interface

- With internal 8B/10B coding: 20-bit or 40-bit interface, without internal 8B/10B coding: 18-bit or 36-bit interface.
- Enable/disable internal 8B/10B coding.
- Use a separate transmission clock: This feature is mandatory if the 18-/20-bit SerDes interface is used and optional in case of the 36-/40-bit interface.

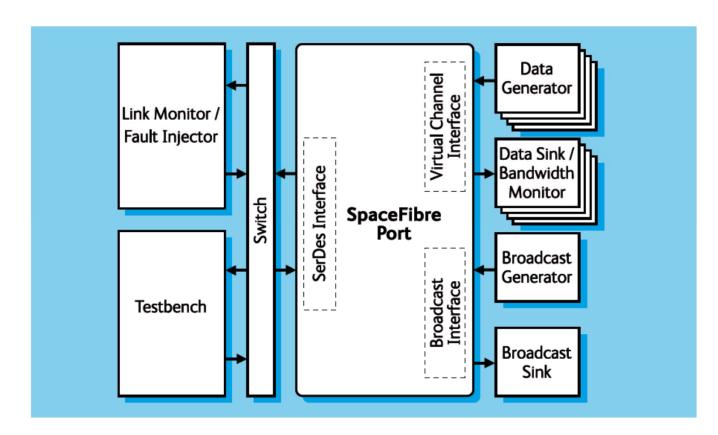
Technology

- Use asynchronous or synchronous reset.
- Generic memory description, which infers correct memories on RTG4 and Virtex-5.
 Can easily be replaced by technologydependent memories.



Verification (1/4)

- Testbench setup comprises a SpaceFibre port with four virtual channels.
- Verified according to guidelines of the European Space Agency (ESA).





Verification (2/4)

- The testbench executes 45 tests, including tests covering all aspects of:
 - the lane layer
 - the virtual channel data communication and flow control
 - the virtual channel QoS mechanisms (bandwidth allocation, priorities, timeslots, babbling idiot protection)
 - the reception and transmission of broadcasts
 - the correct behaviour of the error-recovery mechanisms and
 - the data scrambler and de-scrambler.
- Comes with a convenient macro file to compile and run tests:

```
| SpaceFibre port IP core testbench (c) Cobham Gaisler
| Possible commands:
| (c) Compile all files (cc) Code coverage test runs
| (lt) List all test cases (cp) Configure SpaceFibre port
| (ra) Run all tests (ri) Run individual test
| (cd) Clean directory (q) Quit
```



Verification (3/4)

 The link analyser output is written to a log file during loopback test runs:

3205408000	ps		0000	C5_72_31_DA
3205424000	ps		0000	0E_93_D7_A0
3205440000	ps	ACK	0001	SEQ: 10 CRC: 21
3205456000	ps		0000	55_A4_AF_DC
3205472000	ps		0000	16_72_F0_E7
3205488000	ps		0000	84_38_D5_68
3205504000	ps	SDF	0001	VC: 01
3205520000	ps		0000	00_00_01
3205536000	ps		0000	00_00_02
3205552000	ps		0000	00_00_03
3205568000	ps		0000	00_00_04
3205584000	ps		0000	00_00_05
3205600000	ps		0000	00_00_06
3205616000	ps		0000	00_00_07
3205632000	ps		0000	00_00_08
3205648000	ps		0000	00_00_09
3205664000	ps		0000	A0_00_00
3205680000	ps		0000	00_00_00_0B
3205696000	ps		0000	00_00_00_0C
3205712000	ps	FCT	0001	SEQ: 11 CRC: 3E CH: 00
3205728000	ps		0000	00_00_0D
3205744000	ps	FCT	0001	SEQ: 12 CRC: 21 CH: 01
3205760000	ps		0000	00_00_0E
3205776000	ps	FCT	0001	SEQ: 13 CRC: 07 CH: 02
3205792000	ps		0000	00_00_0F
3205808000	ps	FCT	0001	SEQ: 14 CRC: 1F CH: 03
3205824000	ps		0000	00_00_00_10
3205840000	ps	FCT	0001	SEQ: 15 CRC: 39 CH: 00
3205856000	ps		0000	00_00_00_11



Verification (4/4)

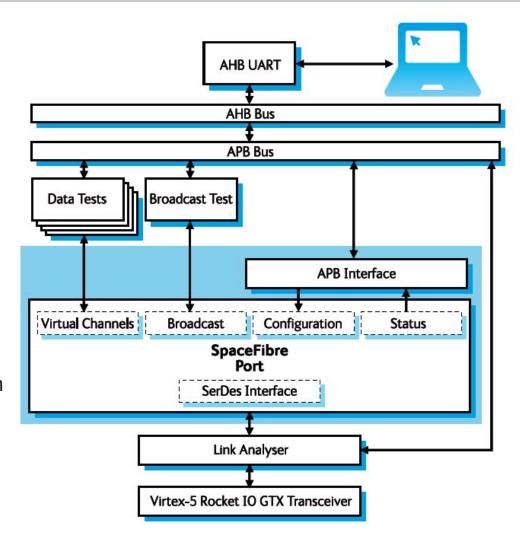
 Full code coverage can be achieved by regression testing using different hard configuration options:

File	Statements	Branches	Condition Terms
async_fifo.vhd	40/40	12/12	2/2
bc_layer.vhd	30/30	20/20	-
fwft_fifo.vhd	25/25	17/17	4/4
fwft_fifo_ack.vhd	27/27	20/20	2/2
if_layer.vhd	166/166	80/80	26/26
lane_layer.vhd	224/224	85/85	40/40
lreset_sm.vhd	24/24	13/13	4/4
retry_buf.vhd	132/132	62/62	8/8
retry_layer.vhd	494/494	308/308	104/104
spfi_pkg.vhd	217/217	4/4	-
spfi_top.vhd	54/54	-	-
sync_dpram.vhd	6/6	9/9	-
vc_layer.vhd	222/222	79/79	28/28

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Validation: Overview

- Validation performed on Xilinx Virtex-5 FX130T and Microsemi RTG4.
- Configuration: 4 Virtual Channels.
- Additional components:
 - 4 Data Generators / Sinks.
 - 1 Broadcast Generator / Sink.
 - Link Analyser.
 - Comfortable control of validation test bench through GRMON / Graphical User Interface.

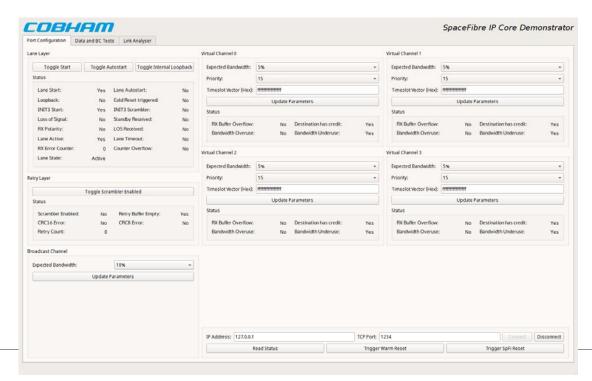




Validation: Test Software (1/3)

- Overview of all IP core status flags.
- Control flags:
 - Start / Autostart / Internal Loopback.
 - Scrambler enabled.
- Expected bandwidth of broadcast channel (1% to 95%).
- Expected bandwidth of virtual channels (1% to 95%).

- Priority level of virtual channels (0 to 15).
- Time-Slot vectors of virtual channels (64 bits).
- Triggering of system reset / link reset.
- Connection to GRMON via TCP connection.



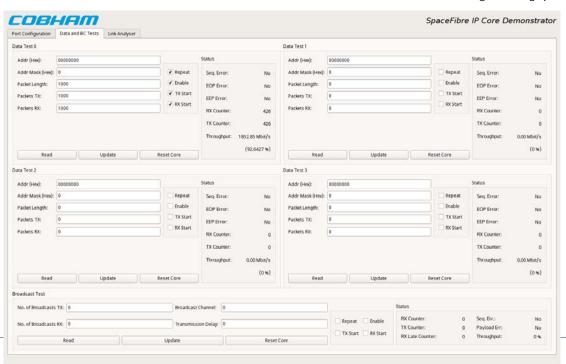


Validation: Test Software (2/3)

- Data Tests (4x):
 - Up to 4 SpaceWire addresses.
 - Packet Length.
 - Number of packets.
 - Auto-repeat function.
 - Indication of:
 - Number of RX/TX packets.
 - Sequence, EOP and EEP errors.
 - Average throughput rate.

Broadcast Test:

- Number of broadcasts.
- Transmission delay between broadcasts.
- Broadcast channel.
- Auto-repeat function.
- Indication of:
 - Number of RX/TX packets.
 - Number of BCs with Late flag set.
 - Sequence and Payload errors.
 - Average throughput rate.

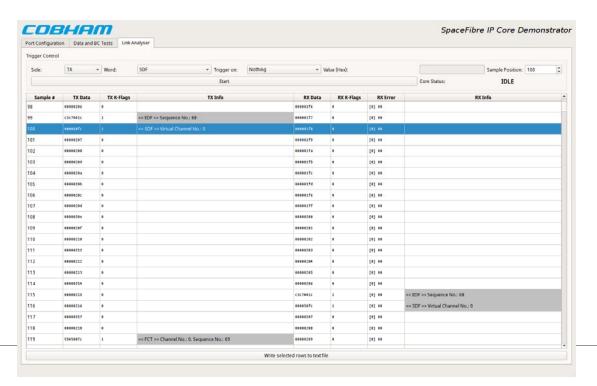




Validation: Test Software (3/3)

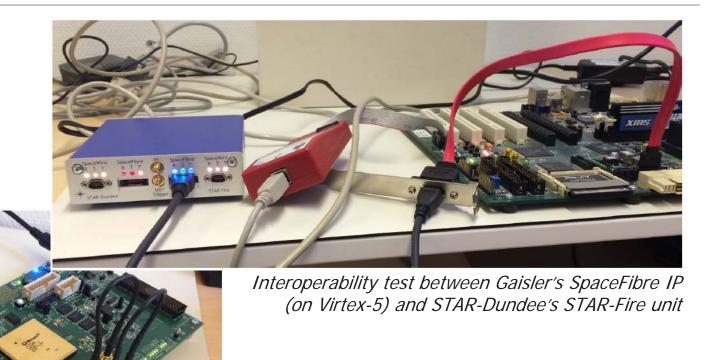
- Comfortable analysis of link traffic.
- Sample position can freely be chosen.
- Raw data is decoded, e.g. virtual channel numbers and sequence numbers.
- Simple export of results to text file.

- Triggering on the following events:
 - Data/Broadcast Payload
 - RXERR, SKIP, IDLE, STANDBY, LOS words
 - INIT1, INIT2, INIT3 words
 - ACK, NACK words
 - FULL, RETRY words
 - SDF / EDF words
 - SBF / EBF words
 - FCT words, SIF words



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Validation: Test Hardware



Loopback tests on Microsemi's new RTG4 device



Validation: Test Results - Loopback

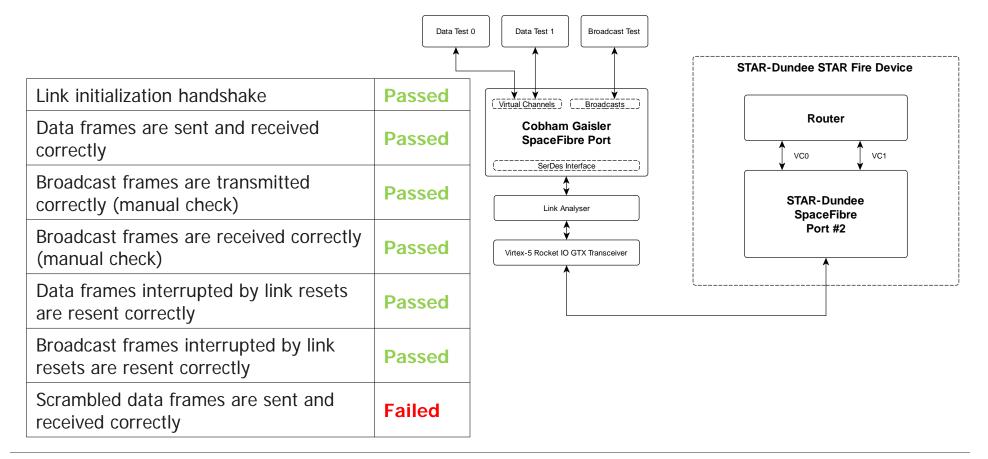
 SpaceFibre core is operated in external loopback mode (near-end PMA loopback of SerDes activated).

1	Link initialization handshake test (link start and auto start mode)	Passed
2	Transmission and reception of data frames	Passed
3	Data frames interrupted by link resets are resent correctly	Passed
4	Transmission and reception of broadcast frames	Passed
5	Broadcast frames interrupted by link resets are resent correctly	Passed
6	Scrambled data frames transmitted/received correctly	Passed
7	Broadcast transmission do not exceed maximum allowed bandwidth value	Passed
8	Priority mechanism for virtual channels works as expected	Passed
9	Timeslot mechanism for virtual channels works as expected	Passed
10	Bandwidth limitation of virtual channels works as expected	Passed
11	Internal loopback mode works as expected	Passed



Validation: Test Results - Device Interoperability

SpaceFibre core is connected to STAR Fire unit via Serial ATA cables.
 Data is sent/transmitted on virtual channels 0 and 1 and looped back through routing switch in STAR Fire unit.



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Synthesis Estimates

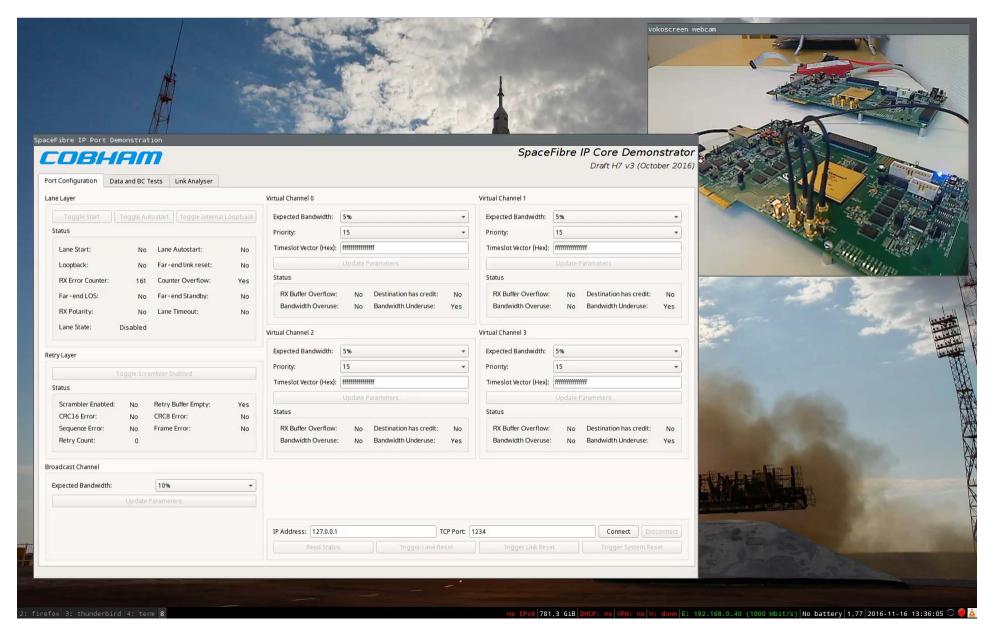
Technology	Configuration	Area	Expected data rate
C65SPACE	Full config with 8 VCs	25,971 NAND gate equivalents	> 6.25 Gbps
Virtex-4QV SX55	No 8b10b with 4 VCs	3% FFs, 9% LUTs, 3% RAMs	> 3.125 Gbps
Virtex-5Q FX130T	No 8b10b with 4 VCs	2% FFs, 4% LUTs, 3% RAMs	6.25 Gbps
RTG4	Full config with 4 VCs	2% FFs, 4% LUTs, 4% RAMs	2.5 – 3.125 Gbps
RTAX2000s	Full config with 2 VCs	27% C-Cells, 19% S-Cells, 37% RAMs	2.0 – 2.5 Gbps



Thank you for your attention

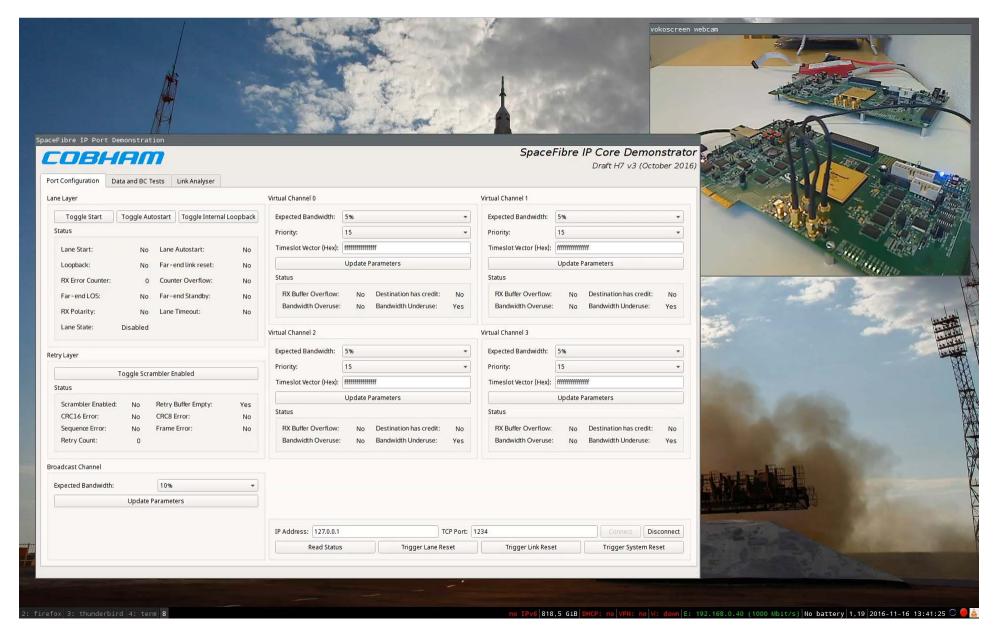


Video Demonstration: Virtual Channel - Bandwidth Allocation



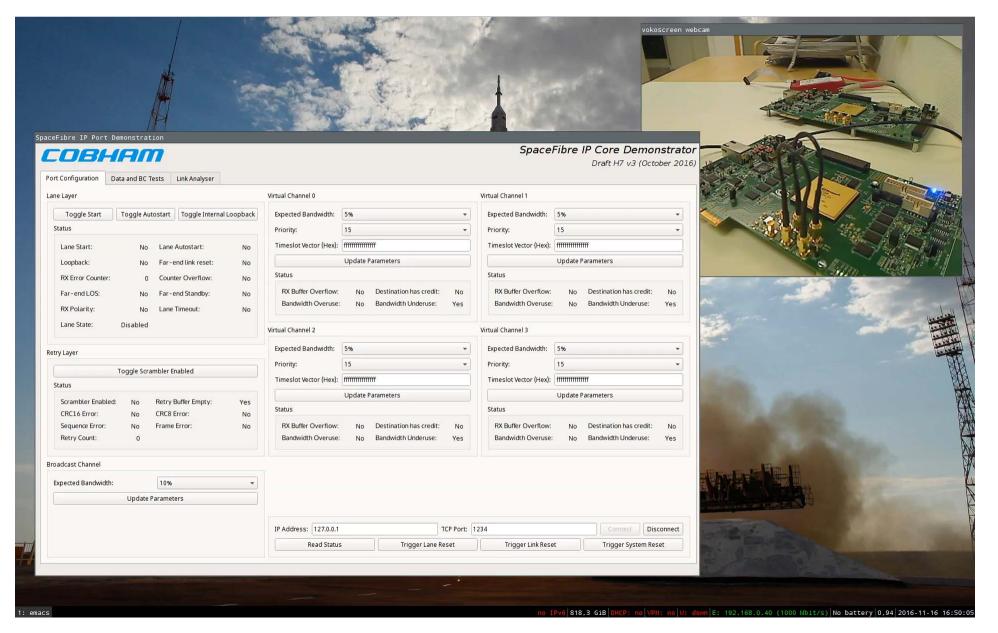


Video Demonstration: Virtual Channel - Different Priorities



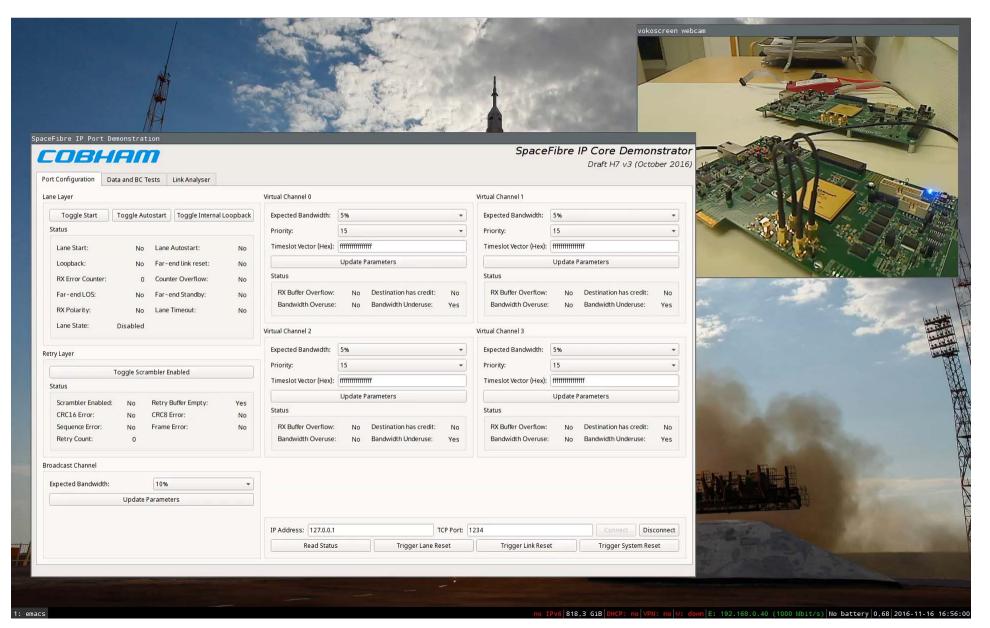


Video Demonstration: Virtual Channel - Timeslots





Video Demonstration: Virtual Channel - Broadcasts





Video Demonstration: Virtual Channel – Link errors

