SpaceFibre Port IP Core

In the course of this activity, Cobham Gaisler developed a VHDL implementation of a SpaceFibre port including a comprehensive verification environment and all required documentation.

SpaceFibre is a new high-speed serial data link specifically designed for spaceflight applications that incorporates several Quality-of-Service (QoS) techniques. Independent communication channels can be combined into a single network stream by means of virtual channels. The virtual channels are multiplexed based on reserved bandwidth, priorities, time-slots, or a combination of these mechanisms. Integrated Fault Detection, Isolation and Recovery (FDIR) support guarantees fault-free communication. Comparable to other modern intercommunication architectures like Serial RapidIO, Serial ATA or PCI Express, SpaceFibre communicates over a Serialiser/Deserialiser (SerDes) device and can therefore reach throughput rates of several Gigabits per Second (Gbps). However, due to its native support of the SpaceWire packet format, its small area overhead and its high performance, SpaceFibre is particularly well suited for future high-speed on-board communication.

The IP core was developed according to the latest draft version H7 of the SpaceFibre specification. It is a fast and easy to implement single-lane implementation with low area and power overhead, which is fully verified in a complex VHDL testbench environment (achieving full code coverage) and validated by means of a FPGA prototype system that also includes a versatile test and debug software. For this task, two FPGAs were chosen that are also available as space-qualified devices: the Microsemi RTG4 and the Xilinx Virtex-5 FX130T.