SpaceWire Physical Layer Testing

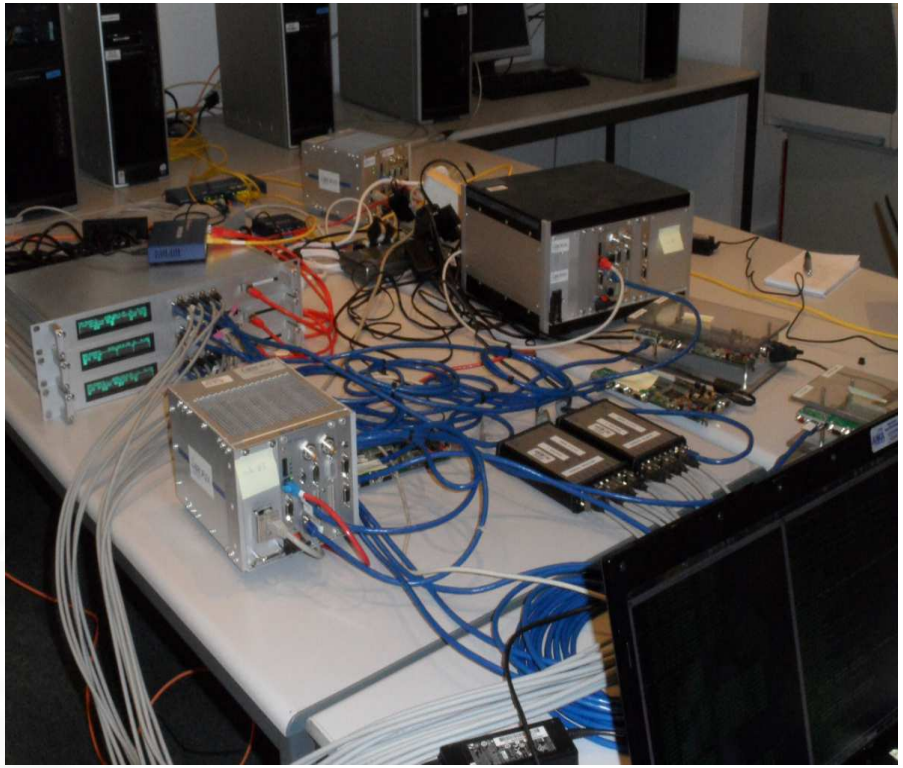
ThalesAlenia Space
A Thales / Finmeccanica Company

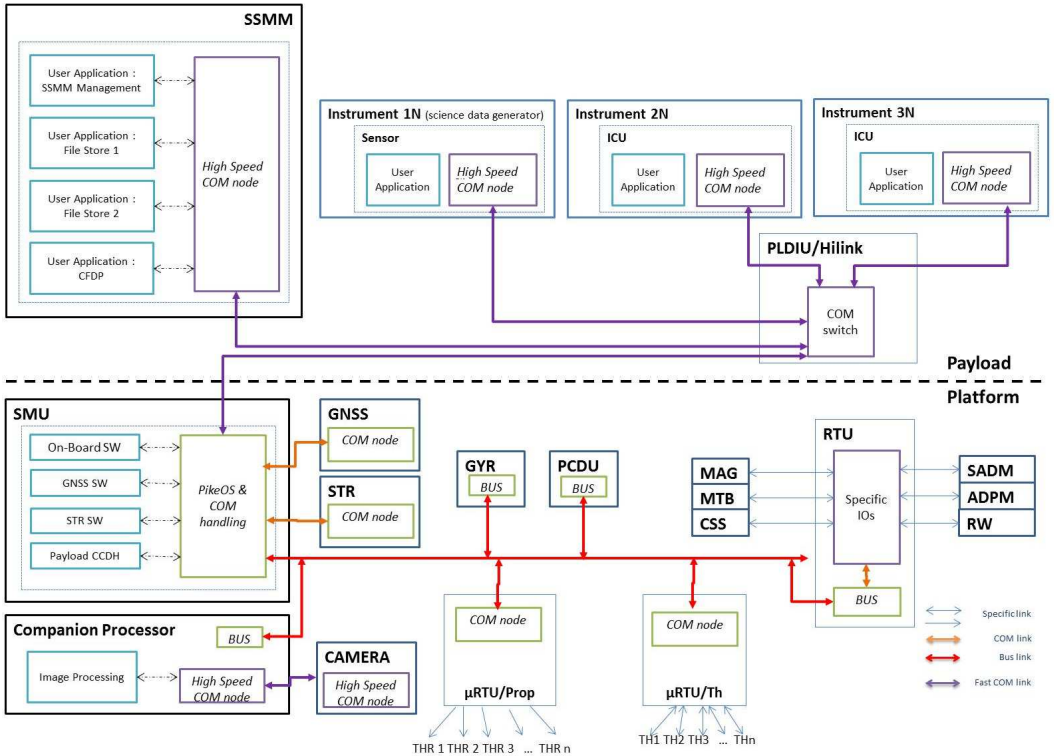
Summary

- Context & objectives
- Test procedure !
- Test results (extracts)
- Recommendations & ways forward

SpaceWire context & study objectives (1)

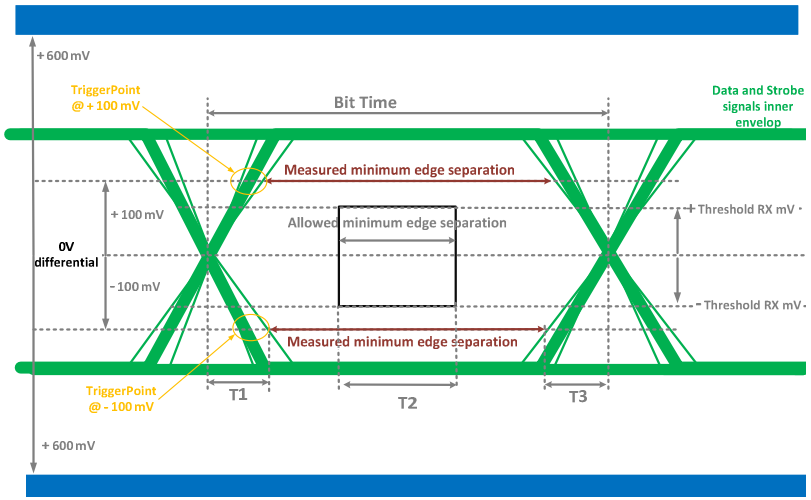
- SpaceWire: network or point-to-point technology enabling 2-200Mbps communications
- SpaceWire is a key technology deployed over all new avionics & baselined in all new CPU SoC developments
  - ECSS standards exist since 2003 (ECSS-E-50-12A originally)
  - Deployed over many missions (and baselined on all new TAS missions)
  - Active working group with worldwide community (EU, Japan, Russia, US & more)
  - Many updates scheduled (standard upgrade, new services around SpaceWire, SpaceFibre)





SpaceWire context & study objectives (2)

- **But: there is still no standard procedure to validate SpaceWire**
- **Main issues:**
  - Fast data link (need to take care about the eye diagram)
  - Variable link speeds
  - Low voltage technology & sensitive to common modes
  - No clock line: data & strobe technology
    - TX: STROBE = DATA XOR CLOCK (strobe encoding)
    - RX: CLOCK = DATA XOR STROBE (clock recovery)
  - SpaceWire characteristics defined by std, but board? System?

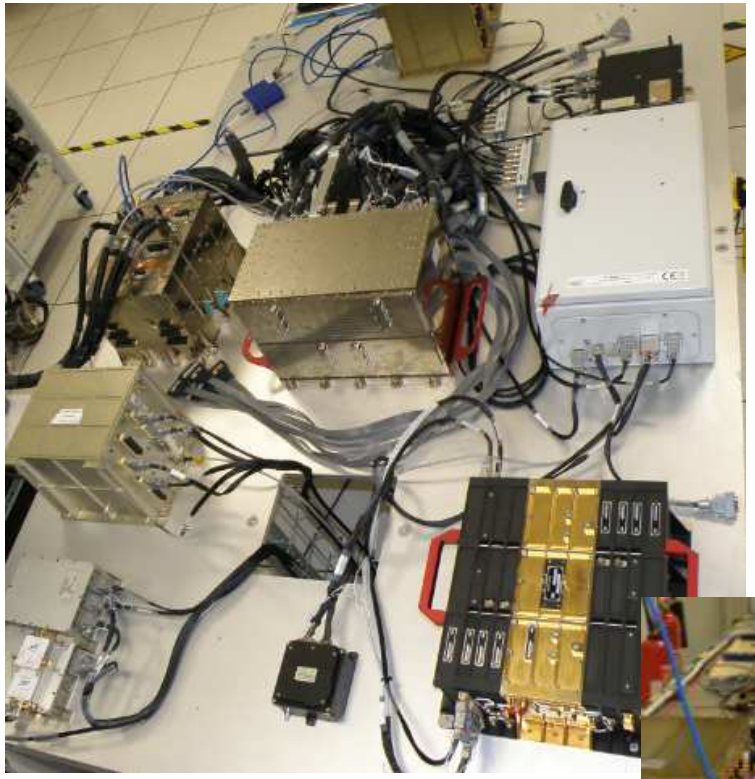


- **Main goals of this activity are to:**
  - Define a test procedure for the SpaceWire physical layer
  - Develop a test board to challenge the procedure and propose a reference implementation & test mean
  - Provide guidelines for testing & designing test means

- **Team:**
  - ESA: Wahida Gasti & Giorgio Magistrati
  - TASF: Brice Dellandrea & Nans Douay
  - TASI: Gianluca Aranci & Marco Mattavelli
  - 4links: Paul Walker

SpaceWire characteristics → System?

- **How to check electrical detailed characteristics in case a link is misbehaving?**



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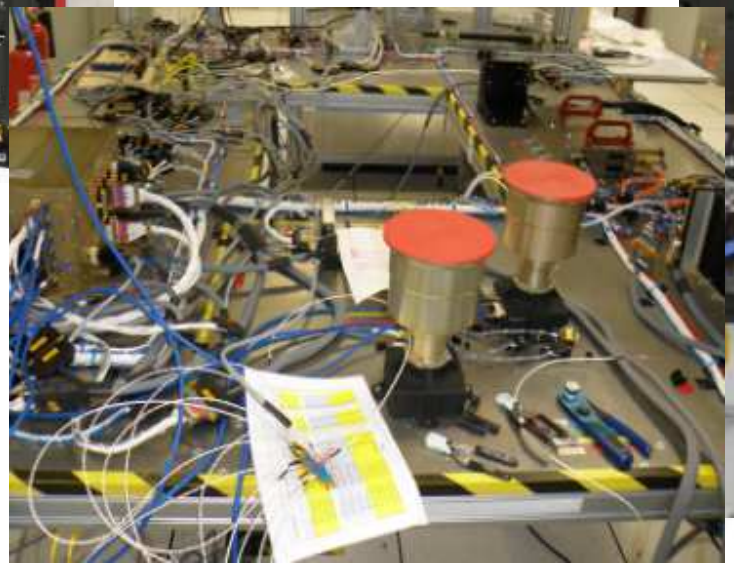

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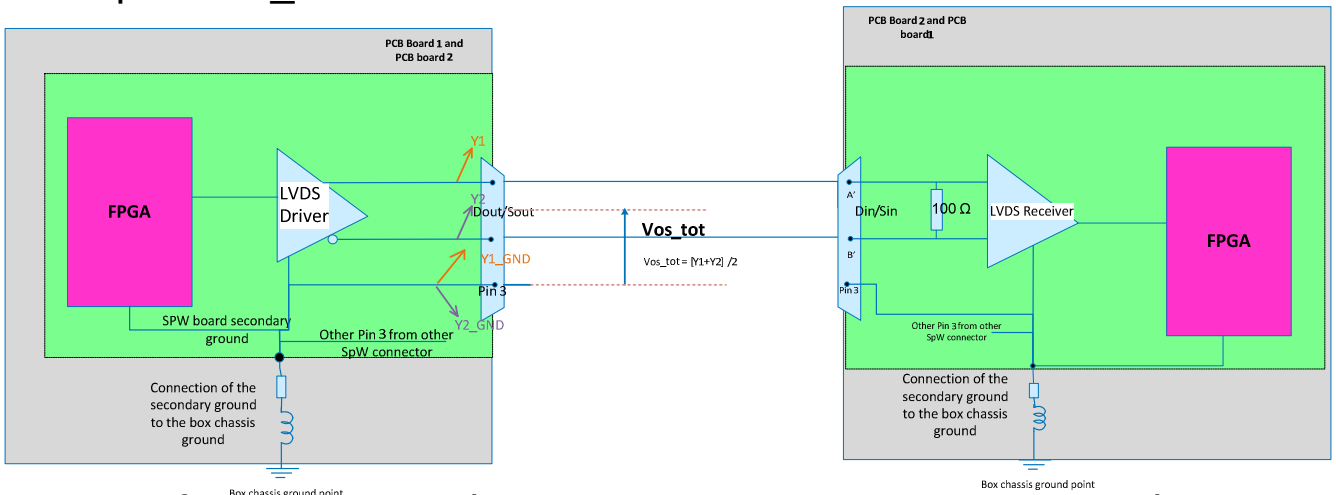
Test procedure !

- Define a thorough validation approach enabling SpaceWire physical layer testing for any SpaceWire equipment:
  - DC-CM tests (Derived from TIA-644-A limits – LVDS standard)
  - AC-CM tests (Related to the condition of usage of the interface within the spacecraft & electrical mass global management policy; needs to be tuned as per specific implementation)
  - Eye-pattern tests & signal quality measurements
  - Cross-talk tests
  - BER tests
  - EMC/EMI tests
  - Thermal tests

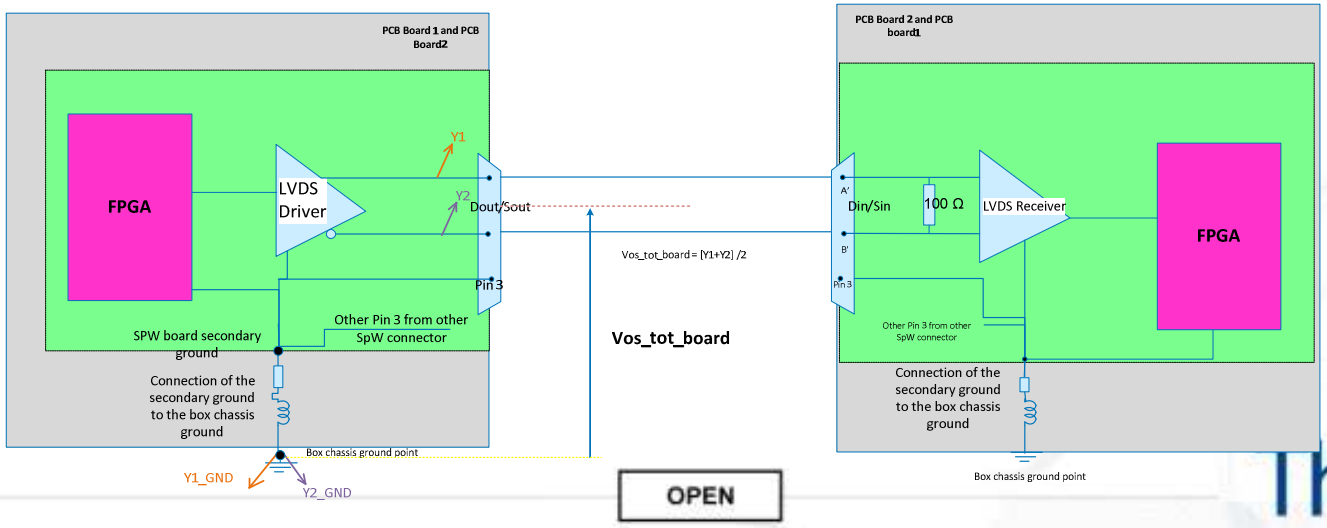
Test procedure !

DC-CM tests

- The SPW DC common mode test purpose is to measure the overall Vos of the LVDS drivers and the overall Vos of the SpW Board: required for drivers operation
- DC-CM test set-up of Vos_tot measurement on FPGA PCB Boards

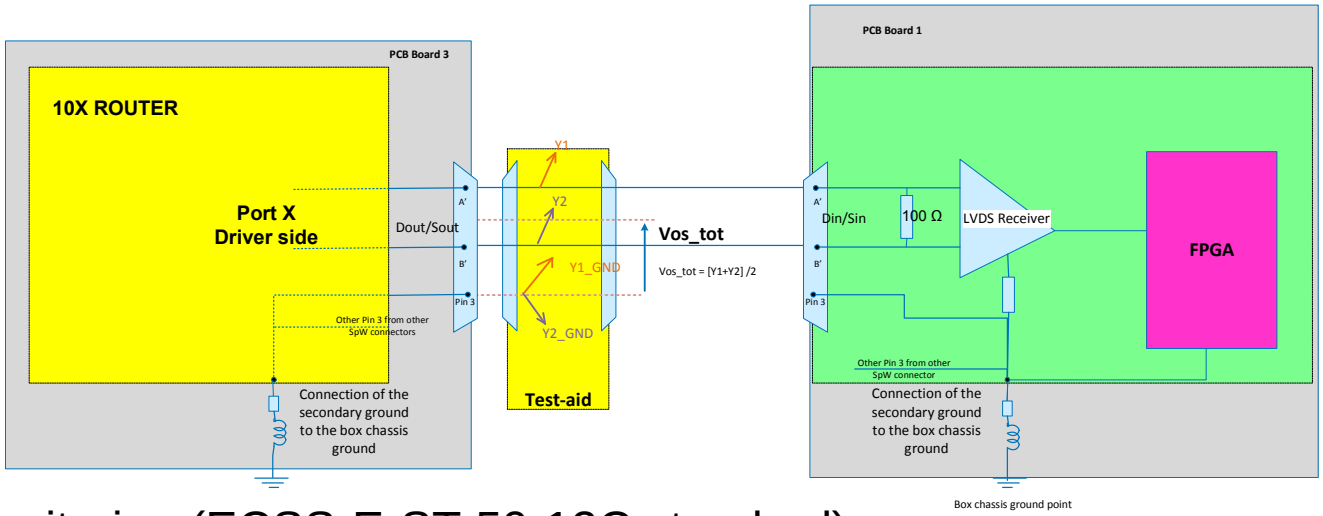


- DC-CM test set-up of Vos_tot_Board measurement on FPGA PCB Boards



Test procedure !

- **DC-CM tests**
  - With a test-aid to reach the relevant measurement points on the hardware to be tested

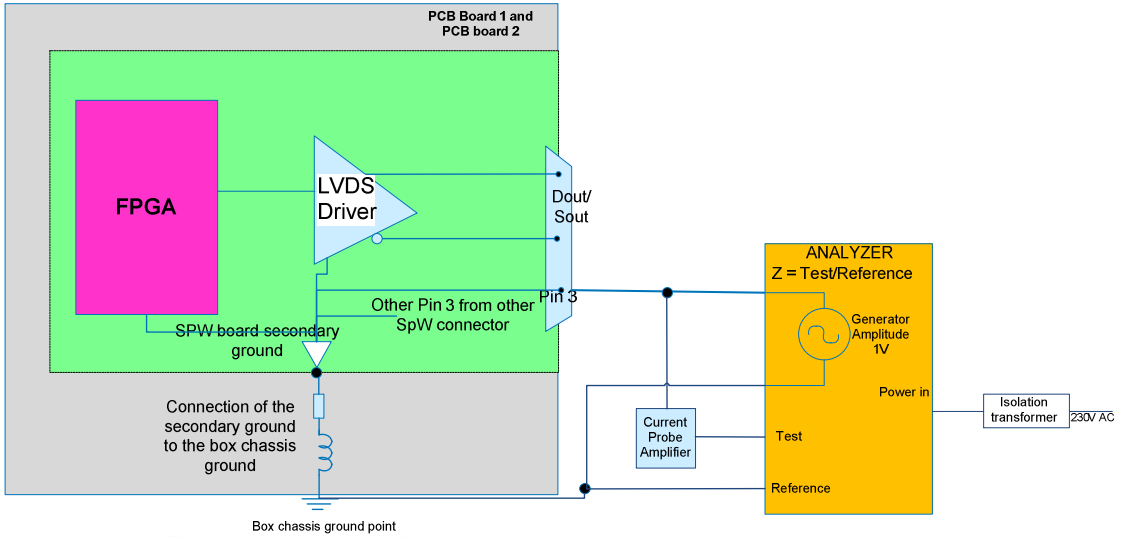


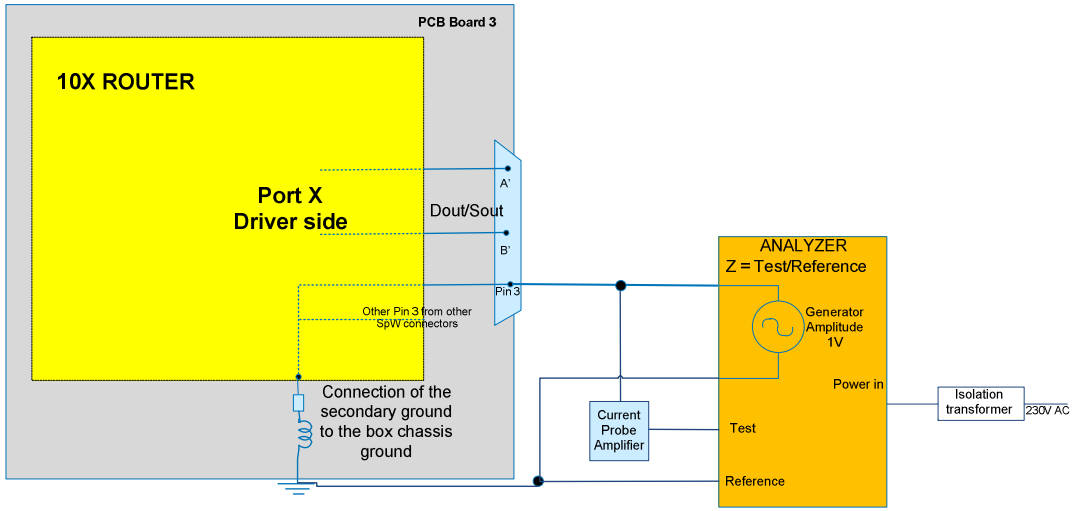
  - Success criterion (ECSS-E-ST-50-12C standard)

Parameter	Min	Max
Vos (steady-state value of the driver offset voltage)	1125mV	1375mV (1450mV in rev1)
|ΔVos| = |Vosh-Vosl|	50mV	
ΔVos Dynamic-State	150mV(peak-peak)	
|Vod| (output/driver differential voltage) to be measured in both logical states	247mV	454mV
|ΔVod| in Steady-State	50 mV	
Vos_tot	1050mV	1450mV (1525mV)
Vcm_driv_FPGA	50 mV (due to the number of terminals)	
Vcm_driv_10X	50 mV (due to the number of terminals)	
Vos_tot_board_FPGA	1050mV	1500mV (1575mV)
Vos_tot_board_10X	1050mV	1500mV (1575mV)

Test procedure !

- **AC-CM tests**
  - Measurementof the impedance of the LVDS driver/10X router secondary ground connection to the box chassis.



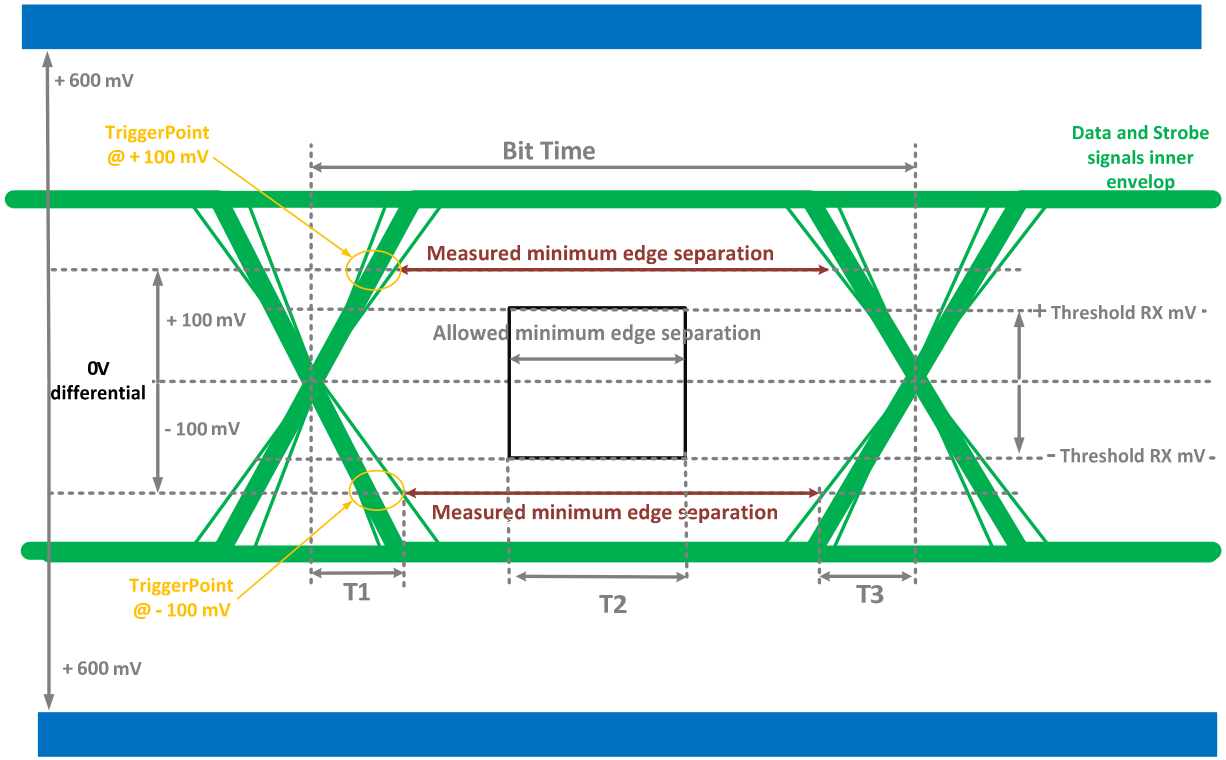


- **Success criterion**
  - The impedance not to exceed is $Z = \frac{Vcm_{driv_{FPGA}}}{100\ \mu A * SQRT(2)}$ so Z ≤ 250 Ω.

Main Frequency(MHz)	Third Harmonic (MHz)	Fifth Harmonic (MHz)
2	3	5
10	15	25
100	150	250
150	225	375
200	300	500

Test procedure !

- **Eye pattern tests**
  - The eye pattern test aims at verifying the signal integrity at receiver level with combined effect of all the communication chain

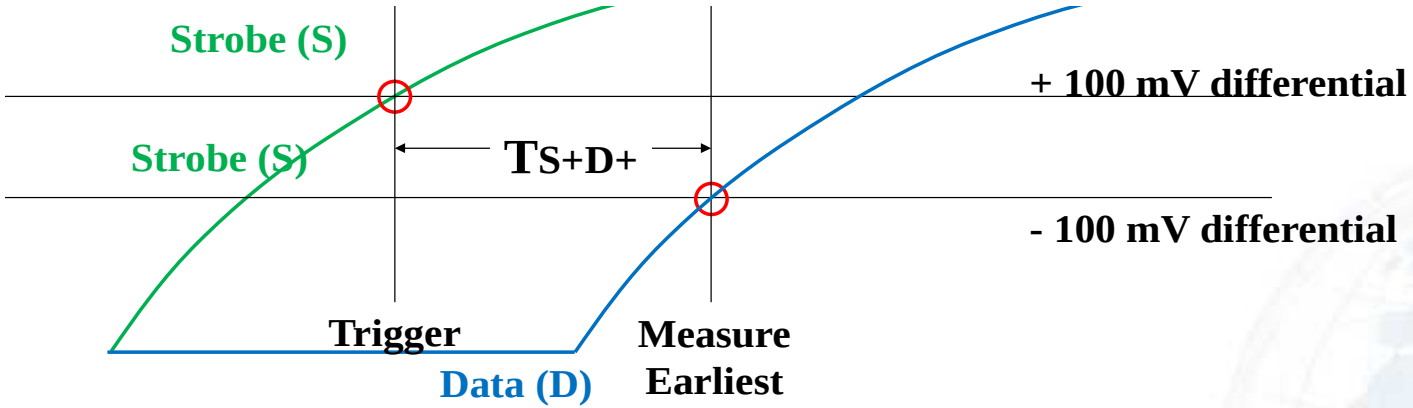


- T1: combination of rise-time, skew and jitter, triggered on the latest signal transition (Data XOR Strobe)
- T2: minimum edge separation allowed by the receiver
- T3: combination of fall-time, skew and jitter
- For a good communication: T1+T2+T3 <= Bit period
- Measured minimum edge separation: minimum duration on which the signal is valid

Test procedure !

Eye pattern tests

- The eye pattern shall be measured at receiver termination resistor level by :
  - 1. Either using the reconstructed clock of the signal (logic: Data XOR Strobe) pending that the timing degradations of the scope are negligible with respect to the bit period and measured the Data and Strobe signal while triggering on the reconstructed clock signal.
  - 2. Or If the timing degradations of the scope are not negligible or this feature is not available in the scope's functionalities , the following measurement set up is predefined:
    - Measurement of the Data and Strobe signal while triggering on the Strobe signal positive and negative edge at +100mV for rising edge and -100mV for falling edge (or preferably the Rx threshold if known).
    - Measurement of the Data and Strobe signal while triggering on the Data signal positive and negative edge at +100mV for rising edge and -100mV for falling edge (or preferably the Rx threshold if known).



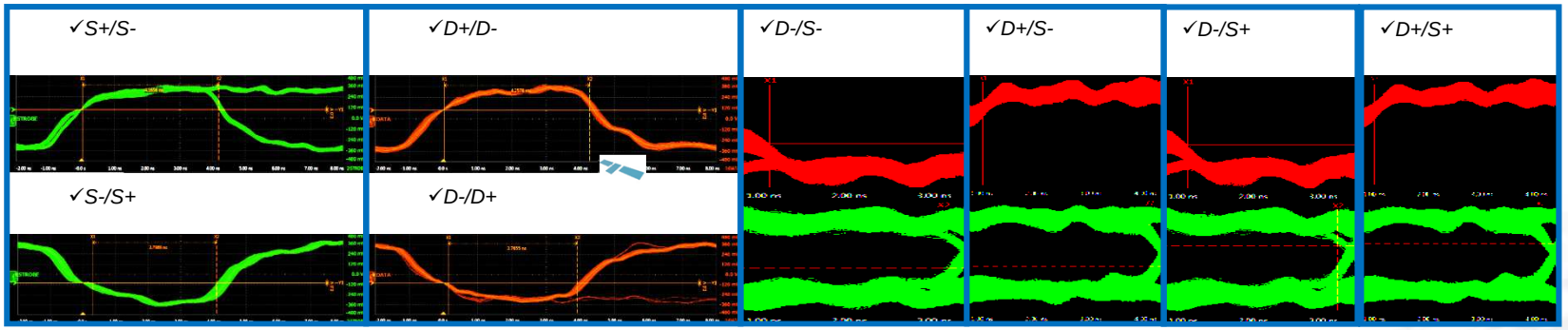
→ Needs to check all transitions: T_{D+D-}, T_{D+S+}, T_{D+S-}, T_{D-S+}, T_{D-S-}, T_{D-D+}, T_{S+D-}, T_{S+D+}, T_{S+S-}, T_{S-S+}, T_{S-D-}, T_{S-D+}

Test procedure !

Eye pattern tests: which pattern?

- There are worst-case patterns that affect specific tranceivers and needs to be checked:
  - Default: random transitions through the transmission of PRBS patterns
  - TS+S- : Strobe 0: {Long chains of [0x55], [0x57, EoP]}
  - TS-S+ : Strobe 1: Long chains of single 0xAA N-Chars each ended with EOP
  - TD+D- : Data 0: {Long chains of {[0x00], [0x01, 0x00, EoP]), (long chain of [0x00], [0x01, 0x00, 0x00], EoP)}
  - TD-D+ : Data 1: {Long chains of [0xFF], [0xFE], ESC(ape), 0xFF,0xFF], EOP}

- Tests have been performed over 2 Mbps, 10Mbps, 100 Mbps, 150 Mbps and 200 Mbps:



- The Success criteria of the EPT is at receiver termination resistor level : Measured min edge separation > allowed min. edge separation = [skew + jitter] contribution of the LVDS receiver (value coming from the datasheet) + FPGA routing contributions (value coming from the FPGA timing analysis)

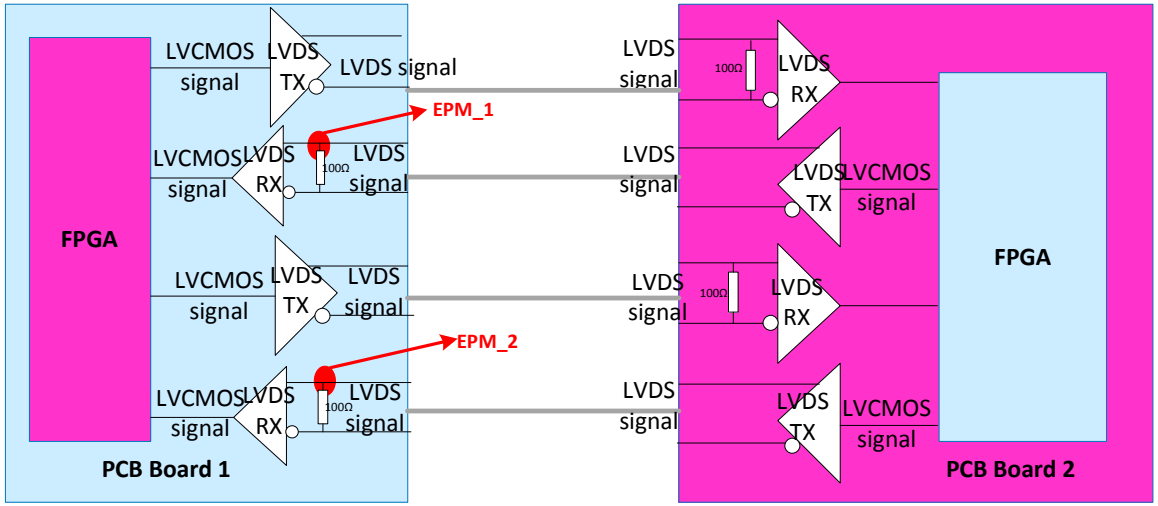
Test procedure !

- **Eye pattern tests: a test defined in ECSS-E-ST-50-12Crev1:**
  - a. When a test signal is sent by the line driver through the SpaceWire connectors and cable assembly, the received signal measured at the receiver termination resistor or within 20 mm of the line receiver inputs shall have:
    - 1. a minimum edge separation which is greater than the minimum edge separation required by the SpaceWire line receiver, see clause 5.3.6,
    - 2. a differential amplitude of more than +100 mV or less than -100 mV in the region between the edges, and
    - 3. a differential amplitude of less than 600 mV.
    - NOTE […]
  - b. The test signal shall comprise a repeating sequence of the following set of SpaceWire packets following one another sent without any Nulls between the data characters:
    - 1. SpaceWire packet of length greater than 1000 bytes containing a pseudorandom bit sequence;
    - 2. SpaceWire packet of length greater than 1000 bytes all set to 0x55.
    - NOTE […]
  - c. The receive signal shall be measured across the line receiver termination resistor using an oscilloscope and differential probes which have bandwidths of at least 1,05 times the reciprocal of the signal rise time.
    - […]
  - d. Where the termination resistors are internal to an integrated circuit, the receive signal may be measured within 3 cm of the line receiver pins on the integrated circuit.
  - e. When access to the termination resistors is not possible, the receive signal may be measured at the connector adjusting for the transfer impedance between the connector and the termination resistor or other equivalent method.
    - NOTE […]

Test procedure !

Cross-talk tests

- The cross talk test will identify any perturbations on the receiver side coming from the interferences between LVCMOS signals and the LVDS signals generated on the same board



- The Success and Failure criterions of the Cross-talk test shall be based on an EPT test: no degradation shall affect the EPT signal shape/timing results, validated by the minimum edge separation

Test procedure !

$$P(\varepsilon < N) = \sum_{k=0}^{N} P_n(k) = \sum_{k=0}^{N} C_{n,k} \cdot p^k \cdot q^{n-k} \qquad CL = 1 - e^{-N \times BER_S} \times \sum_{k=0}^{E} \frac{(N \times BER_S)^k}{k!}$$

BER tests

- Evaluation of the Bit Error Rate over a given duration. For such a link: BER figure expected < 10^{-12}
- The BER test durations shall be as minimum as follows for 2 Mbps, 10Mbps, 100Mbps, 150Mbps and 200Mbps:

Dara Rate (Mbps)	Number of observed errors	Minimal duration for 1 sigma accuracy (67% confidence)	Minimal duration for 2 sigma accuracy (95% confidence)	Minimal duration for 3 sigma accuracy (99.7% confidence)
2	0	153.98	416.07	806.83
2	1	320.83	659.72	1112.50
2	2	480.56	875.00	1376.39
10	0	30.80	83.21	161.37
10	1	64.17	131.94	222.50
10	2	96.11	175.00	275.28
100	0	3.08	8.32	16.14
100	1	6.42	13.19	22.25
100	2	9.61	17.50	27.53
150	0	2.05	5.55	10.76
150	1	4.28	8.80	14.83
150	2	6.41	11.67	18.35
200	0	1.54	4.16	8.07
200	1	3.21	6.60	11.13
200	2	4.81	8.75	13.76

- The BER test can be considered as successful or failed by checking the following table:

CL	1sigma		2sigma		3sigma	
E	REJECT (>= E)	ACCEPT (<=E)	REJECT (>= E)	ACCEPT (<=E)	REJECT (>= E)	ACCEPT (<=E)
0	NA	1.11	NA	3.00	NA	5.81
1	0.41	2.31	0.06	4.75	0.01	8.01
2	1.18	3.46	0.36	6.30	0.08	9.91
3	2.03	4.58	0.82	7.76	0.29	11.65
4	2.90	5.69	1.37	9.16	0.59	13.31

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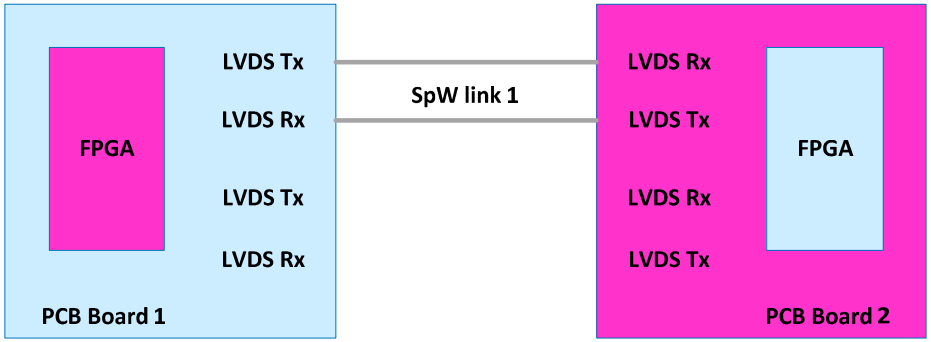
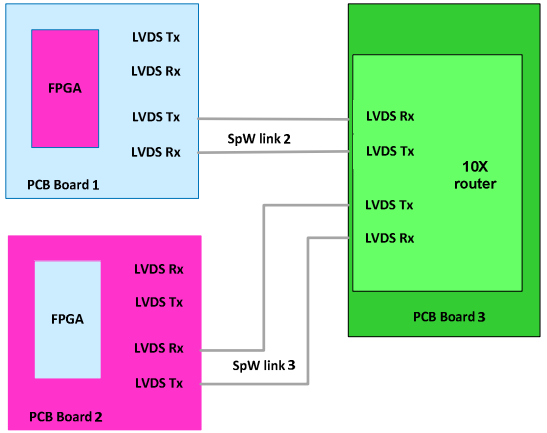
Test procedure !

EMC/EMI tests

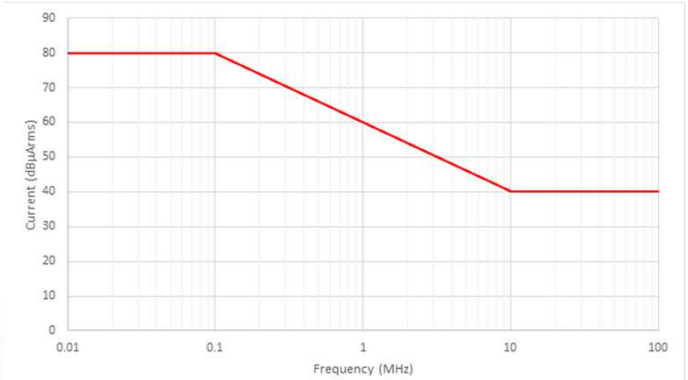
- SpW EMC performance characterization of the 3 SpW Boards with respect to radiated emission and susceptibility

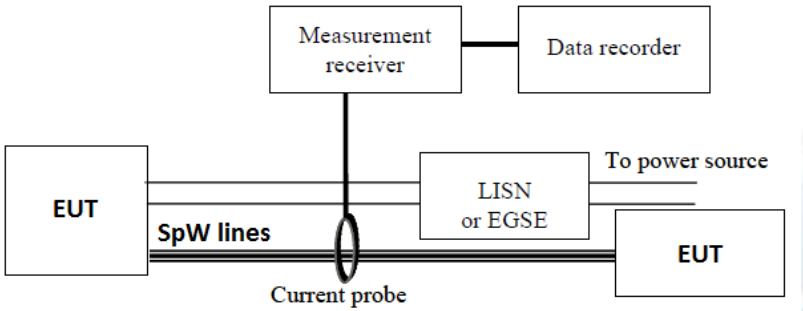




- *CE: Conducted Emission Test*

- The narrowband electric field radiated emissions from the specimen including interconnecting cables shall not exceed the specified limits (range 10 kHz and 400 MHz) defined in the Figure here-below:



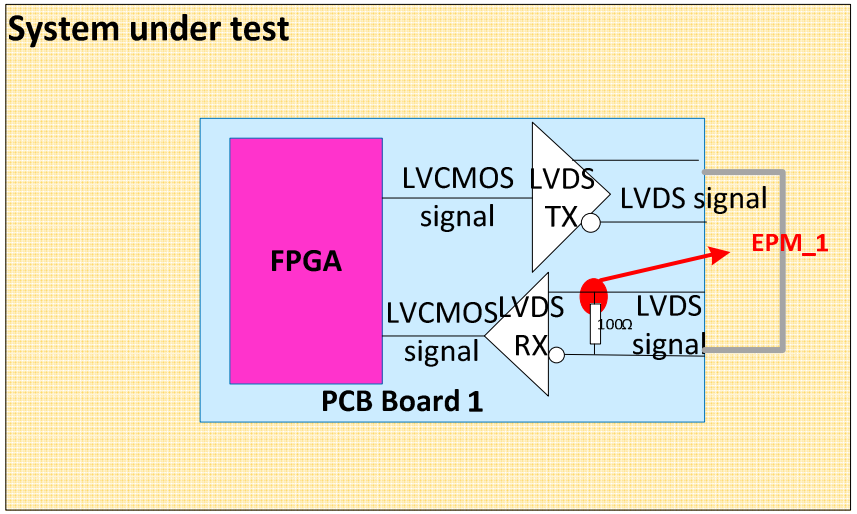


- *+ CS: Conducted susceptibility Test + RE-E: Radiated Emission, Electric field + RS-E: Radiated Susceptibility, Electric field*

Test procedure !

- **Thermal tests**
  - Verification of compliance status over the operational thermal temperature range
  - The Success and Failure criterions of the Thermal test shall be based on a BER test.
    - For the activity: tested at -30° C & +80° C

	Performance electrical Tests				
	BER				
Data-rate	2 Mbps	10 Mbps	100 Mbps	150 Mbps	200 Mbps
Ambient T°C		X	X	X	X
- 30 °C			X		X
+ 80 °C			X	X	X



Test results

- **Specific test board were developed by TAS-I to undergo the test procedure, verify the implementation compliance and cross-check the test procedure relevance**[18]
  - All done expect for EMC tests (scheduled week 50)
  - AC-CM tests modified: computed initially according to a specific impedance/inductance pattern which is not an actual fail/success criterion → a mask has been defined based on common mode conducted emission level instead
  - Edge Separation recorder for data rate of 200 Mbits/s, at Receiver Input (Soldered-Transceivers Board left, Socketed-Transceivers Board right)

Time	Edge Separation Recorded (Ambient Temperature)	Edge Separation Recorded (+3° C)	Edge Separation Recorded (Ambient Temperature)	Edge Separation Recorded (+3°C)
T_{S+D-}	4.02ns	2.96ns	2.62ns	3.01ns
T_{S+D+}	3.18ns	3.04ns	2.55ns	2.94ns
T_{S-D-}	3.33ns	3.23ns	2.63ns	3.06ns
T_{S-D+}	3.34ns	3.23ns	2.61ns	3.12ns
T_{D+S-}	3.06ns	3.06ns	2.82ns	3.06ns
T_{D+S+}	3.06ns	3.06ns	3.68ns	2.13ns
T_{D-S-}	2.13ns	2.16ns	2.72ns	2.01ns
T_{D-S+}	2.03ns	2.09ns	2.73ns	2.05ns
$T_{S+S-,@100}$	3.69ns	3.68ns	3.59ns	2.92ns
$T_{S+S-,@1000}$	3.76ns	3.71ns	3.59ns	2.89ns
$T_{S+S-,@4096}$	3.64ns	3.74ns	3.59ns	2.91ns
T_{S-S+}	3.52ns	2.74ns	3.64ns	2.85ns
T_{D-D+}	3.61ns	3.54ns	2.71ns	2.69ns
T_{D+D-}	3.72ns	3.64ns	3.68ns	3.68ns

Conclusion

- SpaceWire is a high-speed, low-voltage, network technology
- It needs to be designed & handled with care: not as straight-forward as a bus
- Each link can have its own characteristics (speed, transceiver, boards design, routing within the spacecraft, cable shielding policy, cable length, etc…)
- As for a RF link, it needs its own “link budget”: skew/jitter apportionment & specific check-ups

- This activity enabled defining a test procedure and characterized a test setup using representative elements: ESA CODEC & Gaisler Cobham transceivers (socketed or soldered and 2 separate boards)

- A key point: BER test can provide a confidence in the communication establishment in a specific configuration & environment but does not provide any margin figure nor provides an explanation in case of failure

- **Hence the need for thorough testing !**

- Test procedure & report will be available to the community

Thanks for your attention !