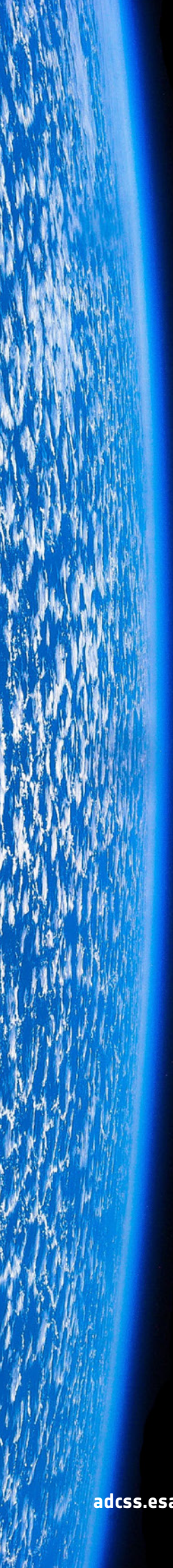
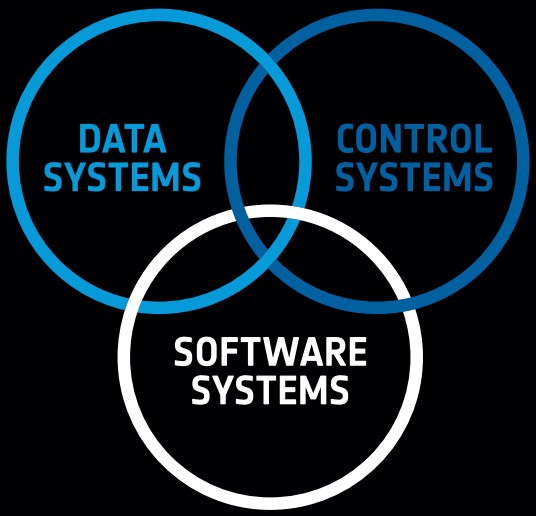


# adcss

## → 10th ESA WORKSHOP

**ESA/ESTEC**
**18-20 October 2016**

**avionics**
**data**
**control**
**software**
**systems**

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European Space Agency

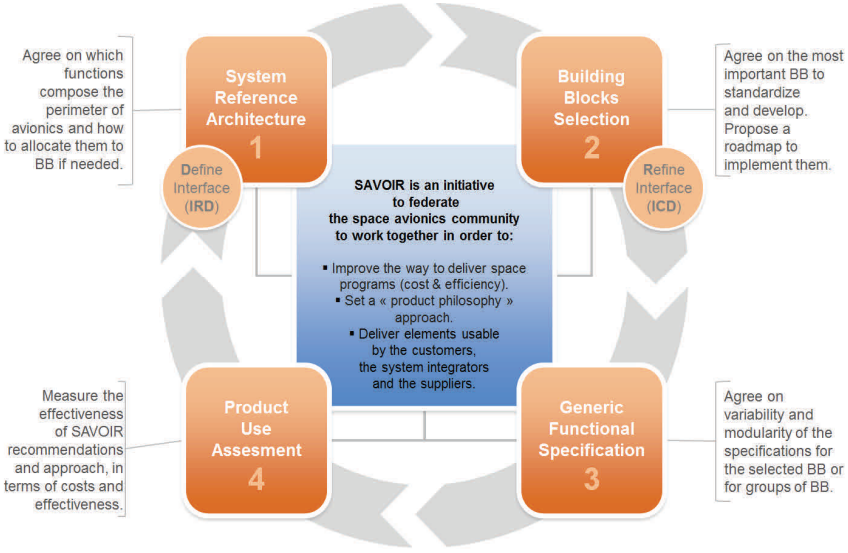
# SAVOIR

space avionics open interface architecture

**Space AVionics Open Interface aRchitecture is an initiative aiming at federating avionics communities in order to streamline avionics subsystems based on reference architectures, generic specifications and common build-in blocks**


## What are the objectives?

- To reduce the schedule and risk and thus cost of the avionics procurement and development, while preparing for the future
- To improve competitiveness of avionics suppliers
- To influence processes by standardizing at the right level in order to get equipment interchangeability (the topology remains specific to a project)
- To define the governance model to be used for the products, generic specifications, interface definition of the elements being produced under the SAVOIR initiative

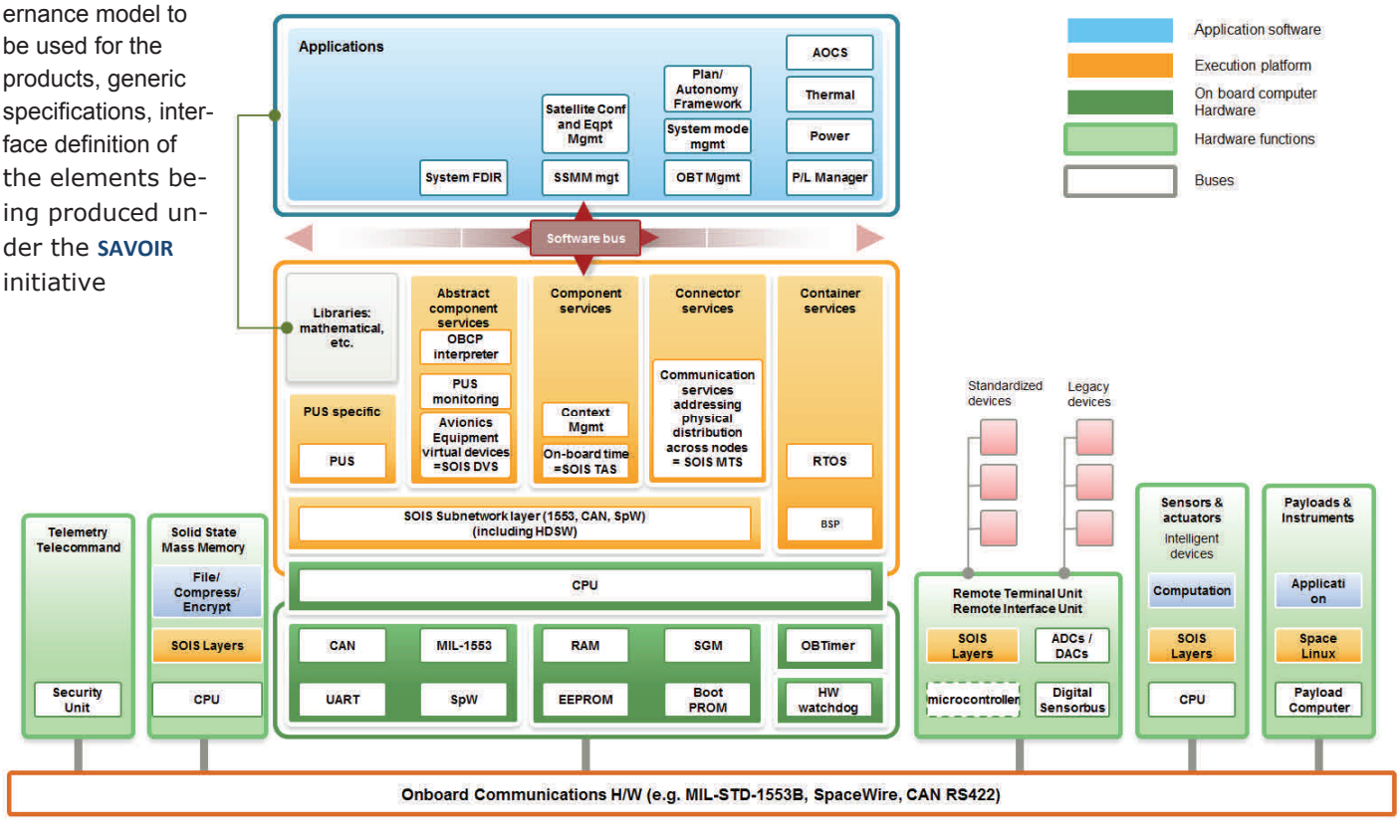



## What are the primary outputs of SAVOIR

- Reference avionics architectures for spacecraft platform hardware and software
- Generic specifications for units such as On-Board Computers and Remote Terminal Units
- A set of standard avionics external and internal interface specifications
- The definition of building blocks composing the architecture
- The functional specification of selected building blocks comprising the architecture
- The implementation of selected building blocks at the right TRL level

## What are the expected benefits of SAVOIR?

- For customers, streamline the procurement process of spacecraft avionics
- For system integrators, facilitate the integration of the spacecraft avionics
- For suppliers, prepare the technical conditions for a more efficient product line organization



# 10th ESA Workshop on Avionics, Data, Control and Software Systems

## ADCSS 2016


# Session Scope

## Tuesday 18 October 2016

## SAVOIR STATUS, HARMONISATION PROCESS of CRITICAL AVIONICS TECHNOLOGIES and MODEL BASED AVIONICS

### Background

A significant effort is being deployed by Agencies and Industry to streamline the development, validation and operation phases of spacecraft, with particular focus on the Avionics. This effort is being coordinated by ESA in the form of the "Spacecraft Avionics Open Interface Architecture" (SAVOIR) initiative. SAVOIR brings together ESA and industry experts in an open forum and is gaining significant momentum. Based on establishment of reference architectures, it provides the ground for the identification of building blocks interacting through standardised interfaces, service access points and protocols across hardware and software boundaries.

### Objective

The objective of this annual SAVOIR session is to update the avionics stakeholders with the progress done over the last year and to discuss the next steps.
A programme has been defined during the SAVOIR Advisory Group (SAG) meetings held in 2016.

- Status of the working groups (Masais, Union, Operability, handbooks)
- Result of the Avionics harmonisation
- Electronic Data Sheet
- Model Based Avionics

**Convenors:** J-L. Terraillon, K. Hjortnaes, Ph. Armbruster & A.Benoit (ESA/ESTEC)
**Coordinators:** J-L. Terraillon, J. Ilstad (ESA/ESTEC)

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## Wednesday 19 October 2016

## MEGA-CONSTELLATIONS, COMPACT SPACECRAFT AVIONICS and MIXED CRITICALITY SYSTEMS

### Background

The satellite market is evolving rapidly and concepts of mega-constellations involving 100's of satellites have been proposed and are in some cases currently under development. There are many challenges to overcome for such large constellations to become a reality. During the second day of ADCSS we shall touch upon particular aspects for what concerns the on-board data handling system requirements for these types of satellites.

The availability of multicore processors as well reconfigurable FPGAs for space, opens new possibilities to implement functions often processed locally at sensor or unit level to be executed either fully or partially in the central computer; such functions often belong to

different criticality domains (e.g. OBC and payload processing). Besides these possibilities, new challenges are also introduced, especially in ensuring that the various functions do not interfere with each other.

### Objective

The scope of the second day of ADCSS is focused on the challenges and opportunities of having higher integration of functions in to the on-board computer as opposed the more traditional distributed architecture. OBC equipment suppliers will give their views on challenges and opportunities with current state of the art building blocks and future needs. The last session of the day is dedicated to challenges on the execution of SW of mixed criticality on the same processor in particular on multi-cores CPU's.

The program for the 2nd day contains the following main sessions:

### Session 1: Avionics in mega constellations satellites

The view from industry and agency representatives will be given on the challenges to be overcome with mega-constellation satellites for what concerns the on-board data handling system.

**Convenors:** J.Ilstad (ESA/ESTEC)
**Coordinator:** G.Magistrati, J.Ilstad (ESA/ESTEC)

### Session 2: Compact on-board computer architectures

Invited talks from industry's leading on-board computer manufacturers will share their views on how the spacecraft development costs can benefit from building blocks enabling integration of more functions as part of the on-board computer.

### Round Table - Higher Integration - cost saving at the expence of reliability?

**Convenors:** G.Magistrati (ESA/ESTEC)

**Coordinator:** G.Magistrati, J.Ilstad (ESA/ESTEC)

### Session 3: Mixed criticality systems issues in relation to space craft avionics

Invited talks from industry and research institutes will introduce the challenges in mixing applications of different criticality on the same hardware device; the state of the art of the solutions identified to those challenges are also presented.

### Round Table - Mixed Critical Systems - are we ready for tomorrows platforms?

**Convenors:** M.Verhoef, J. Lopez Trescastro (ESA/ESTEC)
**Coordinators:** M.Verhoef, J.Ilstad, L.Fossati (ESA/ESTEC)

## THURSDAY 20 October (AM)

## AVIONICS SYSTEMS for EXPLORATION MISSIONS

### Background

The ESA exploration program comprises complex and challenging missions as well as technology development in leading areas. Exploration missions and technologies are ambitious and expensive and demand high performing avionics systems to realize them.

Missions range from the exploration of the planets, moons, and minor bodies (asteroids and comets). The most recent complex scenario is the one of the Moon village proposed by the ESA Director General.

In the area of technology, a new European Exploration Envelope Programme (E3P) will be presented by ESA in the 2016 Ministerial Council for approval. This program allocates for the time period 2017-2020 for technology development. It would replace MREP-2 and would play a key role for avionics systems of the future of exploration.

### Objective

The overall objective of this session are:

- To review the challenges and achievements from past successful exploration activities (missions, mission studies, research and development work, hardware developments, etc.) in the three areas of GNC, data handling and on-board software.
- To share the lessons learnt during the development, implementation and operational use of exploration missions and technologies in the area of avionics.
- To discuss the current avionics needs and requirements raised by the upcoming exploration missions and technology to interplanetary and small body destinations, and discuss shared priorities and possible roadmaps for future endeavours.
- To highlight problems and solutions in the areas of autonomy and FDIR of avionics systems for exploration missions

This session shall cover the 3 legs of avionics: GNC, data, and software and would allow to identify technological gaps where new avionics solutions for exploration need to be developed, or where existing ones need to be extended.

The missions and scenarios to target are the Moon exploration (including the upcoming technologies for the village and the planned space station in L2), as well as exploration of Mercury, Didymos asteroids, Mars, Jupiter, and Saturn. The session will end with a round table for discussion about Avionics Systems for Exploration Missions.

### Round Table - Avionics Systems for Exploration Missions

**Convenors**: Johann Bals (DLR), Michel Delpech (CNES), Guillermo Ortega (ESA/ESTEC)
**Coordinator:** Guillermo Ortega (ESA/ESTEC)

## THURSDAY 20 October (PM)

## Automated Code Generation for AOCS

### Background

AOCS design validations makes commonly use of model-based tools. These tools have been completed by Automated Code Generation (ACG) toolboxes which allow to produce SW code from simulation models. ACG is now used on several ESA satellite platforms (e.g. SGEO, Euclid, JUICE…) for generating (part of) the AOCS applicative SW starting from AOCS simulation models. This trend is currently being deployed in an increasing number of System and AOCS Prime companies of ESA member states.

### Objective

The use of ACG tools induces new rules on AOCS modelling activities and impacts the AOCS development cycle.

The objective of this ADCSS session is to investigate the impact of ACG use for ESA spacecraft AOCS as well as to share returns of experience on the following topics:

- AOCS development cycle, in particular AOCS validation, AOCS SW production and testing
- Modelling rules for ACG: do's and don't
- Tailoring of ECSS coding standards
- New borders between specification and code
- Modularity/versatility wrt mission specificities, industrial layout

### Round Table - Automated code generation for AOCS: return of experience, benefits and challenges

**Convenors:** B. Girouart, D. Sanchez de la Llana (ESA/ESTEC)

**Coordinator:** B. Girouart (ESA/ESTEC)

# ADCSS 2016 Timetable-Newton Conference Centre

| DAY 1 – Tuesday 18 October 2016 | | | |
|---|---|---|---|
| **Date** | **Title** | **Presenter** | **Session** |
| 18 October at 08:30 | Registration/coffee | Ms. Sinka, B. (ESA) | Welcome |
| 18 October at 10:00 | Welcome and Introduction | Mr. Hjortnaes, K. (ESA) | Welcome |
| 18 October at 10:20 | Logistics | Mr. Ilstad, J. (ESA) | Welcome |
| 18 October at 10:30 | SAVOIR Status/ Reference Architecture | Mr. Terraillon, J-L. (ESA) | SAVOIR |
| 18 October at 10:50 | SAVOIR-UNION & SAVOIR-MASAIS | Mr. Honvault, C. (ESA) | SAVOIR |
| 18 October at 11:20 | Generic OIRD | Mr. Accomazzo, A. (ESA) | SAVOIR |
| 18 October at 11:40 | SAVOIR Handbook | Mr. Hult, T. (RUAG Space) | SAVOIR |
| 18 October at 12:00 | FDIR Handbook | Dr. Verhoef, M. (ESA) | SAVOIR |
| 18 October at 12:20 | Electronic Data Sheets | Ms. Hernek, M. (ESA) | SAVOIR |
| 18 October at 12:40 | Generic RTU specification | Mr. Magistrati, G. (ESA) | SAVOIR |
| 18 October at 13:00 | Lunch Break | | |
| 18 October at 14:00 | The ESA Technology Harmonisation Process | Mr. Williams, E. (ESA) | Technology Harmonization |
| 18 October at 14:20 | Avionics roadmap | Mr. Terraillon, J-L. (ESA) | Technology Harmonization |
| 18 October at 14:40 | Data handling roadmap | Mr. Magistrati, G. (ESA) | Technology Harmonization |
| 18 October at 15:00 | Payload data handling roadmap | Mr. Trautner, R. (ESA) | Technology Harmonization |
| 18 October at 15:20 | Microelectronics roadmap | Mr. Fernandez-Leon, A. (ESA) | Technology Harmonization |
| 18 October at 15:40 | Exhibitors Flash Presentations | Exhibitors | |
| 18 October at 16:30 | Coffee Break | | |
| 18 October at 17:00 | Introduction | Mr. Terraillon, J-L. (ESA) | Model Based Avionics |
| 18 October at 17:05 | Model based Avionics roadmap and case studies | Mr. Rossignol , A.(Airbus Defence and Space) | Model Based Avionics |
| 18 October at 17:35 | Rationale, recent projects and future options for Model based Developments | Mr. Wortmann, A. (OHB) | Model Based Avionics |
| 18 October at 18:05 | Avionics and SW issues for MBSE | Mr. Garcia, G. (Thales Alenia Space) | Model Based Avionics |
| 18 October at 19:00 | Cocktail and Walking dinner- ESTEC Canteen Crabtail | | |

# ADCSS 2016 Timetable-Newton Conference Centre

| DAY 2 – Wednesday 19 October 2016 | | | |
|---|---|---|---|
| **Date** | **Title** | **Presenter** | **Session** |
| 19 October at 08:00 | Registration | Ms. B. Sinka (ESA) | |
| 19 October at 09:00 | Welcome and Introduction | Mr. Armbruster, Ph. (ESA) | Avionics in the context of mega constellations satellites |
| 19 October at 09:20 | Acquired experience on the development of 3 major constellations and challenges for future mega constellations | Mr. Charbonnel,Ph. & Mr. Provost-Grellier, A. (Thales Alenia Space, France) | Avionics in the context of mega constellations satellites |
| 19 October at 09:50 | Space Systems stakes and strategy for avionics in the context of mega constellation | Mr. Kervandal, E. & Mr. Notebaert, O. (Airbus Defence and Space) | Avionics in the context of mega constellations satellites |
| 19 October at 10:20 | Coffee and Exhibition | | |
| 19 October at 10:50 | Smart-OBC: integrating functions in the Platform Computer | Mr. Aranci, G. (Thales Alenia Italy) | Compact Onboard Computer Architectures |
| 19 October at 11:20 | The COMPASS OBC, paving the way for a centralised avionics architecture | Mr. Poupat, J-L.(Airbus Defence and Space) | Compact Onboard Computer Architectures |
| 19 October at 11:50 | Compact SAVOIR OBC | Mr. Sandin, P. & Mr. Hult, T.(RUAG Space) | Compact Onboard Computer Architectures |
| 19 October at 12:20 | Round Table - Higher integration - Cost saving at the expense of reliability? | | |
| 19 October at 13:00 | Lunch break | | |
| 19 October at 14:00 | Introduction | Mr. Verhoef, M. (ESA) | Mixed Critical systems issues in relation to spacecraft avionics |
| 19 October at 14:20 | Mixed-Criticality Systems (MCS): Introduction and State of Practice | Dr. Cazorla F.J. (Barcelona Supercomputing Centre and IIIA-CSIC) | Mixed Critical systems issues in relation to spacecraft avionics |
| 19 October at 15:00 | Mixed criticality and partition systems | Mr. Rossignol, A. (Airbus Defence and Space), Mr. Planche, L.(Astrium) | Mixed Critical systems issues in relation to spacecraft avionics |
| 19 October at 15:30 | Iridium Next STR S/W: a first step towards mixed criticality in OBSW | Mr. Veran, G. (Thales Alenia Space - France) | Mixed Critical systems issues in relation to spacecraft avionics |
| 19 October at 16:00 | TSP architectures for OBSW in CNES | Mr. Galizzi, J.(CNES) | Mixed Critical systems issues in relation to spacecraft avionics |
| 19 October at 16:30 | Coffee break- Exomars landing live coverage | | |
| 19 October at 17:15 | (On the way to) Success Stories From Non-Space Domains | Mr. Perez, J. (IK4-IKERLAN), Dr. Cazorla, F.J. (IIIA-CSIC and BSC) | Mixed Critical systems issues in relation to spacecraft avionics |
| 19 October at 18:00 | Round Table - Mixed Criticality Systems, are we ready for tomorrow's platforms? | Mr. Trescastro, J.L. (Flight Software Systems Section), Mr. Verhoef, M.(ESA) | Mixed Critical systems issues in relation to spacecraft avionics |
| 19 October at 18:30 | End of DAY 2 | | |

# ADCSS 2016 Timetable-Newton Conference Centre

| DAY 3 – Thursday 20 October 2016 | | | |
|---|---|---|---|
| **Date** | **Title** | **Presenter** | **Session** |
| 20 October at 09:00 | Welcome and Introduction | Dr.. G.H. Ortega (ESA) | Avionics Systems for Exploration Missions |
| 20 October at 09:15 | Avionics Systems for the Exploration of Asteroids and small moons | Dr. Mammarella, M. (GMV) | Avionics Systems for Exploration Missions |
| 20 October at 09:45 | Exploring the planets and avionics systems: challenges and opportunities | Mr. Tramutola, A. (Thales Alenia Space) | Avionics Systems for Exploration Missions |
| 20 October at 10:15 | Avionics Systems Technology for New Exploration Scenarios | Mr. G. H. Ortega (ESA), Mr. Bals J. (DL R), Mr. Delpeche M. (CNES) | Avionics Systems for Exploration Missions |
| 20 October at 10:45 | Coffee Break | | |
| 20 October at 11:15 | Low cost avionics systems for fast track missions to the planets | Mr. Tiago Hormigo (Spinworks) | Avionics Systems for Exploration Missions |
| 20 October at 11:45 | Autonomy and FDIR of avionics systems for exploration | Ms. Cristina Tato (SENER) | Avionics Systems for Exploration Missions |
| 20 October at 12:15 | Round table with introduction from ESA about Avionics Systems for Exploration Missions | Dr. G.H. Ortega (ESA) | Avionics Systems for Exploration Missions |
| 20 October at 13:00 | Lunch | | |
| 20 October at 14:00 | Introduction | Ms. Girouart, B. (ESA) | Automated Code Generation for AOCS |
| 20 October at 14:05 | Industrial and optimized auto-coding process for AOCS SW development in CD phase | Mr. Bourdon, J. (Airbus Defence and Space (F)) | Automated Code Generation for AOCS |
| 20 October at 14:30 | Model Based AOCS Design and Automatic Flight Code Generation: Experience and Future Development | Mr. Bodin, P. (OHB Sweden) | Automated Code Generation for AOCS |
| 20 October at 14:55 | From 1995(MINISAT) to 2016(EUCLID): Auto-coding evolution for different types of AOCS | Mr. Llorente , S.(SENER (Sp.)) | Automated Code Generation for AOCS |
| 20 October at 15:20 | Integration of automatic code generation in a AOCS development process: feedback and perspectives | Mr. Dandre, D. & Mr. G. Veran, G. (Thales Alenia Space (F)) | Automated Code Generation for AOCS |
| 20 October at 16:00 | Round Table - Automated code generation for AOCS: return of experience, benefits and challenges | Ms. Girouart, B. (ESA) | Automated Code Generation for AOCS |
| 20 October at 16:30 | End of ADCSS 2016 | | |

# 10th ESA Workshop on Avionics, Data, Control and Software Systems

**Tuesday 18 October 2016 - Thursday 20 October 2016**

**European Space Research and Technology Centre (ESTEC)**

# Programme

# Table of contents

# Tuesday 18 October 2016

## Registration/coffee - Newton Conference Center (08:30-10:00)

**- Presenters: Ms. SINKA, Bertilla (ESA/ESTEC- Data Systems Division)**

## Welcome to ADCSS 2016 - Newton Conference Center (10:00-10:20)

**- Presenters: Mr. HJORTNAES, Kjeld (ESA/ESTEC -Head of Software Systems Division)**

## Logistics - Newton Conference Center (10:20-10:30)

**- Presenters: Mr. ILSTAD, Jørgen (ESA/ESTEC-Data Systems Division)**

## Session 1 - SAVOIR STATUS and ONGOING ACTIVITIES - Newton Conference Center (10:30-13:00)

**- Conveners: Mr. TERRAILLON, Jean-Loup (ESA/ESTEC- Software Systems Division)**

| time | title |
|---|---|
| 10:30 | **SAVOIR Status/ Reference Architecture (00h20')**<br>*Presenter: Mr. TERRAILLON, Jean-Loup (ESA/ESTEC- Software Systems Division)*<br>The presentation will introduce the Space Avionics Open Interface (SAVOIR) initiative, the process, the perimeter, the main outputs, the reviews, the way that Savoir documents are used in ESA projects, and the status on the workplan, as an introduction to the following working group specific presentations. |
| 10:50 | **SAVOIR-UNION and SAVOIR-MASAIS (00h30')**<br>*Presenter: Mr. HONVAULT, Christophe (ESA/ESTEC- Head of Software Systems Engineering Section)*<br>The SAVOIR-MASAIS Working Group aims at defining the functional, performance, operational and interface requirements of the Avionics System Reference Architecture Data Storage function and the definition of standard services and interfaces to manage data on-board.<br>The SAVOIR-UNION Working Group aims at defining the functional, performance and interface requirements of the Avionics System Reference Architecture functional links.<br>The status of these two Working Groups supported by TRP activities will be presented. |
| 11:20 | **Generic OIRD (00h20')**<br>*Presenter: Mr. ACCOMAZZO, Andrea (ESA/ESOC- Head of Solar and Planetary Missions Division)*<br>The presentation will recall the need for a generic OIRD as a way to reduce the variability of our avionics systems with regards to operability. It will present the first draft document, the results of the initial review, and will introduce the way that the document will be modified in order to take into account the results of the review, as well as the plan for applicability. |
| 11:40 | **SAVOIR Handbook (00h20')**<br>*Presenter: Mr. HULT, Torbjörn (RUAG Space)*<br>The SAVOIR architecture is now quite established, with a couple of documents that have passed public review and were released during spring 2016. The documentation this far includes descriptions and specifications but there is also a need to have documentation that more describes how to use the functions and features of SAVOIR in real projects. A SAVOIR Data Handling handbook, dealing with functions described in the SAVOIR Functional Reference Architecture document, is now prepared in a first issue. The presentation will describe the contents of the handbook and give a few examples on how to solve problems and open points quite frequently appearing in projects. |
| 12:00 | **FDIR Handbook (00h20')**<br>*Presenter: Mr. VERHOEF, Marcel (ESA/ESTEC- Software Systems Division)*<br>The need for consolidation of FDIR terminology and methodology was clearly identified at the FDIR special session that was held at ADCSS in 2015. As a follow-up activity, ESA has taken the initiative to create a FDIR handbook, as a first step towards this consolidation, from an explicit multi-disciplinary perspective. This talk will address the scope and foreseen content of the handbook and its relation to past and present R&D activities and experiences gained from ESA projects. We present the work plan and the approach to gain maturity and momentum of the handbook, in the context of SAVOIR and ECSS. |

| | |
|---|---|
| 12:20 | **Electronic Data Sheets (00h20')**<br>*Presenter: Ms. HERNEK, Maria (ESA/ESTEC- Head of Flight Software Systems Section)*<br>The CCSDS is developing a standard set of communication services to support the onboard applications which are in turn supported by communication protocols. The idea of “plug and play” avionics units is a major goal while enabling use of standard building blocks and reuse.<br>A major step in this direction is through the definition of Electronic Data Sheets (EDS). The presentation will address the current status of the international standardisation, the activities in ESA and a view of future steps. |
| 12:40 | **Generic RTU specification (00h20')**<br>*Presenter: Mr. MAGISTRATI, Giorgio (ESA/ESTEC-Head of On-Board Computers Handling Section)*<br>The SAVOIR initiative has the final mission to achieve standardization and harmonization of Space products in Europe. The goal is pursued by means of technical notes, product specifications and handbooks. In term of product specifications after the Generic OBC Specification ( SAVOIR-GS-001) and Flight Computer Initialisation Sequence Generic Specification (SAVOIR-GS-002) , issued as final version in 2016 after a public review, the Savoir Advisory Group is currently involved in the finalization of a SAVOIR RTU Functional and Operability Requirements. The Remote Terminal Unit (RTU) is an Avionics building blocks that provides functions such as collection of housekeeping data, commanding of pulse commands, interfacing to sensors & actuators, and in general to devices which do not have a direct link to the OBC via the spacecraft command & control bus. The presentation will give an overview of the current status of the specification. |

## Lunch Break - ESTEC Canteen (13:00-14:00)

## Session 2: Results of the ESA Technology Harmonisation Meetings - Newton Conference Center (14:00-15:40)

- **Conveners: Mr. TERRAILLON, Jean-Loup (ESA/ESTEC-Software Systems Division)**

time title

| | |
|---|---|
| 14:00 | **The ESA Technology Harmonisation Process (00h20')**<br>*Presenter: Mr. WILLIAMS, Edmund (ESA/ESTEC- Head of Technology Planning Section)* |
| 14:20 | **Avionics roadmap (00h20')**<br>*Presenter: Mr. TERRAILLON, Jean-Loup (ESA/ESTEC- Software Systems Division)*<br>Out of the subsequent Harmonisation roadmap, the main areas of research will be presented, with highlights on the activities that have received the highest priorities, in order to show the trends in avionics R&D at system level. The following sectorial presentations will address the domain of the specific disciplines of avionics. |
| 14:40 | **Data handling roadmap (00h20')**<br>*Presenter: Mr. MAGISTRATI, Giorgio (ESA/ESTEC- Head of On-Board Computers Data Handling)*<br>In 2016, a new cycle of technology harmonisation activities took place for several avionics technology areas. ESA, in collaboration with the Technology Harmonisation Advisory Group (THAG), has established a new R&D roadmap for Data Systems and On-Board Computers (DSOBC) technologies covering the 2016-2023 timeframe. Data Systems and On-board Computers encompass a vast range of functional blocks that include Telecommand and Telemetry Modules, On-Board computers, Data Storage and Mass memories, Remote Terminal Units, Communication protocols, Busses and Wireless Technologies for P/F. These elements are common to all projects and are subject to a demanding set of evolving requirements from Science, Exploration, Earth Observation and Telecom missions. In this presentation an overview of the new harmonised roadmap for DSOBC architecture, building blocks , interfaces and technologies will be presented. Key elements as reference designs and microcontroller for space will be highlighted. |
| 15:00 | **Payload data handling roadmap (00h20')**<br>*Presenter: Dr. TRAUTNER, Roland (ESA/ESTEC- Data Systems Division)*<br>In 2016, a new cycle of technology harmonisation activities took place for several avionics technology areas. ESA, in collaboration with the Technology Harmonisation Advisory Group (THAG), has established a new R&D roadmap for On-board Payload Data Processing (OBPDP) technologies covering the 2016-2023 timeframe. In this roadmap, activities for the domains of Digital Signal Processors, High Speed Networks, Payload Mass Memories, I/O and DAQ modules, Data Compression, Reconfigurable P/L Processors, Payload Support Software, and Wireless Technologies for P/L have been defined together with associated scope, priority, approximate funding level and other aspects. In this presentation, an overview of the new harmonised roadmap for OBPDP technologies will be presented. Key development lines and associated activity sequences will be pointed out. Critical technologies for European competitiveness and non-dependence will be highlighted, and challenges for the roadmap implementation will be explained. |

| | |
|---|---|
| 15:20 | **Microelectronics roadmap (00h20')**<br>*Presenter: Mr. FERNANDEZ-LEON, Agustin (ESA/ESTEC-Head of the Microelectronics Section)* |

## Session 3 - Exhibitors Flash Presentations - Newton Conference Center (15:40-16:30)

***Short introductory talks by the exhibitors.***

**- Conveners: Mr. Ilstad, Jørgen (ESA/ESTEC- Data Systems Division)**

time title

| | |
|---|---|
| 15:40 | **Exhibitor 1 - TTTech (00h05')**<br>Deterministic Ethernet as basis for distributed IMA and mixed-criticality systems. |
| 15:45 | **Exhibitor 2 - Cobham Gaisler (00h05')** |
| 15:50 | **Exhibitor 3 - Ramon-Chips (00h05')** |
| 15:55 | **Exhibitor 4 - Microchip Atmel (00h05')** |
| 16:00 | **Exhibitor 5 - Technobis (00h05')** |
| 16:05 | **Exhibitor 6 - Embedded-Brains (00h05')** |
| 16:10 | **Exhibitor 7 - Skylabs (00h05')** |
| 16:15 | **Exhibitor 8 - ARM (00h10')** |

## Coffee Break - Newton Conference Center (16:30-17:00)

## Session 4 - Model Based Avionics - Newton Conference Center (17:00-18:40)

**- Conveners: Mr. TERRAILLON, Jean-Loup (ESA/ESTEC-Software Systems Division)**

time title

| | |
|---|---|
| 17:00 | **Introduction (00h05')**<br>*Presenter: Mr. TERRAILLON, Jean-Loup (ESA/ESTEC- Software Systems Division)* |
| 17:05 | **Model based Avionics roadmap and case studies (00h30')**<br>*Presenter: Mr. ROSSIGNOL, Alain (Airbus Defence and Space)*<br>Functional avionics for a Satellite means architecture and technologies targeting definition, design, implementation and validation in Computers & SW intensive equipment of functions and algorithms which are coming from various system levels (complete system, sub-systems, platform, equipment, boards), from very different functional chains (Command & Control, Flight management, GNC, Image processing, payload and instruments data processing…), with a large variety of criticality and safety levels.<br><br>On avionics architecture and computing domain, initial requirements and design engineering of new products with computers, on-board software, system functions and applications algorithms (GNC, Autonomy, Mission planning, payload data processing), sensors and actuators, payloads are key for mastering cost, schedule, quality and risks of the avionics development.<br><br>The main objectives of this project are first to improve the early maturity of the On-Board Functional Avionic requirements and design, in particular through an improvement of the interfaces between Operations, FDIR and System to Software, to make available to the Avionics architects a set of methods and tools which are adapted to the different operational situations they are facing, to better address and manage the system complexity, like the dependencies inside the architectures and in between, and for the interface definitions and finally to provide and assess process(es), methodology (ies) and tooling to design a spacecraft avionics architecture using MBSE controlling and reducing the project risks and costs, including flexibility of the avionics architecture to cover different similar mission profiles. It will also propose recommendation for links to the others MBSE initiative for full spacecraft system, other sub-systems and ground systems.<br><br>The presentation will introduce main expectations out of a successful MBSE implementation in this domain, experience feedbacks of first use cases, main trends for the next step. |

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| 17:35 | **Rationale, recent projects and future options for Model Based Developments (00h30')**<br>*Presenter: Mr. WORTMANN, Andreas (OHB)*<br>The presentation motivates the application of model based approaches in the development process of avionics. The fundamental ideas and rationales are given, benefits are derived and common counter arguments are discussed.<br><br>The presentation covers a wide range of model based approaches and developments as employed at OHB. The focus is on the development of avionic systems.<br><br>A non-comprehensive list of activities that apply model based development approaches at OHB is presented. The selection covers the full range from theoretical mathematical analysis models to advanced integrated development environments utilized for (software) implementation.<br><br>A set of such examples is taken from ongoing (commercial) projects. The successful application of the selected activities is proven in practice. A second set of examples represents research projects and show potential ways forward in utilizing and advancing model based approaches. |
| 18:05 | **Application of MBSE to avionics and software development: achievements and future goals (00h30')**<br>*Presenter: Mr. PANUNZIO, Marco (Thales Alenia)*<br>Model-Based System Engineering applied to Avionics has recently became a reality in Thales Alenia Space, in addition to the already mature model-based engineering practices adopted on OBSW side. This was made possible thanks to the deployment of a mature and efficient tooling based on Melody Advance, the Thales toolset recently released as Open-source software under the name “Capella”. For the past 3 years, TAS engineers have been using the capabilities of this suitable tool together with appropriate methodologies to smoothly move from a document-centric process to a model-centric process, relying on documentation and code generation, and model-to-model transformations. To foster the deployment of this approach on actual programs, several R&D activities are on-going to extend the Model Based approach to all disciplines, from Product Line Engineering, to V&V activities, including FDIR, and also relationship with the Satellite Data Base and test & simulation bench development. |

## Coktail and Walking dinner - ESTEC Canteen- Crabtail (19:00-22:00)

# Wednesday 19 October 2016

## Registration - Newton Conference Center (08:00-09:00)

- **Conveners: Ms. Sinka, Bertilla (ESA/ESTEC- Data Systems Division)**

## Session 1 - Avionics in the context of mega constellations satellites - Newton Conference Center (09:00-10:20)

- **Conveners: Mr. Ilstad, Jørgen (ESA/ESTEC- Data Systems Division)**

| time | title |
|---|---|
| 09:00 | **Welcome and Introduction (00h20')**<br>*Presenter: Mr. ARMBRUSTER, Philippe (ESA/ESTEC- Head of Data Systems Division)*<br>New missions and advanced development paradigms lead to compress schedules while minimising costs. When applied to Avionics and on-board data handling in particular, these objectives can be attained with more compact units integrating more functions. This introductory presentation will outline challenges we are confronted to and establish a list of contributions the day's sessions are expected to provide. |
| 09:20 | **Acquired experience on the development of 3 major constellations and challenges for future mega constellations (00h30')**<br>*Presenters: Mr. CHARBONNEL, Philippe (Thales Alenia France), PROVOST-GRELLIER, Antoine (Thales Alenia Space - France)*<br>In the past 10 years, Thales Alenia Space has developed the three major commercial constellations: GLOBALSTAR2, O3b and IRIDIUM NEXT representing 125 spacecraft on LEO and MEO orbits. Each development has required Avionics enhancement in order to meet the objectives of recurrent cost, radiation environment, in-flight autonomy, or high rate production. Further enhancements of the avionics are being studied to face the new challenges required by the changing Telecom constellation market.<br><br>In the first part of the presentation we will review the design and process upgrades applied onto the avionics for these three constellations. In particular we will address the design optimisation, the use of COTS components, the higher integration of the electronics, the validation optimisation and the Satellite autonomy improvement.<br><br>The second part of the presentation will deal with the upcoming challenges raised by the mega constellations market. The increased cost saving objectives and need for enhanced on-board autonomy leads to develop new avionics solutions within reduced duration. |
| 09:50 | **Space Systems stakes and strategy for avionics in the context of mega constellation (00h30')**<br>*Presenters: Mr. KERVANDAL, Erwan, Mr. NOTEBAERT, Olivier (Airbus Defence and Space)*<br>In the last few years, interest in constellations of satellites has significantly increased, especially in the context of the so-called New Space economy. Indeed, many commercial ventures or entrepreneurs now consider constellations as an efficient and affordable way to provide large access to pictures of Earth, world-wide access to the Internet, and many other services relying on data broadcast, collection or fusion. This new evolution in space industry mainly results from two game-changers: a more affordable access to space, proposed by companies such as SpaceX for instance, and most importantly availability of powerful, and yet cheap, COTS components, designed to be robust enough to radiations through mitigation techniques.<br>However, manufacturing, validating, launching and then operating satellites in large quantity is still a challenging endeavour. This paper will focus on the avionics subsystem that has been directly impacted by emergence of powerful COTS components. In particular, it will discuss several topics such as use of COTS from mainstream to space industry or Fault Detection, Identification and Recovery and Operations strategies. |

## Coffee and Exhibition - Newton Conference Center (10:20-10:50)

## Session 2 - Compact Onboard Computer Architectures - Newton Conference Center (10:50-12:20)

**- Conveners: Mr. Magistrati, Giorgio (ESA/ESTEC- Head of On-Board Computers & Data Handling Section)**

| time | title |
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| 10:50 | **Smart-OBC: integrating functions in the Platform Computer (00h30')**<br>*Presenter: Mr. ARANCI, Gianluca (Thales Alenia Italy)*<br>In the continuous trend to miniaturize electronic equipment for space applications, Thales Alenia Space has managed the evolution of the On Board Computer integrating more functions and features as soon as relevant key technologies become available. These developments permitted to improve competitiveness, mass, volume and power consumption budgets at system level. Further enhancements of the OBC are currently on going, in a trend similar to the one observed in the consumer electronics leading to the Smartphone, where many functions and sensors, formerly spread over many gadgets, have been integrated in a single compact product.<br><br>In the first part of the presentation the author recall a brief history of platform computer evolution in the last 20 years, showing the convergence from many units (Computers and Remote Terminals) to a single one.<br><br>The second part shows current developments at TASI, focused to integrate GNSS Receiver, Gyroscope and Mass Memory storage functions in the Platform computer. A synthesis of Pros and Cons are presented, as experienced during the course of the development.<br><br>The last section part of the presentation deal with new perspectives offered by introduction of COTS, Multicore Processor, Ultra Large Reprogrammable FPGA and deep sub-micron silicon technology. The challenges related to this opportunities are briefly analysed from the equipment manufacturer point of view. |
| 11:20 | **The COMPASS OBC, paving the way for a centralised avionics architecture (00h30')**<br>*Presenter: Mr. POUPAT, Jean-Luc (Airbus Defence and Space)*<br>In the frame of its continuous innovation process, Airbus Defence and Space, - Space Equipment Division is working on a next generation of on board computer (OBC) to drastically drop down the avionics HW acquisition cost.<br>This product, named COMPASS, is more than an OBC, it is a centralized avionics.<br>COMPASS (Centralized Open & Modular Processing Avionics & Space Sensors) relies on a centralized high performance processing core, associated to a specific SW architecture allowing the overall avionics processing to be performed in this single chip.<br>Compact design, light, with minimized power consumption, COMPASS is not jeopardizing the reliability and rely on adapted assurance quality management to bring to the market the most efficient centralized avionics unit. |

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| 11:50 | **Compact SAVOIR OBC (00h30')**<br>*Presenters: Mr. SANDIN, Patrik (RUAG Space AB), Mr. HULT, Torbjörn (RUAG Space)*<br>RUAG Space has more than 30 years of experience in developing high-reliable launcher and satellite on-board command and data-handling electronics. Through this experience the following key items exists:<br>• a design database with existing & qualified SW and FPGA IP-modules<br>• an internal certified and customer audited design process for high-reliable electronics<br>• a high quality and high efficiency electronics production facility already today capable of producing large series industrial electronics.<br><br>The RUAG Space approach to mega constellation satellite electronics is to:<br>• reuse the existing design data-base, design processes and production facility<br>• use a mix of high-rel components and up-screened commercial components<br><br>This enables us to offer:<br>• reliable data handling products with low risk<br>• significantly lower prices and higher performance than the corresponding traditional high-reliable Products<br><br>RUAG Space offers a very compact and reliable SAVOIR compliant On-board Computer (OBC) with integrated GNSS receiver and security functions for mega constellations as a complement to our traditional OBC based on high-rel components.<br><br>The mega constellation OBC is designed for 5-7 years lifetime in LEO. Parts procurement, manufacturing and production test strategy is optimised for batches of unit allowing the price per unit to be kept at a fraction of the traditional OBC. Due to the use of state-of-the-art commercial technology the mega constellation OBC provides processing performance in excess of 10 times that of the traditional OBC still providing the same functionality although the number of interfaces is optimised to fit the needs of a small satellite. RUAG Space is developing the OBC for mega constellations product, partially funded by ARTES for specific areas. |

## Round Table - Higher integration - Cost saving at the expense of reliability? - Newton Conference Center (12:20-13:00)

**- Conveners: Mr. Magistrati, Giorgio (ESA/ESTEC- Head of On-Board Computers & Data Handling Section)**

time title

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| 12:20 | **Round Table - Higher integration, cost saving at the expense of reliability? (00h40')**<br>The scope of the second day of ADCSS is focused on the challenges and opportunities of having higher integration of functions in to the on-board computer as opposed the more traditional distributed architecture. OBC equipment suppliers will give their views on challenges and opportunities with current state of the art building blocks and future needs. The following topics will addressed in the round table:<br><br>- How will moving to a more centralised and integrated avionics architecture affect testing, and is it contributing to costs saving? As an example; integrating functions into to the OBC effectively moves testing of unit functionality, e.g. provided be Start Trackers or Internal Measurement Unit supplier, from system level testing to become the responsibility of the OBC supplier.<br><br>- It is considered mandatory to calculate the reliability of the avionics unit, however at present there is insufficient reliability data on use of COTS components and technologies (e.g. use of ceramic vs. plastic packaging) to be able to estimate unit reliability. How do we best ensure that the introduction of COTS parts do not adversely affect the unit reliability? |

## Lunch Break - ESTEC Canteen (13:00-14:00)

## Session 3 - Mixed Critical systems issues in relation to spacecraft avionics - Newton Conference Center (14:00-18:00)

**- Conveners: Mr. Trescastro Lopez, Jorge (ESA/ESTEC- Software Systems Division); Dr. Verhoef, Marcel (ESA/ESTEC- Software Systems Division)**

time title

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| 14:00 | **Introduction (00h20')**<br>*Presenter: Mr. VERHOEF, Marcel (ESA/ESTEC- Software Systems Division)* |
| 14:20 | **Mixed-Criticality Systems (MCS): Introduction and State of Practice (00h40')**<br>*Presenter: Dr. CAZORLA, Francisco J. (Barcelona Supercomputing Center and IIIA-CSIC)*<br>Across all real-time domains companies aim at increasing their competitive edge by offering additional functionalities and services on every new product release. With the aim of reducing costs, functionalities with different criticalities are executed sharing various hardware components. However, without appropriate preconditions, integrating mixed-criticality functionalities onto the same platform can significantly increase certification costs. This overall situation is compounded with the on-going transition towards multicore and many core systems.<br><br>In this talk I will introduce and review different existing interpretations of mixed-criticality, which has been indistinctly applied to timing, safety and security, among others. I will also discuss some concepts in existing standards in each application domain that help developing in a cost-reasonable manner mixed-criticality systems. This includes freedom from interference between software components in automotive domains and software Time and Space partitioning in Integrated Modular Avionics. I will also discuss how the use of multicore processors as the baseline computing platform in these real-time domains challenges certified mixed criticality execution. Finally I will cover some of the current proposals to reduce certification cost in mixed-criticality multicores. |
| 15:00 | **Mixed criticality and partition systems (00h30')**<br>*Presenters: Mr. ROSSIGNOL, Alain (Airbus Defence and Space), Mr. PLANCHE, Luc (Astrium)*<br>After R&D studies on Integrated Modular Avionics (IMA) architecture and process, after definition and development of Time & Space Partitioning solutions with Hypervisors & Separation Kernels, the first space operational use cases are starting, with the need to maximize the integration of different functions & sensors software inside the same computer. Depending on the mission and the industrial organization, the different application software running in the different partitions could come from different companies or teams with different levels of maturity. As for aeronautical first IMA generation, in order to simplify the first partitioning deployments, only a unique criticality approach is applied on all software components and partitions in the same computer.<br>In future projects we are targeting to enlarge the solution with mixed criticality application software in the different partitions, taking also benefits from multicore processors solutions and also to consider, in some specific use cases, a set of data security needs and requirements.<br>The presentation will introduce the current status on recent R&D and first deployment, and will address stakes for the next step with mixed criticality systems. |
| 15:30 | **Iridium Next STR S/W: a first step towards mixed criticality in OBSW (00h30')**<br>*Presenter: Mr. VERAN, Guillaume (Thales Alenia Space - France)*<br>The migration of spacecraft functions from hardware to software together with a higher centralization is one of the current ways to reduce the cost of spacecraft avionics. This requires to manage mixed criticality software in the main platform computer. The integration of a star tracker software (MHSTR SW) in Iridium Next platform software was a major step in this direction for TAS-F.<br><br>This presentation will first describe this integration, in particular the MHSTR SW constraints (risks, timing, metrics..), the management of the interfaces between the MHSTR SW and the OBSW and the integration and V&V strategy. Then the modifications implemented on TAS internal RTOS (OSTRALES) to offer a first level of time and space partitioning will be detailed. Finally the failure management and associated FDIR strategy for the partitioned MHSTR SW will be presented.<br><br>After this industrial return of experience, the discussion will address further challenges and perspectives in the field of “mixed criticality” software. |
| 16:00 | **TSP architectures for OBSW in CNES (00h30')**<br>*Presenter: Mr. GALIZZI, Julien (CNES)*<br>The lessons learnt from the CNES projects are that the institutes involved in the payload developments have to systematically develop general “non-scientific” features, such as boot, platform interface, FDIR, I/O, timing, mass memory interface, etc. CNES have therefore initiated some years ago generic developments in order to offer off-the-shelf building blocks that could be easily reused with a low level of adaptation effort, aiming therefore at decreasing the cost of the mission, and increasing the reliability of the payload developments. The institutes can consequently concentrate their efforts on real science, high degree of expertise, especially on the science mission on-board software application part rather than “housekeeping” features. The presentation will describe the technical choices that have been made in order to provide a high level of genericity enabling a clear and effective decoupling between “housekeeping” and science, thanks to Time & Space Partitioning. It will provide status of development of the various building blocks, including visibility on current real but also future use cases and how TSP could efficiently help to solve budget constraints and to optimize the avionics architecture. |

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| 16:30 | Coffee break and live coverage of Exomars landing (00h45') |
| 17:15 | **(On the way to) Success Stories From Non-Space Domains (00h45')**<br>*Presenters: Mr. PEREZ, Jon (IK4-IKERLAN), Dr. CAZORLA, Francisco J. (IIIA-CSIC and BSC)*<br>The development of mixed-criticality systems that integrate applications of different criticality (e.g., safety) in a single embedded system can provide multiple benefits such as product cost-size-weight reduction, reliability increase and scalability. However, the integration of applications of different levels of criticality in a single embedded system leads to several challenges with respect to current safety certification standards.<br><br>During the last 6 years, within several European research projects, IK4-IKERLAN has leaded the definition of several research level 'safety concepts' for different safety standards (e.g., IEC-61508 industrial, EN-5012X railway, ISO-26262 automotive) assessed by external certification authorities. Each 'safety concept' describes, for a given safety application, the safety techniques and strategies that enable the usage of multicore devices with or without hypervisors (e.g. XtratuM). The analysis, definition and external assessment of such strategies and techniques, has paved the way towards current industrial projects: (1) we have integrated multicore and hypervisor technology into a wind-turbine control system; (2) we are developing an IEC-61508 mixed-criticality protection system based on a COTS multicore device and (3) we are collaborating on exporting and extending the lessons learnt from the integrated architectures to other sectors such as railway domain. This talk will dig deeper into the aforementioned technical topics and explain IK4-IKERLAN roadmap to a successful research and industrial developments story. |

## Round Table - Mixed Criticality Systems, are we ready for tomorrow's platforms? - Newton Conference Center (18:00-18:40)

**- Conveners: Mr. Lopez Trescastro, Jorge (ESA/ESTEC-Software Systems Division); Dr. Verhoef, Marcel (ESA/ESTEC-Software Systems Division)**

# Thursday 20 October 2016

## Session 1 - Avionics Systems for Exploration Missions - Newton Conference Center (09:00-12:15)

**- Conveners: Dr. Hernando Ortega, Guillermo (ESA/ESTEC-Head Guidance, Navigation and Control Section)**

| time | title |
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| 09:00 | **Welcome and introduction (00h15')**<br>*Presenter: Mr. GUILLERMO, Ortega Hernando (ESA/ESTEC-Head of Guidance, Navigation and Control Section)* |
| 09:15 | **Avionics Systems for the Exploration of Asteroids and small moons (00h30')**<br>*Presenter: Dr. MAMMARELLA, Marco (GMV)*<br>The Vision Based Navigation will be one of the key technologies in future ESA missions. The maturation of the technology is the essential issue required for acquiring confidence in this innovative and crucial navigation system. The discussion that GMV intend to present will be focused on the need of HW/SW co-design carried out to develop mature prototype bread-boarding and focused to reach the requirements of the GNC technology.<br>The fundamental step is to identify the real needs of the GNC in term of performance and frequency of operations taking into account Vision Based techniques available, the second step is to bring the initially developed and validated through simulation software to representative hardware where the Vision Based Navigation has to fulfil Real-Time performance maintaining the accuracy demonstrated in simulation. In this discussion GMV will bring as example the actual developments in AIM, PILOT, and CAM-PHOR-VNAV, emphasizing the different architectures and the requirements driving the selection of the architectures validation steps foreseen. Furthermore the problematics of using HW in the loop will be discussed. |
| 09:45 | **Exploring the planets and avionics systems: challenges and opportunities (00h30')**<br>*Presenter: Mr. TRAMUTOLA, Antonio (Thales Alenia Space)*<br>Exploration of planets is part of the space exploration of celestial structures of the outer space. Once a planet has been identified by astronomers and scientists as a target environment to be deeply analyzed, the technology needed to reach the objective are studied and developed by the industries. Complex space systems have to be designed to perform cruise, approach, landing and surface exploration, taking also into account stringent autonomy requirements. As a consequence the configuration of these systems is composed by modules with different functions connected each other in a composite spacecraft. Carrier or Orbiter module, Descent module and Rover module are the elements of the Exomars mission; Orbiter vehicle, Earth Return Vehicle, Earth Return Capsule plus Lander Platform and Lunar/Mars Ascent Vehicle are the modules designed in the Lunar Polar sample return and for Mars sample and return missions.<br><br>As a consequence the avionic system design has to consider this modular structure distributing properly the avionic functions (processing, communication, data handling, power distribution and autonomy) among the designed building blocks according to the mission needs. Key requirements for the exploration have to be considered in the avionic design: low power consumption, minimum mass, high computational capability, and reliable communication systems able to perform also Direct to Earth communication for command uplink and fast communication with orbiters for high data rate telemetry downlink.<br><br>Requirements inspire new technologies like Vision Based Navigation tailored to the different mission phases that provides high level of autonomy and specific sensors (radar, altimeters, LIDAR) integrated in compact avionic architectures. These technologies should possibly be based on COTS platforms able to provide high computational performance and significant cost reduction.<br>These new avionic platforms could be extended to mission scenario like Active Debris Removal or Rendezvous and Docking or Earth Observation providing opportunity for cost reduction and standardization of some key components. |
| 10:15 | **Avionics Systems Technology for New Exploration Scenarios (00h30')**<br>*Presenters: Dr. ORTEGA, Guillermo Hernando (ESA/ESTEC-Head of Guidance, Navigation and Control Section), Mr. J., Bals (DLR), Mr. M., Delpeche (CNES)*<br>Robotics and human space exploration space missions have brought astonishing accomplishments till date (e.g. 12 humans actually walking on the lunar surface). The ESA roadmaps of technology for the exploration of the Solar System have been designed to set the goal of fostering robotics exploration with the final aim to support human exploration. Within those technology roadmaps, spacecraft avionics techniques and technologies play a special and remarkable role. This talk provides a wide overview of the current technology programs and upcoming activities in the area of avionics, including mission for asteroids (AIM), Phobos (PHOOTPRINT), Mars (sample return and human), Moon (South Pole landing), Jupiter (JUICE), etc. The talk highlights the needs of new performing, agile and low cost avionics systems, as well as the corresponding quick and fast verification, and validation techniques |

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| 10:45 | Coffee break (00h30') |
| 11:15 | **Low cost avionics systems for fast track missions to the planets (00h30')**<br>*Presenter: Mr. HORMIGO, Tiago (Spinworks)*<br>Future exploration missions will require the development of new and advanced GNC-related technologies relying on the use of significantly more powerful avionics components than currently available. We put forward the argument that significant advances in low-cost/high-performance processing components, the widespread availability of specialized and open-source software/hardware resources, and the commoditization of vehicles which can easily serve as test platforms (e.g. multicopters, CubeSats), are poised to expedite the GNC development cycle through incremental, frequent, low-cost, high-return-on-investment experimentation - extending from initial algorithm formulation through ground/laboratory testing, flight testing, and finally in-space demonstration. Furthermore, through our own experience in the scope of several past and ongoing ESA projects, we also believe that a criterious use of these technologies, together with a phased transition to the space qualification of selected avionics components in a process duly supervised by experts at ESA, will ultimately enable the validation of radically new exploration capabilities through the execution of low-cost, fast track, GNC technology demonstration missions to the planets. |
| 11:45 | **Autonomy and FDIR of avionics systems for exploration (00h30')**<br>*Presenter: Ms. TATO, Cristina (SENER)*<br>Exploration missions are in all cases expeditionary by nature, but are as well expeditionary in terms of technology. They require specific solutions both in platform and payload that will be a novelty in the frame of space technology. As well the context and environment of these missions will make them unique and may involve a specific approach to many avionic functions as per FDIR.<br>In the recent years avionics for space community is progressing towards several areas of interest as: increased processing capabilities, harmonization, building blocks based designs or modelling techniques. In terms of FDIR function within a spacecraft all of these need to be considered as enablers to increase FDIR performance and capabilities. FDIR concepts and solutions to be provided in the frame of the exploration missions will need to have into account all these enablers when being proposed and developed.<br>This presentation is intended on the one hand to provide an overview of these exploration missions' key points regarding FDIR strategy. On the other hand the presentation will provide an insight on the current status and trends of FDIR approaches and into the way forward in terms of FDIR solutions. |

## Round table with introduction from ESA about Avionics Systems for Exploration Missions - Newton Conference Center (12:15-13:00)

- **Conveners: Mr. Guillermo, Ortega Hernando (ESA/ESTEC-Head Guidance, Navigation and Control Section)**

time title

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| 12:15 | **Round table - Avionics Systems for Exploration Missions (00h45')** |

## Lunch - Newton Conference Center (13:00-14:00)

## Session 2 - Automated Code Generation for AOCS - Newton Conference Center (14:00-16:00)

- **Conveners: Ms. GIROUART, Bénédicte (ESA/ESTEC- Control Systems Division); Mr. Sanchez de la Llana, David (ESA/ESTEC-Software Systems Division)**

time title

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| 14:00 | **Introduction (00h05')**<br>*Presenter: Ms. GIROUART, Bénédicte (ESA/ESTEC-Head of AOCS and Pointing Systems Section)* |

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| 14:05 | **Industrial and optimized auto-coding process for AOCS SW development in CD phase (00h25')**<br>*Presenter: Mr. BOURDON, J. (Airbus Defence and Space (F))*<br>Airbus Defence and Space continuously improves its functional avionics development process, willing to reduce its cost base, the development duration and improve the confidence in the design. In this continuous transformation, model-based design (MBD) approach has been the backbone of AOCS & GNC analyses and simulations for 20 years. Indeed, based on Matlab/Simulink modelling tools, AOCS & GNC teams design algorithms as well as equipment, dynamics and environment, allowing straightforward frequency analysis & time simulation, based on trans-nationally shared tools and processes.<br>Since the last 5 years, a step further has been reached, establishing this MBD approach over a multi-domain process (AOCS, On-Board SW & simulator teams), defining a complete process, from early design to S/C implementation and validation.<br>Two demonstrators have been carried out with CNES and DLR to validate it, from April 2012 to March 2013 (CSO and Sentinel-2). Then, this process has been presented and agreed by ESA, ESOC, CNES and DLR. This development process has been declared as the baseline for future projects in 2014 by the project entities (Earth obs. & sci., telecom). Hence, all the most recent projects are now deploying it: NGSAR, MetOp-SG, Merlin, Juice, Quantum and Eurostar eNeo.<br>In this operational context, and in addition to the technical prowess to generate automatically the code, the main following challenges shall be mastered: compliance to ECSS (E-40 and Q-80), code quality, CPU and memory budget, V&V (Model coverage analysis, Quality rule checking, Requirement tracing, Automatic documentation generation), in-flight operations and software maintenance. |
| 14:30 | **Model Based AOCS Design and Automatic Flight Code Generation: Experience and Future Development (00h25')**<br>*Presenter: Mr. BODIN, P. (OHB Sweden)*<br>OHB Sweden has almost 20 years' experience from using Model Based Design and Automatic Code Generation for AOCS flight application software. This presentation will give an overview of how these techniques have been used within different projects and what the experience has been. One of the main advantages of using Model Based Design and Automatic Code Generation is that the techniques allow for an integrated development of the AOCS functionality and the associated application software. The software development process resulting from this experience will be briefly presented. Finally, challenges and opportunities for future further integration of the AOCS and software development will be discussed. |
| 14:55 | **From 1995(MINISAT) to 2016(EUCLID): Auto-coding evolution for different types of AOCS (00h25')**<br>*Presenter: Mr. LLORENTE, S. (SENER (Sp.))*<br>Auto-coding tools emerged in the 90´s, as complement from several model-based design tools. SENER was one of the first companies to apply this type of tools for the implementation of auto-coded on-board SW for the MINISAT ACS. After that, the design and auto-coding tools have been continuously evolving, with tools enhancements allowing more controlled application of the auto-coding SW on AOCSs of different types, and this is becoming more widely used also for highly demanding missions.<br>SENER will present some highlights of the auto-coding processes applied along the years and missions, with emphasis on the most relevant aspects for improvement and formalisation of the processes, and its application to EUCLID AOCS as one of the most recent target science missions from ESA, where SENER applies the technique. Also some expectations for the future will be mentioned.<br>The review will touch relevant aspects like the share and organisation of the auto-coded SW in front of the manual SW and its integration, the overall SW specifications and SW testing particularities, etc. Also the options in the modelling and auto-coding, with specific constraints will be commented.<br>In general the evolving nature of the auto-coding tools and accessories, is also determining an evolving auto-coding process, tools and rules, with a wide range of valid and selectable configurations. Such evolving process and particularities may deserve an evolution of the ECSS to a general framework focussed on guaranteeing the models characteristics and the properties of the associated auto-coded SW. |
| 15:20 | **Integration of automatic code generation in a AOCS development process: feedback and perspectives (00h25')**<br>*Presenters: Mr. DANDRE, P. (Thales Alenia Space (F)), Mr. VERAN, G. (Thales Alenia Space (F))*<br>The AOCS engineers widely use model-based simulation tools for the definition and pre-validation of the algorithms to be implemented in the SW code. Introduction of Automated Code Generation tools have added new constraints and modified the development process and the roles between the AOCS engineers and the SW engineers. The classical V-cycle does not answer all items of this new approach. Model-based design has been introduced to provide a new methodology for the design and validation of an embedded software. This presentation will present the return of experience of Thales Alenia Space France (TAS-F) on this topic (Spirale, Sentinel-3, Göktürk) with a dedicated focus on the new roles, constraints and responsibility between AOCS team and SW team. The discussion will end with the perspectives of TAS-F on integrating a complete model-based design and validation process. |
| 15:45 | Break (00h15') |

## Round Table - Automated code generation for AOCS: return of experience, benefits and challenges - Newton Conference Center (16:00-16:30)

- **Conveners: Ms. Girouart, Bénédicte (Head of AOCS and Pointing Systems Section); Mr. Sanchez de la Llana, David (ESA/ESTEC-Software Systems Division)**

| time | title |
|---|---|
| 16:00 | **Round Table - Automated code generation for AOCS: return of experience, benefits and challenges (00h30')**<br>Following the presentations by several AOCS (and System) Prime industries on their experiences of Model Based Design and Automated Code Generation techniques for AOCS and AOCS SW production, the round table will allow exchanges, between the Presenters and the audience, on the following topics:<br>- Impact of the use of the Automated Code Generation techniques on the AOCS development process and cycle, in particular AOCS validation, AOCS SW production and testing<br>- Modelling rules for ACG: do's and don't and expected evolutions<br>- (Non-)Compliance with AOCS/coding standards<br>- New borders between specification and code: who does what?<br>- Modularity/versatility wrt mission specificities and industrial layout: re-use of models for code generation and interface with 'manual' code. |

## ADCSS 2016 closing remarks - Newton Conference Center (16:30-16:50)

# 10th Workshop on Avionics, Data, Control and Software Systems

# ADCSS 2016

**EXHIBITORS**

**Cobham Gaisler AB**

**Embedded Brains**

**Ramonchips**

**Skylabs**

**Space IC**

**TTTech**

**Microchip Atmel**

# Cobham Gaisler AB

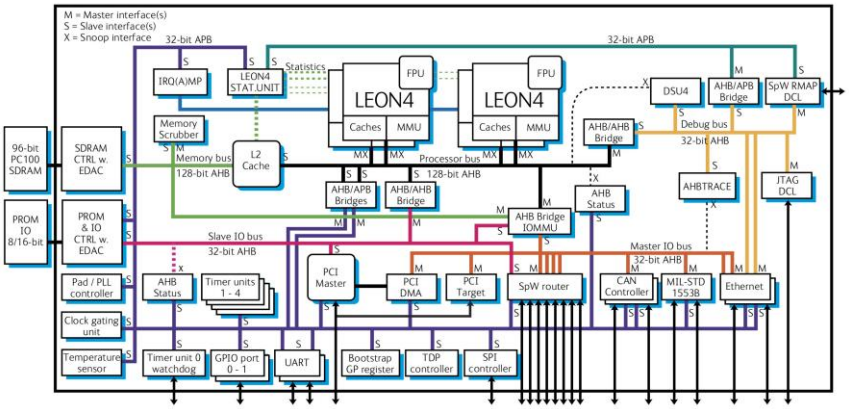
Cobham Gaisler AB is a provider of system-on-chip (SoC) solutions for exceptionally competitive markets such as aerospace, military and demanding commercial applications. Cobham Gaisler's products consist of user-customizable 32-bit SPARC V8 processor cores, peripheral IP cores and associated software and development tools. Cobham Gaisler solutions help companies develop highly competitive customer and application-specific SoC designs, as well as providing radiation- hardened components for the space market.

The key product is the LEON synthesizable processor model together with a full development environment and a library of IP cores (GRLIB). The LEON processor and the library of IP cores are highly configurable, and are suitable for SoC designs. The processor combines high performance and an advanced architecture with low gate count and low power consumption. Implementing the SPARC V8 architecture (IEEE-1754), the LEON processor offers a truly open and well supported instruction set.


*GR740 component*

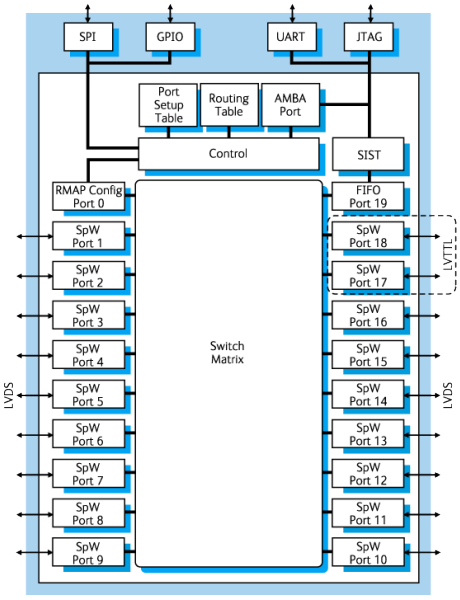
The Cobham Gaisler GRLIB IP core library is also the foundation for Cobham Gaisler's radiation tolerant processor and network components. The latest additions to Cobham Gaisler's device product portfolio are the GR740, a quad-core LEON4 FT SPARC V8 processor, and the GR718, an 18-port SpaceWire Router.

The GR740 device is a radiation-tolerant system-on-chip featuring a quad-core fault-tolerant LEON4 SPARC V8 processor, eight port SpaceWire router, PCI initiator/target interface, MIL-STD-1553B interface, CAN 2.0 interfaces and 10/100/1000 Mbit Ethernet interfaces.




*GR740 Block Diagram*

The GR740 was designed as the European Space Agency's Next Generation Microprocessor (NGMP) and is part of the ESA roadmap for standard microprocessor components. The GR740 is the first rad-hard implementation of the NGMP system-on-chip.




*GR718 Block Diagram*

The GR718 router implements a routing switch as defined in the ECSS-E-ST-50-12C SpaceWire links, nodes, routers and networks standard, supporting all mandatory and optional features. The router implements eighteen external routing ports, 16 of which with internal LVDS, an internal configuration port, and an internal port for system level test support.

The configuration port provides access to configuration and status registers, and the routing table, using the Remote Memory Access Protocol (RMAP) as defined in the ECSS-E-ST-50-52C protocol standard.

The router also fully supports the ECSS-E-ST-50-51C SpaceWire protocol identification standard.

# RTEMS - Real Time Operating System with SMP

**Background of RTEMS**
Real-Time Operating System for Multiprocessor Systems (RTEMS) originally developed in the late 1980s for the US Military to provide hard real time resource assignment. Since 1993 available as public source software under GNU Licence.

Widely applicable

- Deterministic performance and resource usage
- Multitasking and Multiprocessor capabilities
- Memory footprint < 32kB
- Boot time from 150ms
- Available for 15+ CPU families and 150+ BSPs
- 64bit internal time, respresenting nanoseconds since POSIX epoch (32 bit Classic API time types still available)

Open Source - Commercial Grade Software

- Free software, no restrictions or obligations placed on application code
- Open source code for OS, support components, tests, documentatio and development environment
- Test coverage is openly reported
- More than 50% of users are professionals
- embedded brains offers professional training and support

**New SMP features**

- Clustered scheduling
  - flexible link-time configuration
  - fixed-priority scheduler
  - job-level fixed-priority scheduler
- State of the art locking protocols
  - O(m) Independence-Preserving Protocol (priority inheritance)
  - Multiprocessor Resource Sharing Protocol (MrsP, priority ceiling)
- Lock-free timestamps
- Scalable timeout support
- Operating system core uses fine-grained locking
- C11/C++11 thread-local storage
- OpenMP 4.5 (GCC, libgomp)
- APIs
- - RTEMS Classic
- - POSIX threads
- - C11/C++11 threads

Hardware Implementation

- GR740 (LEON4 SPARC V8)
- GR712RC (LEON3FT SPARC V8 )
- NXP QoriQ (e.g. 24 processor T4240)
- Xilinx Zynq
- Altera Cyclone V
- everything else, we can do it

ECSS SW Qualification Challenges:

- Qualification of an Open-Source Software
- Nonlinear behaviour of Real Time OS combined with SMP
- Dynamics of using shard resources (e.g. Memory

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RAMONchips

In collaboration with

MacSpace

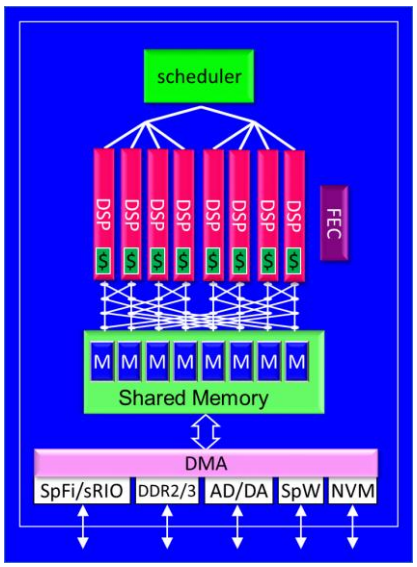
FP7 project, participants:
Ramon Chips (IL)
Thales Alenia Space (IT)
DSI (DE)
TU Braunschweig (DE)
Presto Eng (FR)
Arttic (FR)

# RC64 Many-Core DSP

## 64-Core High Performance Rad-Hard Single Chip Parallel DSP

## Enabling Software Defined Satellites

RC64, designed especially for software-defined satellites, is a many-core digital signal processor (DSP) enabling high performance computing in space. It integrates 64 cores, 4MB shared memory, rich I/O and 12 high-speed SpaceFibre SERDES.




RC64 employs fine-grain parallelism, delivering linear scalability and near-linear speedup. The on-chip 256-port shared memory enables direct access of each core. A hardware ***Synchronizer / Scheduler*** automatically manages parallel tasks, removing task management overhead from the cores and software and enabling nearly-perfect dynamic load balancing.

Applications include SDR, transparent and regenerative (IP routing) GEO and LEO telecom payloads, EOS, SAR and space robotics.

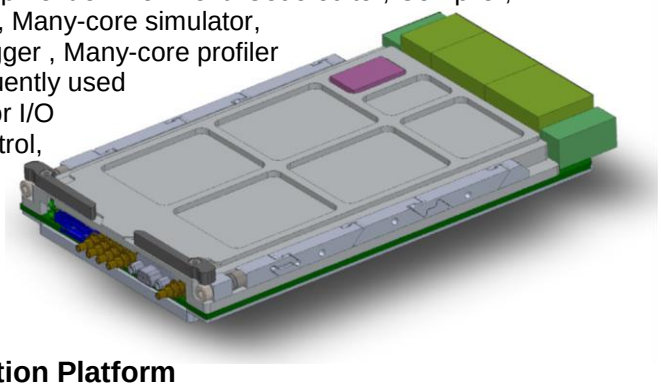
RC64 samples are planned for 2017, EM and early FM parts are due in 2018 and Class S FM parts are expected in 2019.

### *Preliminary Specifications*

- Fabricated on 65nm CMOS process
- Rad-hard RadSafe™ Ramon Chips technology
- 64 CEVA X1643 DSP cores with 64 SP Floating Point Units
- 300 MHz clock frequency
- 75 GMAC/s (16-bit), 38.4 GFLOP/s
- Modem (LDPC and Turbo-code) accelerator
- Hardware synchronizer/scheduler
- 4 MByte shared data memory
- DDR3 32-bit memory controller with 16-bit Reed-Solomon ECC at 800 MWord/s supporting 4 GByte memory
- NAND flash controller for boot and NVM storage, page ECC
- 12 high-speed SpaceFibre/sRIO SERDES, 60 Gbit/sec.
- 48 LVDS links at 800 MWords/s for ADC/DAC
- Power 1-10 Watts, depending on modes
- Package 624 pins CCGA or PBGA
- Temperature range –55ºC to +125ºC
- Temperature monitoring and stabilization
- Rad hard: 300 kRad(Si), SEL and SEU protected, EDAC for on- & off-chip memories, error detectors, memory scrubbing
- MIL-STD-883 / MIL-PRF-385353 Class S, ESCC-9000

### Software Development Tools

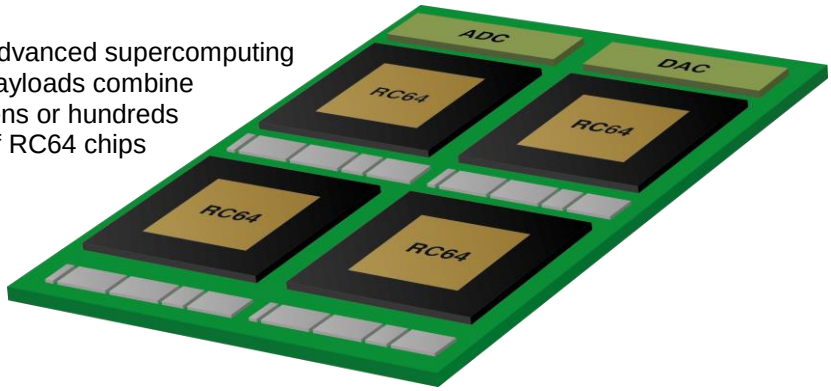
- Integrated development environment: Code editor, Compiler, assembler, linker, Many-core simulator, Many-core debugger , Many-core profiler
- Libraries for frequently used functions, APIs for I/O configuration/control, host control and monitoring



### Hardware Evaluation Platform

- 3U-VPX board, one RC64, ADC or DAC
- Custom board, 16 RC64 units super-computer

Advanced supercomputing payloads combine tens or hundreds of RC64 chips



## SKYLABS AT A GLANCE

*SkyLabs is space technology oriented company providing miniaturized on-board data handling solutions and innovative approach to space engineering. SkyLabs is focused on fault tolerant hardware and software development, digital signal processing, fast prototyping, space and ground segment communication, and development of custom solutions for high-tech embedded systems, mainly in the field of on-board data handling. In recent years we have become also specialized in development of IP Core.*

**DIFFERENT**
Leveraging new ideas to introduce innovative technologies for the emerging aerospace market.

**RESILIENT**
Sophisticated fault tolerant design enables previously unreachable nano-scale applications.

**EFFICIENT**
Deliver more by combining next level of integration with reduced overall system complexity.

## Platform NANOsky I

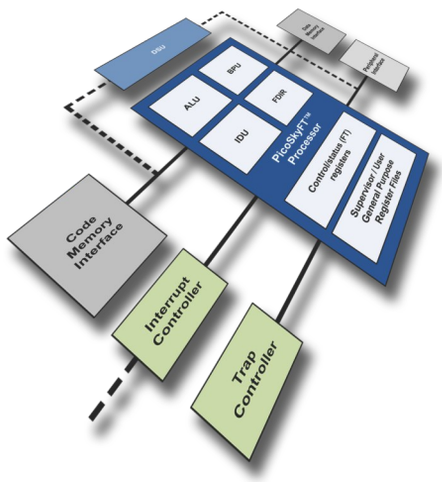
### Avionics platform for small-micro satellitles

The new avionics platform NANOsky is tailored to meet increasingly demanding requirements on reliability, fault tolerance and low power consumption. SEE tolerant, innovative error mitigation techniques, sophisticated three-level FDIR policy, redundancy on all critical functions and thoughtful component selection ensure robustness, high reliability and the availability of the platform.
Their form factor, mass and dimensions make them attractive for the small and nano satellite market and launch vehicle segments where a reduction in the size and mass of their power and data handling sub-systems are key factors. The capacity for on-board data handling, data storage and data transfer meets the current trend towards more advanced missions in smaller spacecraft.
Small in scale and big on features are the key advantages addressing the new horizons of the emerging space market.

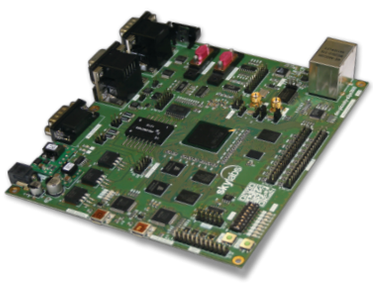
## PicoSkyFT™ processor IP Core

### Small footprint - fault tolerant processor

PicoSkyFT™ is designed for embedded processing functions within SoC by providing another layer of abstraction to tackle complexity and adequately respond to rapidly changing needs, and securing development and verification efforts. Rad hard by design, small size, low power and configurable architectural features optimised for hard, real-time processing make this type of core suitable for multi-core specialised applications. The PicoSkyFT™ is a high performance Fault Tolerant 8/16-bit embedded processor. The processor provides a rich and powerful instruction set with 16-bit operation codes with single cycle execution on most instructions to provide throughputs of 1 MIPS per MHz. The SEE tolerant design is achieved by several error mitigation techniques and incorporated fault detection, isolation and recovery policy to increase reliability.

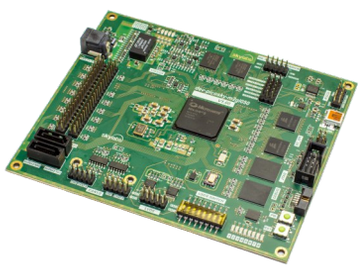



## PicoSky™ Development boards family



### PicoSky™ Development Board ProASIC3

The board fully exploits features of Microsemi ProASIC3e® FPGA. It incorporates a set of various memory technologies to enable a versatile IP cores development, testing and prototyping platform.'Special care has been taken, in order to provide comprehensive interoperability ecosystem. Thus the board features interfaces like dual SpaceWire, dual CAN, RS422/232, LVDS, USB, Ethernet, and many others.



### PicoSky™ Development Board IGLOO2/SmartFusion2

PicoSky™ Development Board IGLOO2 / SmartFusion2 is a newcomer to the SkyLabs product portfolio. It is based on Microsemi IGLOO2 or SmartFusion2 FPGA which delivers more resources in low density devices, with the lowest power consumption, proven security and exceptional reliability. The board has been designed in a way to fully support evaluation of PicoSkyFT™ soft core processor and development of a complete ecosystem around it. The SmartFusion2 version adds a high performance ARM Cortex-M3 processor that can deliver up to 1.25 DMIPS / MHz.

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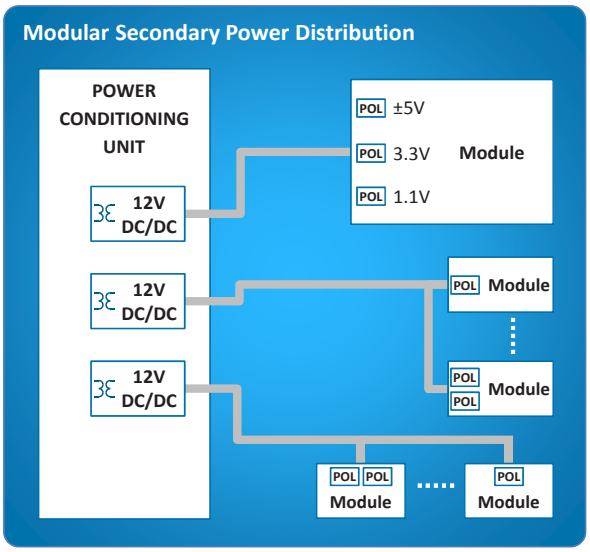
info@skylabs.si | www.skylabs.si

# ADCSS 2016

## Easy Applicable POL Converters for High Efficiency and Re-Use

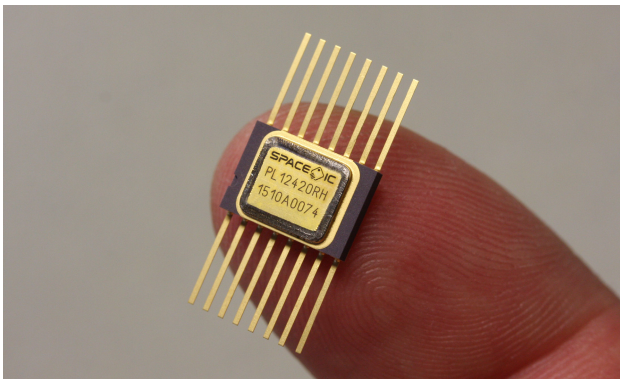
### POWER ARCHITECTURE



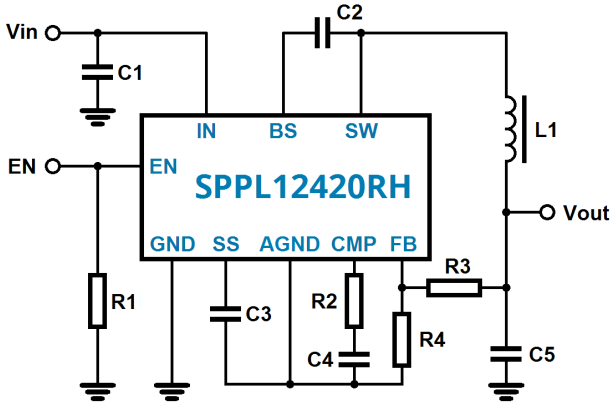

The evolution of power distribution in spacecraft goes into direction of modular architecture. Especially secondary power distribution from the satellite bus to the modules can be made more efficient by applying modular design.
For this, easy applicable solutions for local power conversion are needed, which can deliver exactly the required voltages and currents to the load and can be directly integrated into the power consuming modules. Such approach makes the single modules easy re-usable and can be realised using SPACE IC integrated point-of-load (POL) converters.

### SPACE IC POL SOLUTION

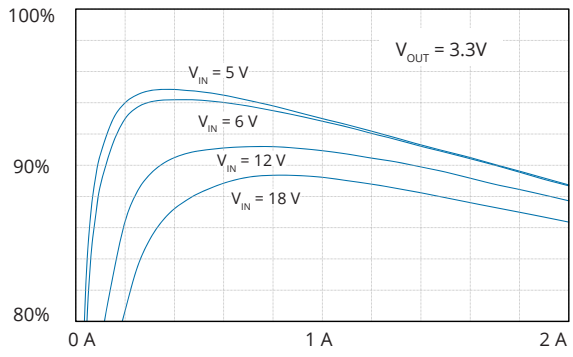
- Monolithic IC (ESCC9000)
- Only few passive external components
- Radiation-hard, hermetic flatpack 16
- 2 A continuous output current
- 4.5-24 V input voltage capability
- 0.923 V minimum output voltage
- Latch-up immune (SOI technology)
- Made in Germany - ITAR/EAR free




### EASY APPLICABLE




### BEST EFFICIENCY





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Ensuring Reliable Networks **TTTech**

# ADCSS 2016 – TTEthernet Product Development

## a) TTE End System Controller Space and TTE Switch Controller Space(1)


Available in 2017

**Key Benefits**

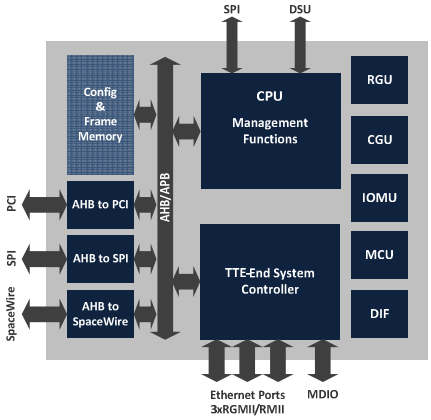
- Three supported traffic classes
  - Ethernet (IEEE802.3)
  - Rate-constrained (ARINC 664 p7)
  - Time-triggered traffic (SAE AS6802)
- 3 Ethernet channels, full duplex at 10/100/1000 Mbit/s
- Up to 0.5 MByte of frame memory
- Operating temp.: -55°C to +125°C
- Max. power consumption of 3W
- Rad-tolerant (100 krad (Si) and SEU/latch-up immunity up to 60 MeV/cm2/mg)
- Max. power consumption of 3W

The TTE End System Controller Space is an integrated device supporting standard Ethernet, rate-constrained and time-triggered Ethernet communication. Three different host interfaces (SPI, PCI and SpaceWire) provide flexibility in connecting it to different host controllers.

### Quality of Service and Partitioning

Supports 128 send/256 receive virtual links which can be fully separated via 8 memory partitions allowing the use of standard Ethernet and time-triggered/ rate-constrained traffic on the same network without interference.

- Suitable for highly dependable, distributed real-time systems with guaranteed response times
- 1024 send COM ports, 2048 receive ports
- Flexibly configurable periods
- Diagnosis and status registers
- Profiled IP/UDP, sampled and queued ports
- 3 x 10/100/1000 Mbps via RGMII or 3 x 10/100 Mbps via RMII

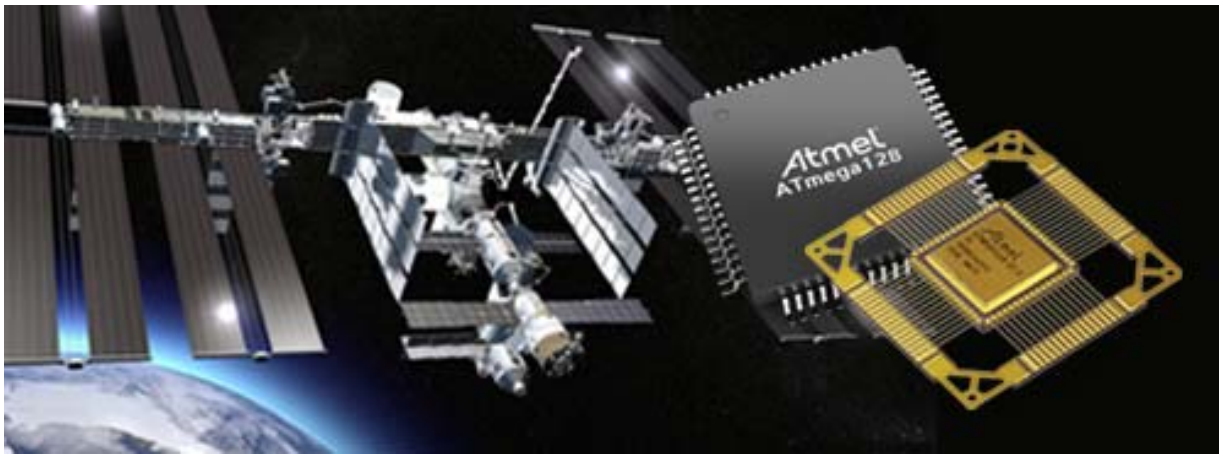



*(1) The companion 18-port Switch Controller development was partly funded by ESA FLPP-3.*

## b) TTEthernet Test Bed(2)

Recently TTTech has started the development of a generic test bed which allows fault injection and standardized test routines to verify the robustness of own and third-party end-system (network interface) cards. It utilizes the same 24-port lab switches and 3-channel interface cards used in the Ariane 6 development program.


*(2) This development will be partly funded by an ESA GSTP-5 project.*



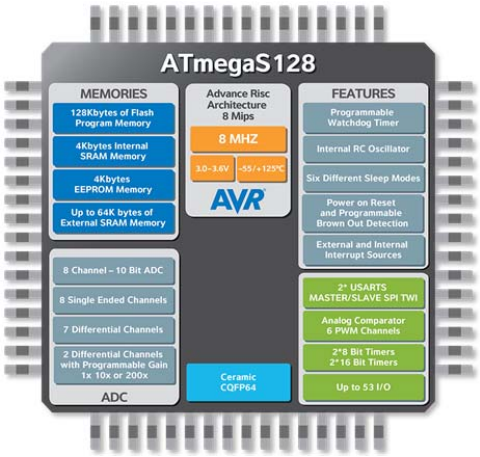

From the last 20 years, **Atmel** is established as main space microprocessor supplier out of US. With worldwide sales of over 5000 flight models based on SPARC architecture, Atmel's processor experience and knowledge has an unrivalled flight heritage.

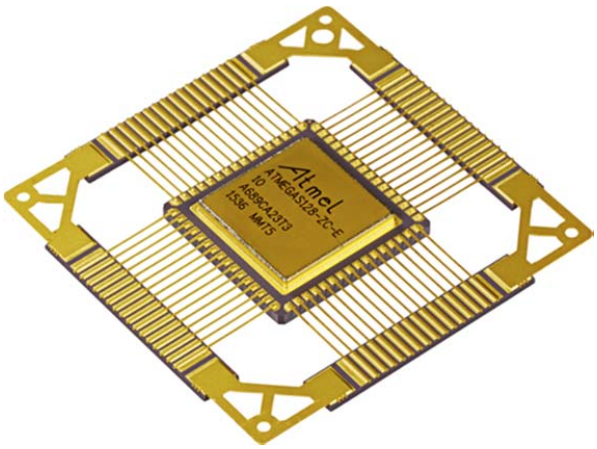
In order to answer to market trend and demand to benefits from proven other domains devices, reducing costs but also to provide the right level of performances and quality required for Space, **Atmel proposes Rad Tolerant microcontrollers**.

By using select devices from Atmel's industrial or automotive portfolio, **Atmel Aerospace** reuses the full metal mask set and manages epitaxial improvements to be latch up immune under radiation. This methodology doesn't change the device functionality and the new Rad Tolerant device is fully compatible with the full ecosystem available for commercial product: development tools, evaluation boards …

Associated to radiations performances improvement, **Atmel** applies to **Rad Tolerant** devices the same space quality flow than all usual space parts: full wafer lot traceability, space screening and a space qualification flow as done for QMLQ & QMLV grade components. This qualification is done for ceramic hermetic package version with all required steps: visual inspection, PIND test, Burn-in and Group A to D tests.

For high volumes and low cost driven program, a plastic version can be also proposed with product spec, full temperature range tests and traceability.




The first **Atmel Rad Tolerant product** available is the **ATmegaS128**, derivative from ATmega128 commercial device: AVR 8 bits, 10MIPS, 3.3V, ADC, UART, PWM, TWI & SPI at 3.3V in QFP64 package.

**ATmegaS128** is today selected in many kind of missions, some FMs already delivered and is planned for flight in 2017 after product introduction on the market end 2015.

**ATmegaS128** achieved radiations performances results are:

- No Latch-up at 62.5 MeV/mg/cm2 @ 125°C (3.6V Vcc max)
- Full SEU characterization done @125°C for all functional blocks from 2 to 62.5MeV.cm²/mg. Saturation reached at 30 MeV.cm²/mg. Estimated SER : 1 event every 1000 days (LEO*)
- TID = 30 Krad

**AMR and AVR new Rad Tolerant microcontrollers coming in 2017:**

- AVR **ATmegaS64M1**: 10 MIPS with CAN & Motor control, QFP32
- ARM **Cortex M3, SAM3XE RT** : 100 MIPS,CAN, Ethernet & dual bank flash, QFP144
- ARM **Cortex M7, SAMV71 RT** : 600 MIPS, CAN, Ethernet, FPU & MPU, QFP144

**Atmel** has been acquired by **Microchip** since April 2016 and is Aerospace activity is now named **Microchip Aerospace & Defense**. It will bring to Aerospace much more rad tolerant devices opportunities around microcontroller: PHYs, NVM, RS485, HV devices and so on.

# FUTURE EVENTS

## 2016

### TEC-ED & TEC-SW Final Presentation Days

6-7 December 2016, ESA/ESTEC, The Netherlands
https://indico.esa.int/indico/event/146/

### Model-Based System and Software Engineering - Future directions

8 December, ESA/ESTEC, The Netherlands
https://indico.esa.int/indico/event/161/

## 2017

### Simulation and EGSE for Space Programmes - SESP2017

28-30 March 2017, ESA/ESTEC, The Netherlands
http://esaconferencebureau.com/2017-events/17c01

### TEC-ED & TEC-SW Final Presentation Days

30-31 May 2016, ESA/ESTEC, The Netherlands
https://indico.esa.int/indico/event/165/

### 11th Workshop on Avionics, Data, Control and Software Systems - ADCSS2017

17-19 October 2017, ESA/ESTEC, The Netherlands
adcss.esa.int


DATA
SYSTEMS
CONTROL
SYSTEMS
SOFTWARE
SYSTEMS