# ADCSS Session 2
## Compact on-board computer architectures

# "SmartOBC":
# integrating functions in Platform Computer

# TAS-I experience

Gianluca Aranci

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# Agenda

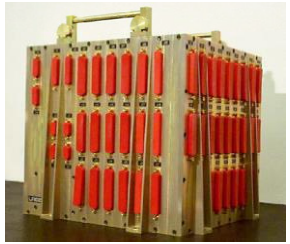
- Integration trends in Platform Computer
- Integrating new functions
- Perspectives and opportunities: COTS, Multicore Processors, Reprogrammable FPGA

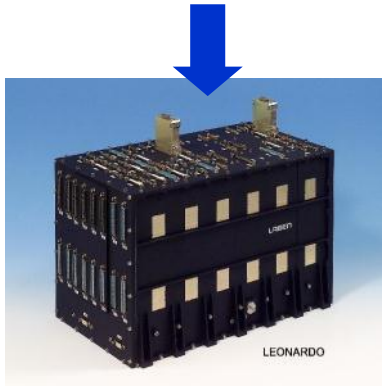
# ADCSS Session 2: Integration Trends in Platform Computer

- The interest to combine several functions and interfaces within a single "Avionic" Computer is always present in the space community
- A typical Avionic system in the 90s was composed by (e.g. XMM-Newton):
  - On Board Data Handling Computer (Processor, TM&TC, FDIR, Avionic Bus IF)
  - OBDH Remote Terminal(s) to collect discrete TM and execute TC towards S/C users
  - AOCS Computer
  - AOCS Remote Terminal(s) to acquire attitude sensors and command actuators
- The need of many units was caused by the limited performances of available Microprocessors qualified for space application and sizing of discrete electronic devices to be used for I/O interfaces

# ADCSS Session 2: Integration Trends in Platform Computer

- At beginning of 2000 the availability of ERC-32 processor allowed to combine in one single Computer equipment the OBDH and AOCS processing
- Miniaturization and new technologies (e.g. Rigid-Flex PCB) permitted also to integrate Remote Terminals in the same box.



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# ADCSS Session 2: Integration Trends in Platform Computer

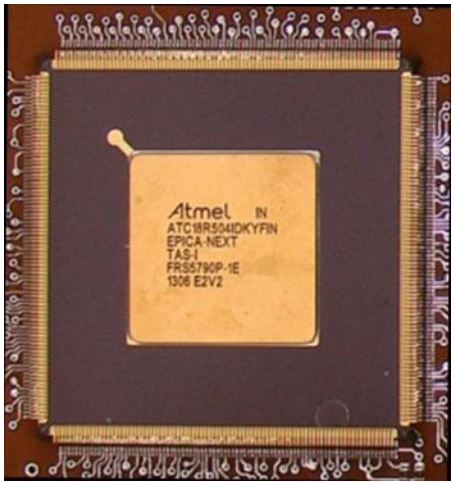
- From 2010 key technological elements have become available
  - Leon Processor (SPARC-V8)
  - System-On-Chips and sub-micron ASIC techno (180nm)
  - Larger FPGA (RTAX)
  - MEMS sensors

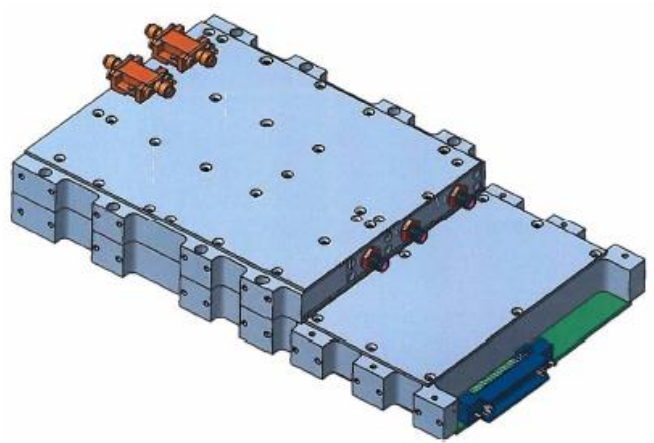
- The above activated a process "similar" to one observed in consumer electronics. The "SmartPhone", combining and integrating in a single device functions previously spread in several gadgets:
  - Navigation
  - Orientation
  - Data Storage

## TAS new generation "Smart" Platform computer products now include:

### > Navigation

- Star Trackers processing within Leon-3FT Processor embedded in Epica-Next SoC
- GNSS Receiver miniaturized module (based on AGGA-4 ASIC)

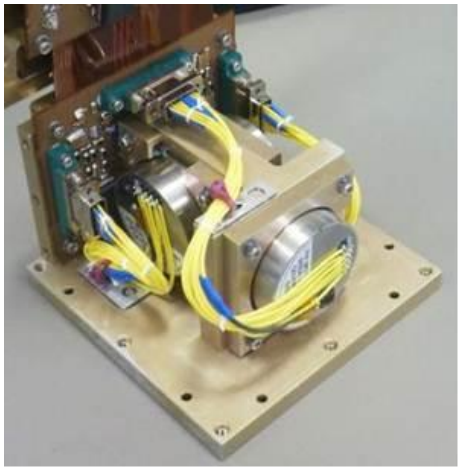


## TAS new generation "Smart" Platform computer products now include :

### > Orientation

- 3 axis Coarse Rate Sensor gyroscope based on MEMS technology up-screened to space quality, suitable for application in top-class Telecom satellites



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## TAS new generation "Smart" Platform computer products now include :

### > Data Storage:

- 32Gbit Local mass Memory with autonomous Packet Store management integrated together with the Telemetry/Telecommand and FDIR module

## Smart computer Pros and Cons

### > Cons

- Constraints for the shared resources (OCXO, Power supplies,..)
- Complex EMC/EMI design
- Complex mechanical and thermal accommodation of the internal functions/modules
- Demanding AIV activity (at equipment level)
- Reduced Flexibility and Intricate Reparability
- Reliability (?)

## Smart computer Pros and Cons

### > Pros

- Increased competitiveness at system level (cost increase at equipment level is largely compensated by cost reduction at system level)
- Sharing of critical and expensive elements, e.g. OCXO common to GNSS RX and OBT, single DC/DC Converter, Mechanical Box,…
- Better physical budgets (mass, volume and power)
- Optimized procurement
- Optimized interface among the modules
- Reduced harness at system level
- Simpler AIV activity at system level

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# ADCSS Session 2: Integration Trends in Platform Computer

- Further improvements and opportunities are expected in the presented trend thanks to:

  - Commercial Of The Shelf components (COTS)
  - Multicore processors
  - Very Large Reprogrammable FPGA

  } Deep submicron silicon techno

## COTS

- COTS components are generically considered of interest in view of competitiveness (cost reduction) …
- … furthermore, COTS are juicy because features/performances available in the consumer/automotive domains will be probably never available in a space qualified component (mainly because manufacturers have no interest to invest money to cover space hi-rel qualification huge cost considering the business volume)
- Examples : silicon MEMS (accelerometers, gyros), GNSS receiver FE electronics

## Multicore Processors

- Although the effort spent to integrate more functions in the Platform Computer, today we still must use many discrete CPUs, due to limited performances of the single Leon core.
- Independently on discussion on going about the future specific core to adopt (Leon, ARM, …), multicore approach permits to efficiently combine on a single silicon device the processing of several functions:
  - GNSS Autonomous navigation
  - Extended Star Tracker based functions: rate measurement, tracking robustness, data fusion
  - Mass Memory File Management System and CFDP
  - Security : TM Encryption and TC Decryption & Authentication → HW/SW integrated solutions

## Multicore Processors (cont')

- Question: is it better one single hi performance processor or multi core processor?
  - From consumer world indication is in favor of multi-core
  - Multicore chip can run at lower clock frequency providing same overall perfo
  - SW tasks partition can be more efficient (if SW is developed properly)
  - SW tasks segregation and failure effects

## Very Large Reprogrammable FPGA

- Increased Integration of the electronic
- Full computer in one board
- Further improvements:
  - Flexibility of reprogrammable FPGA allows mission specific customization
  - Development schedule compression no need to redesign board
  - Mass, volume, power consumption
  - Cost
  - Reliability (?)

## Deep Submicron silicon techno

- Combining Multicore Processor with very large reprogrammable FPGA in one single device
- Full computer in one device!
- Challenges:
  - Define “standard” functions and interfaces to be implemented in the “fixed” section
  - Select the Processor
  - Ensure durability/suitability of the design for a very long time justifying the huge development costs

# THANK YOU !!