

# ADCSS 2016 - Day 2 – Mega-Constellations - Compact Spacecraft AVIONICS and Mixed Criticality Systems



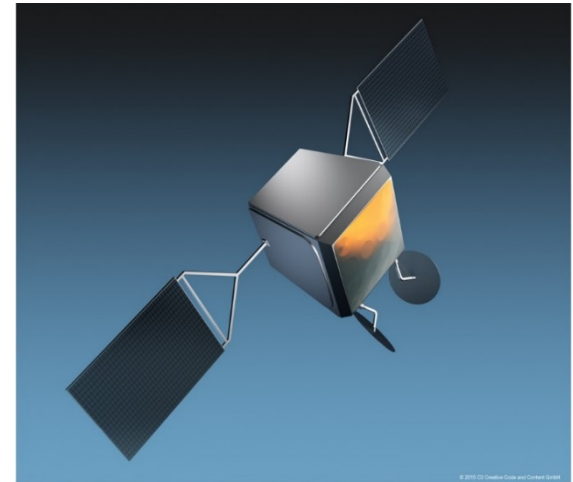
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The satellite market is evolving rapidly and concepts of **mega-constellations involving 100's of satellites** have been proposed and are in some cases currently under development. There are many challenges to overcome for such large constellations to become a reality.

These platforms will probably/certainly be re-used for other mission. Their architecture and retained technologies are therefore of general interest.

During this ADCSS second day, we shall touch upon particular aspects for what concerns the **on-board data handling system requirements** for these types of satellites.



**Facts & Figures**

 size	 less than <b>150 kg</b>	 up to <b>4</b> built every day	 <b>900</b> satellites to be built
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 **AIRBUS**  
DEFENCE & SPACE



# Options to reduce budgets (kg .. W .. L .. €)

- ❑ Less Units : Integrating functions and merging them in in smaller number of electronic units (e.g. OBC, RTUs)
  - Not always easy as some units are “connector limited”
  
- ❑ Less connectors
  - Multiplexing more signals on less wires (serial busses, serial networks)
  - Merging power lines and data lines ?
  - Fiber optics ?
  - Wireless ?
  
- ❑ More compact equipment: Integrating sensors or part of sensors/actuators processing chains in OBCs/RTUs (e.g. Corse IMU)

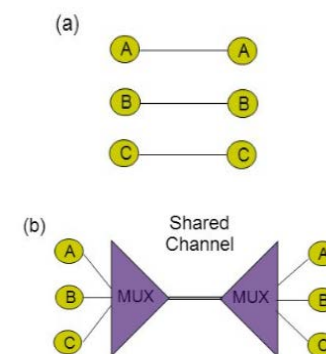


Figure 4: Photo of the SpaceCube 1.5 multi-function avionics implementation (image credit: NASA)

# Options to reduce budgets (kg .. W .. L .. €)

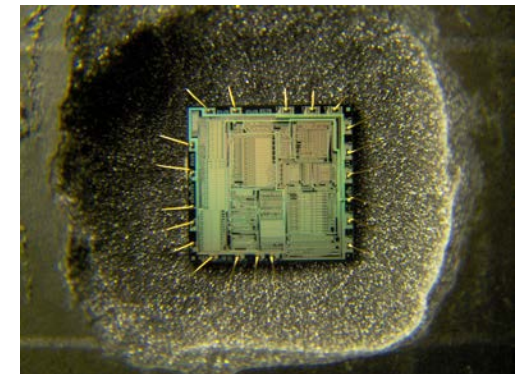
## ❑ Less devices

- SCOCs making best use of advances in microelectronics



## ❑ Using more COTS devices

- Yes, but screening and evaluations can be tricky and costly
- Mitigating radiation induced effects can be complex
- Giving up on reliability and/or availability to reduce costs is not always an option



The availability of :

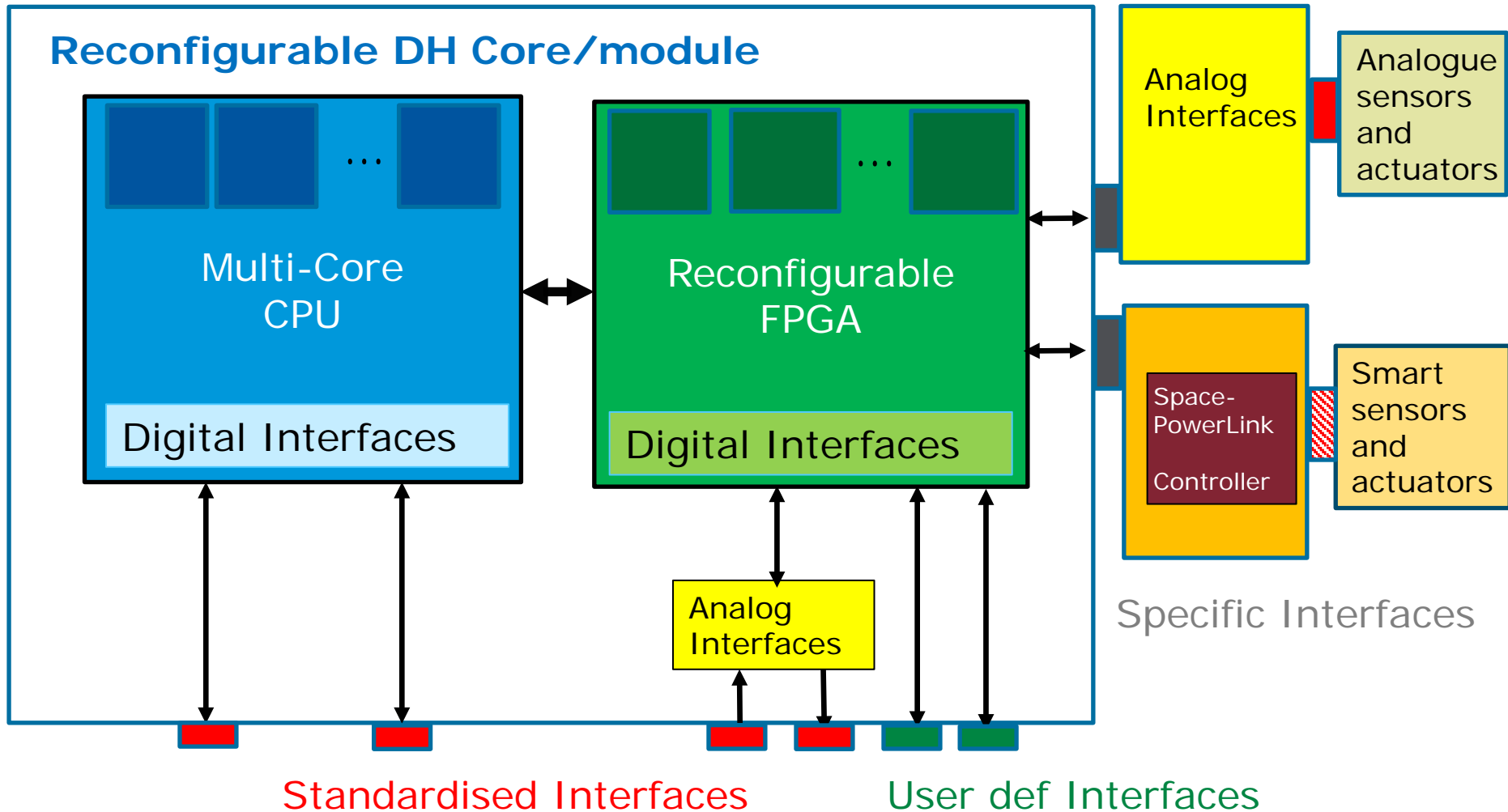
- **Multicore processors**
- **Reconfigurable FPGAs for space**
- **High speed and very high speed links**

opens new possibilities to implement functions often processed locally at sensor or unit level to be executed either fully or partially in the central computer.

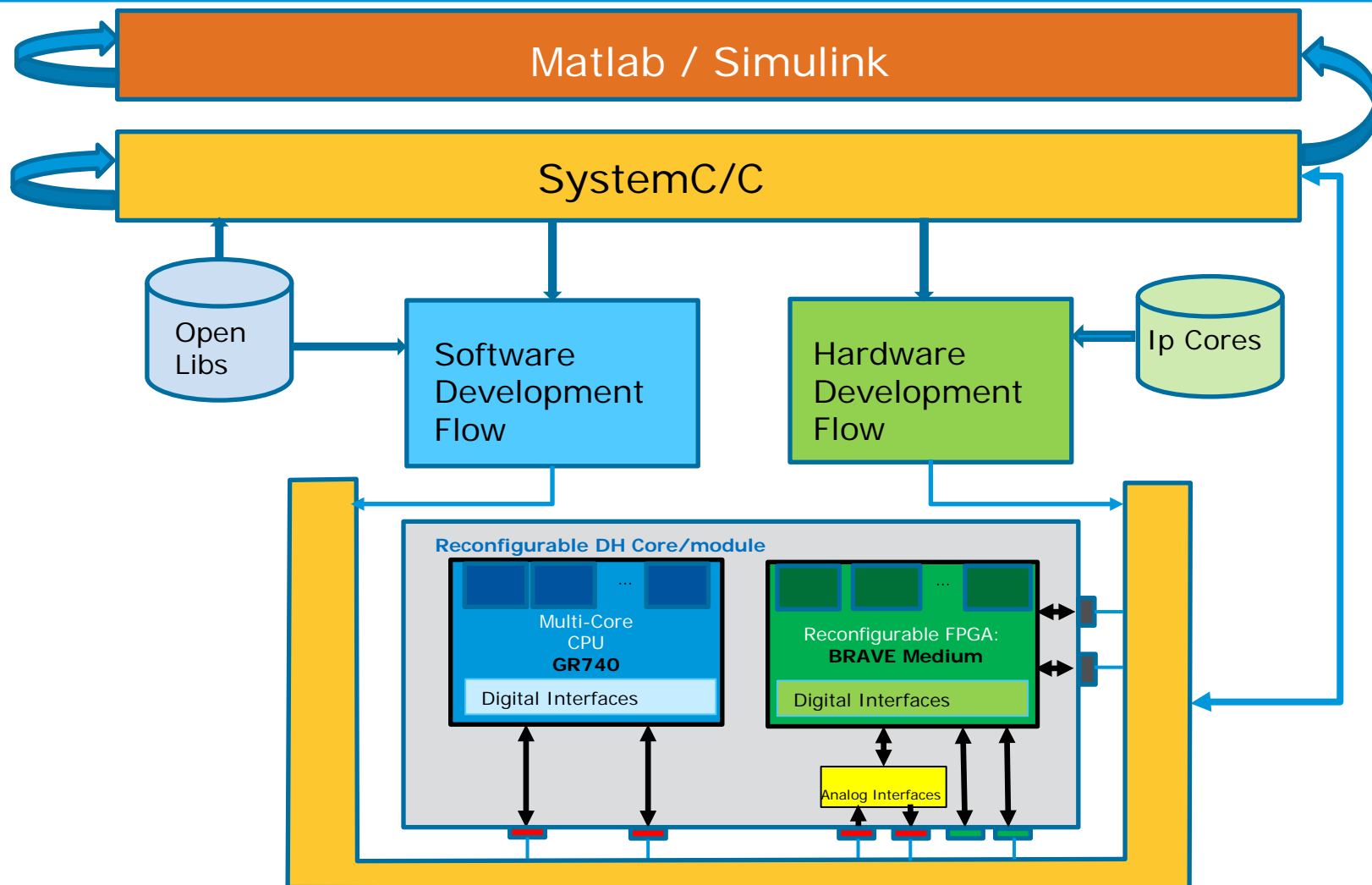
Such functions often belong to **different criticality domains** (e.g. OBC and payload processing). Besides these possibilities, new challenges are also introduced, especially in ensuring that the various functions do not interfere with each other.



# Compact Reconfigurable Avionics Concept : Reconfigurable Data Handling core



# Compact Reconfigurable Avionics: Development flow



The scope of the second day of ADCSS is focused on the challenges and opportunities of having **higher integration of functions in to the on-board computer as opposed the more traditional distributed architecture.**

OBC equipment suppliers will give their views on challenges and opportunities with current state of the art building blocks and future needs.

The last session of the day is dedicated to challenges on the execution of **SW of mixed criticality** on the same processor in particular on multi-cores CPU's.

*Objective of the day: Fostering interaction between stakeholders ... i.e. Us*

*Welcome to ADCSS 2016 Day 2 !*